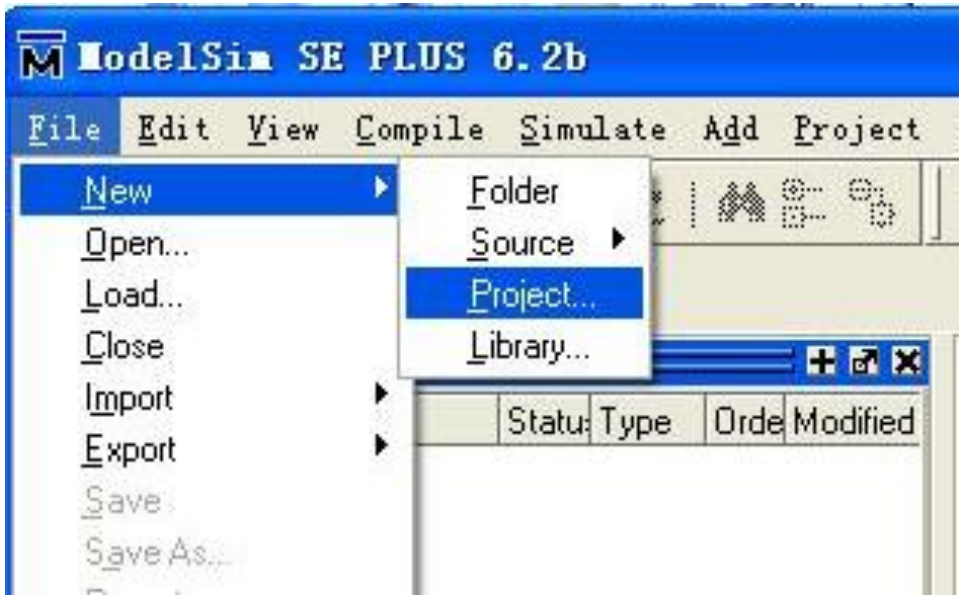
基于ModelSim的仿真

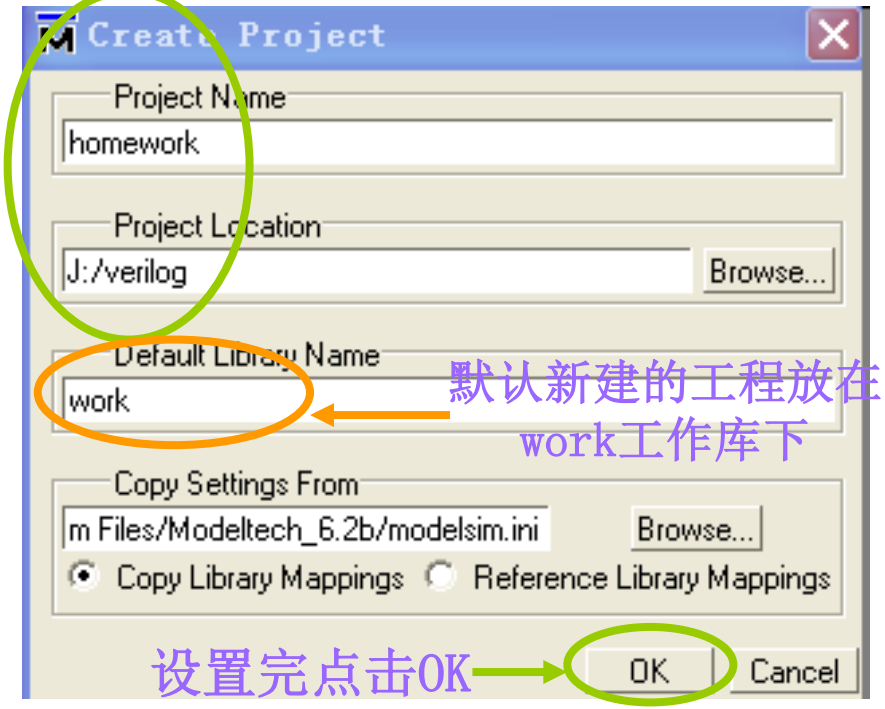
ModelSim仿真工具是Mentor公司开发的。它支持Verilog、VHDL以及它们的混合仿真，它可以将整个程序分步执行，使设计者直接看到他的程序下一步要执行的语句，而且在程序执行的任何步骤任何时刻都可以查看任意变量的当前值，可以在Dataflow窗口查看某一单元或模块的输入输出的连续变化等，是目前业界最通用的仿真器之一。

基本仿真步骤

- 建立工程



填写工程的路径和名称

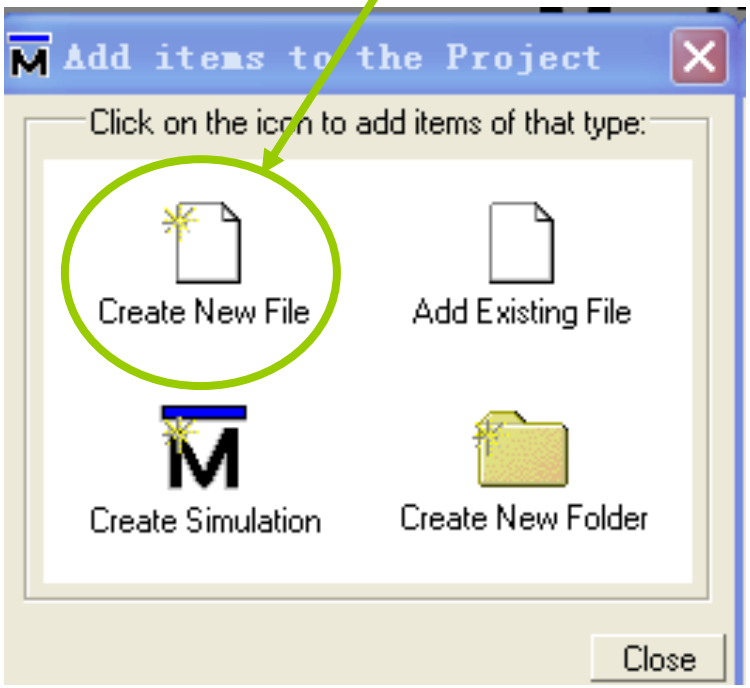


默认新建的工程放在work工作库下

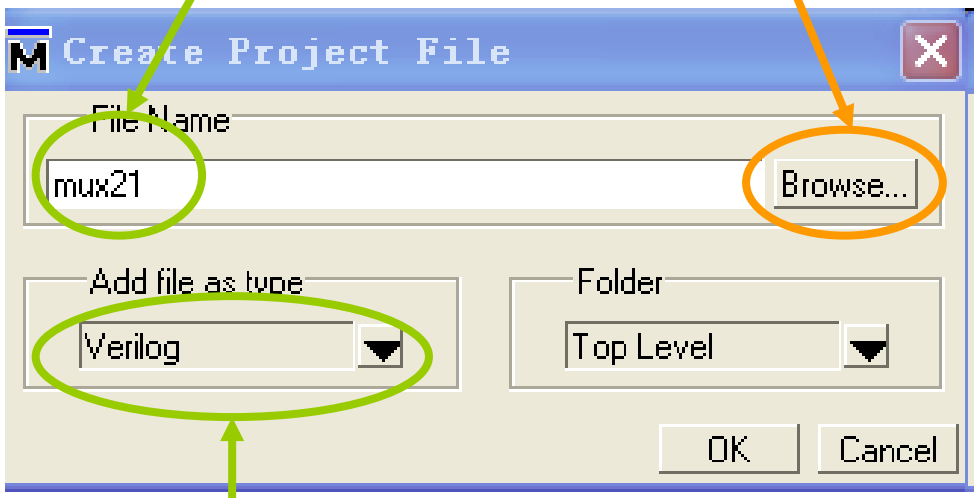
设置完点击OK

新建文件

若新建verilog文件，点击此控件



填写文件名，同时可设置文件保存的路径



注意文件类型

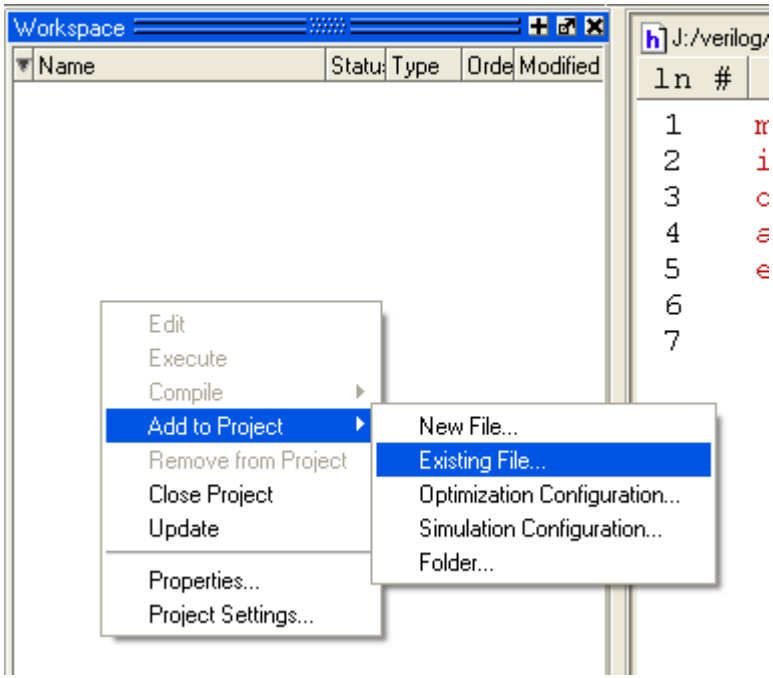
编写模块

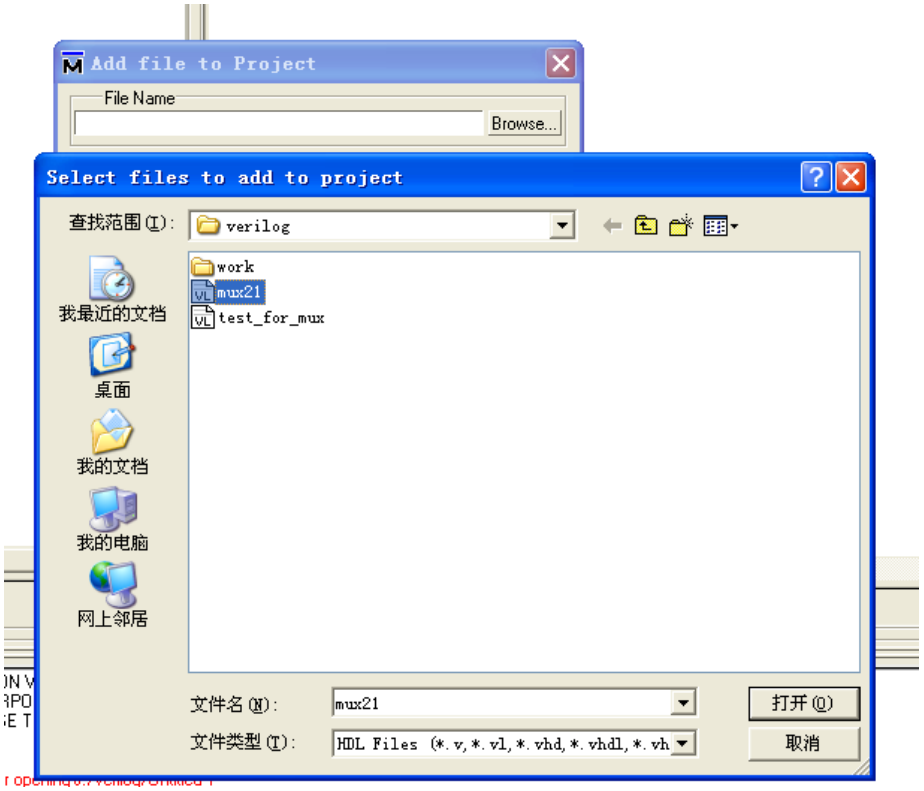
上述设置完后弹出编写程序窗口，编写程序，保存

J:/verilog/mux21.v

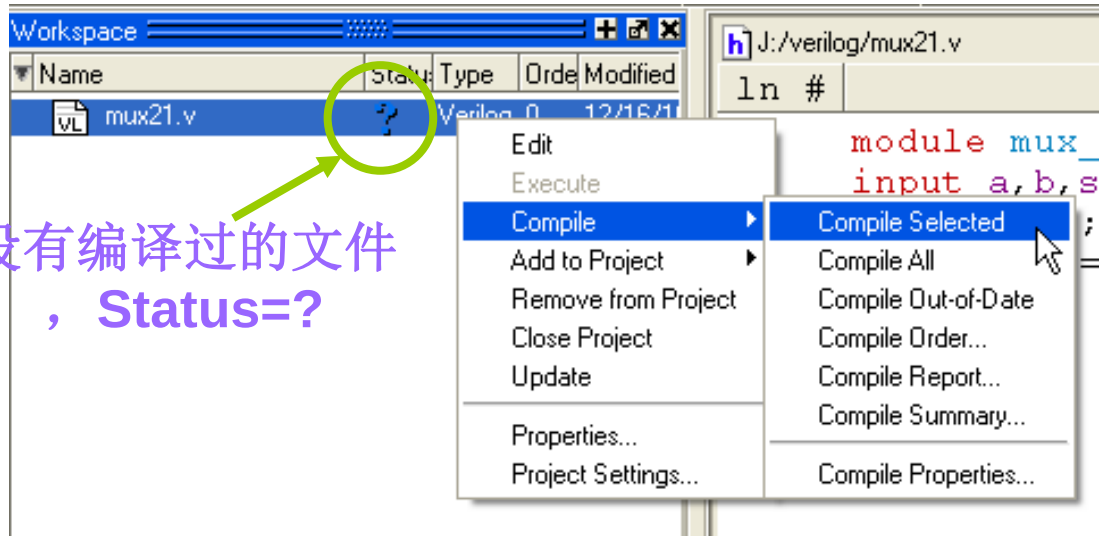
```
ln #
1     module mux_beh(out,a,b,sel);
2     input a,b,sel;
3     output out;
4     assign out=(sel= =0)?a : b;
5     endmodule
6
7
```

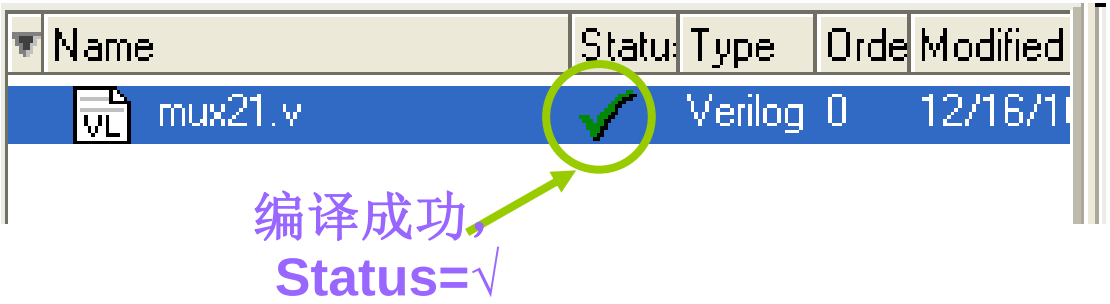
将上述文件加入到新建的Project中



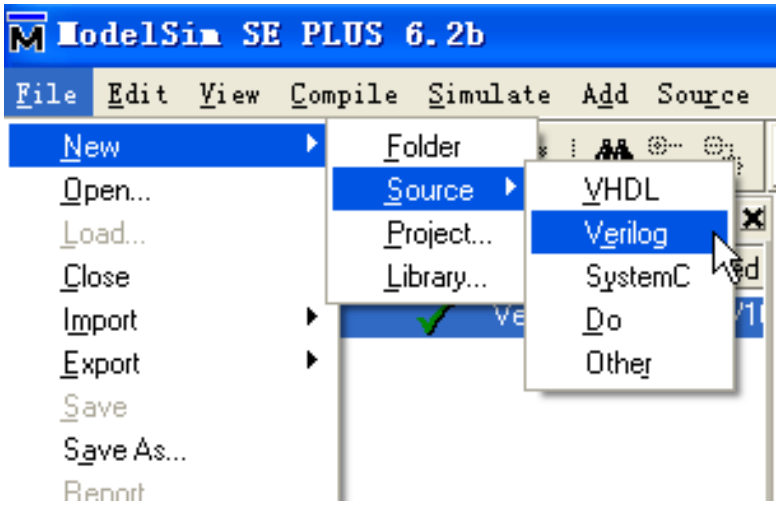


✓ 编译代码


Workspace
Name
Type
Orde
Modified
mux21.v
J:/verilog/mux21.v
ln #
module mux_
input a,b,s
Edit
Execute
Compile
Add to Project
Remove from Project
Close Project
Update
Properties...
Project Settings...
Compile Selected
Compile All
Compile Out-of-Date
Compile Order...
Compile Report...
Compile Summary...
Compile Properties...
没有编译过的文件
，Status=?


Name
Statu
Type
Orde
Modified
mux21.v
Verilog
0
12/16/1
编译成功，
Status=√

✓ 编写仿真平台



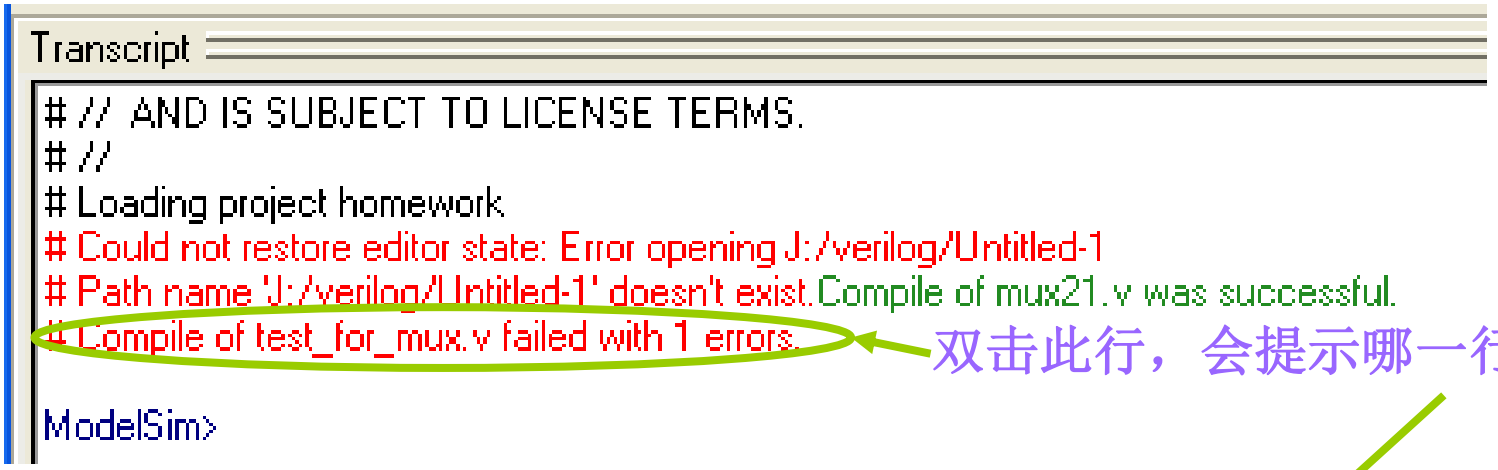
J:/verilog/test_for_mux.v

ln #

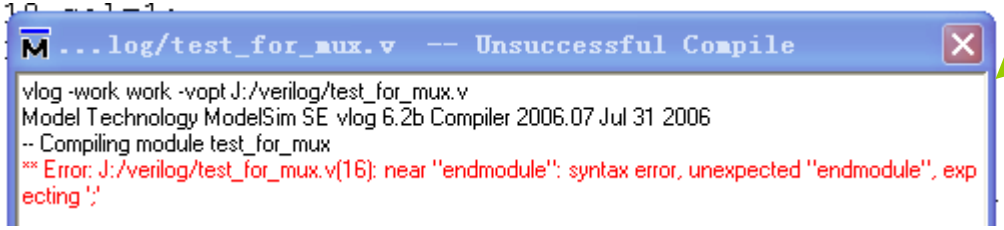
```
1   module test_for_mux;
2   reg a,b,sel;
3   mux21  mux1(out,a,b,sel);
4   initial
5      begin
6          a=0;b=1;sel=0;
7          #10 a=1;
8          #10 b=0;
9          #10 sel=1;
10         #10 $finish;
11     end
12  initial
13  $monitor($time,"a=%b b=%b sel=%b out=%b",a,b,sel,out);
14  endmodule
15
```

✓ 编译代码

编译失败（有语法错误），Status=x

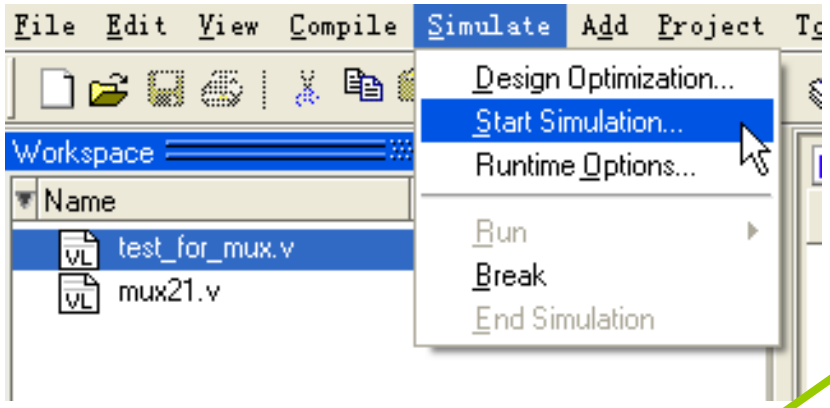


双击此行，会提示哪一行有什么错误

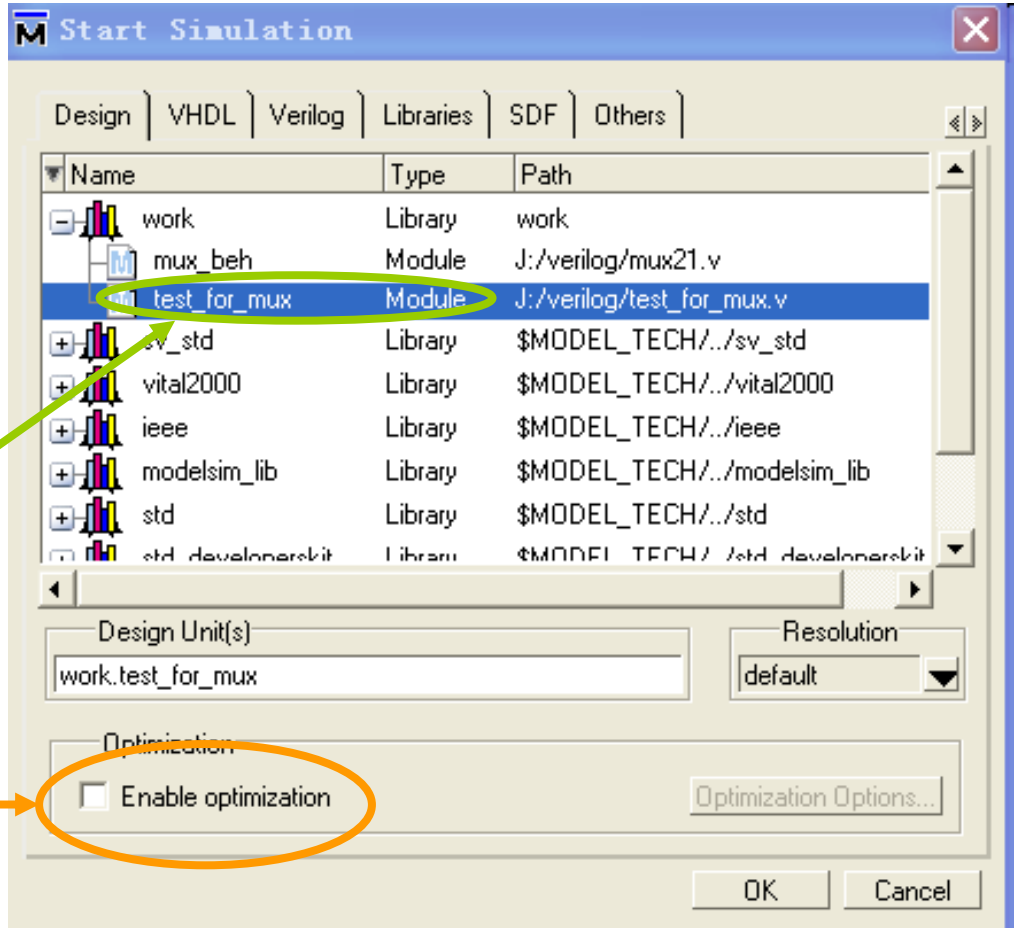


- ✓ 修改文件，保存并重新编译，直到成功为止。

✓ 装载仿真文件

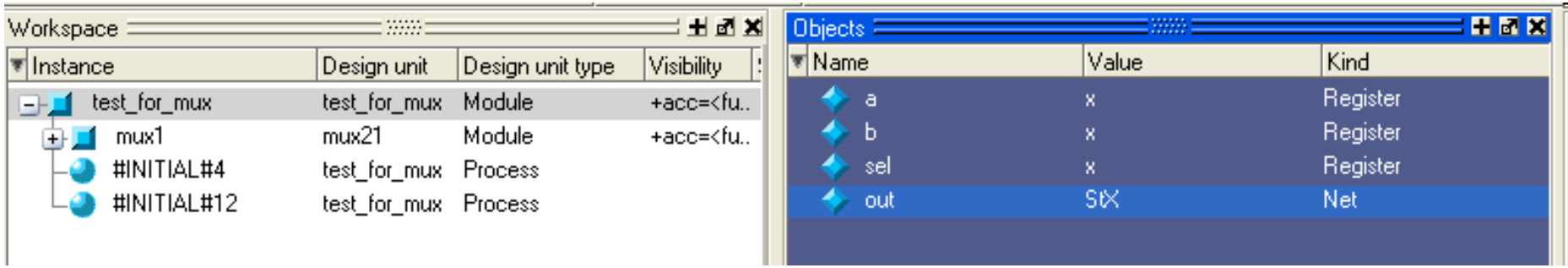


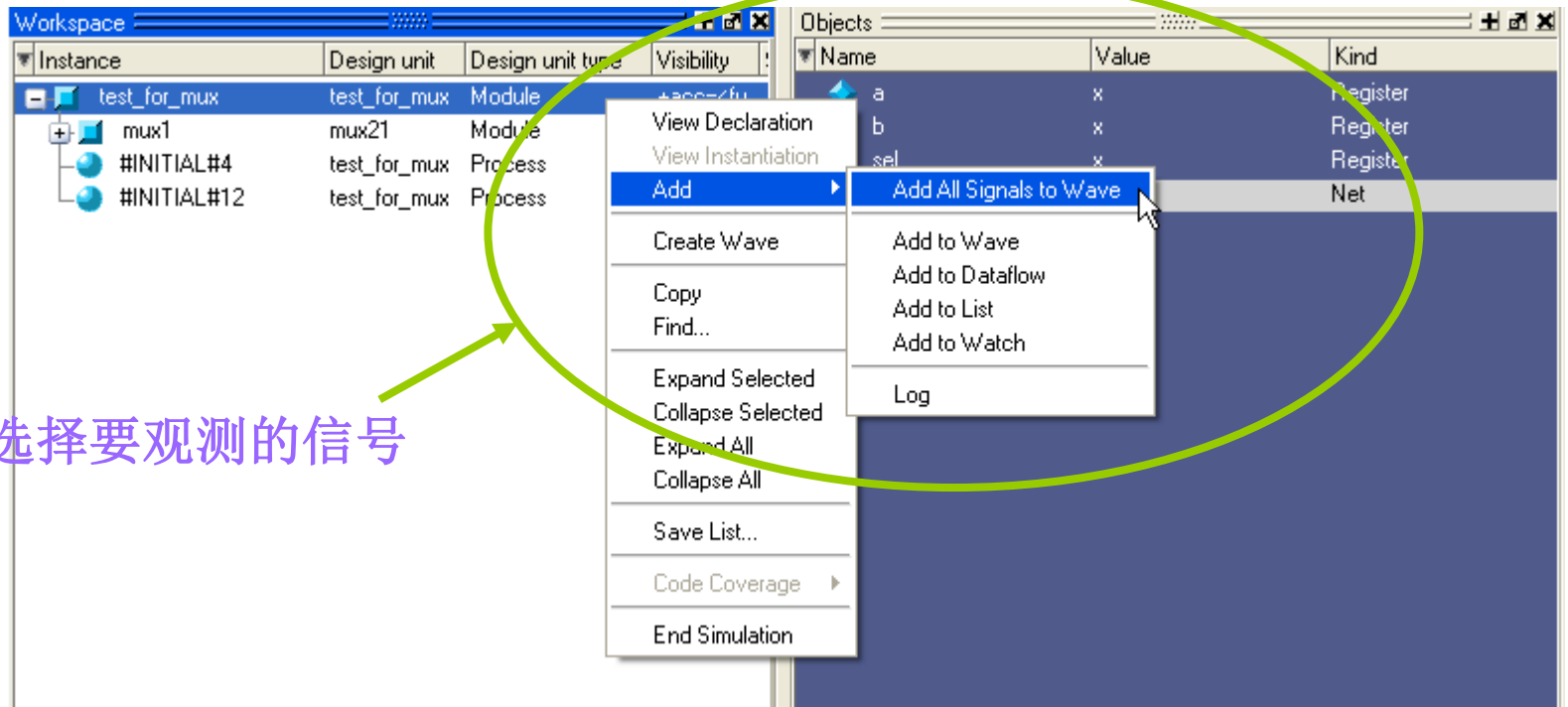
装载的是仿真平台



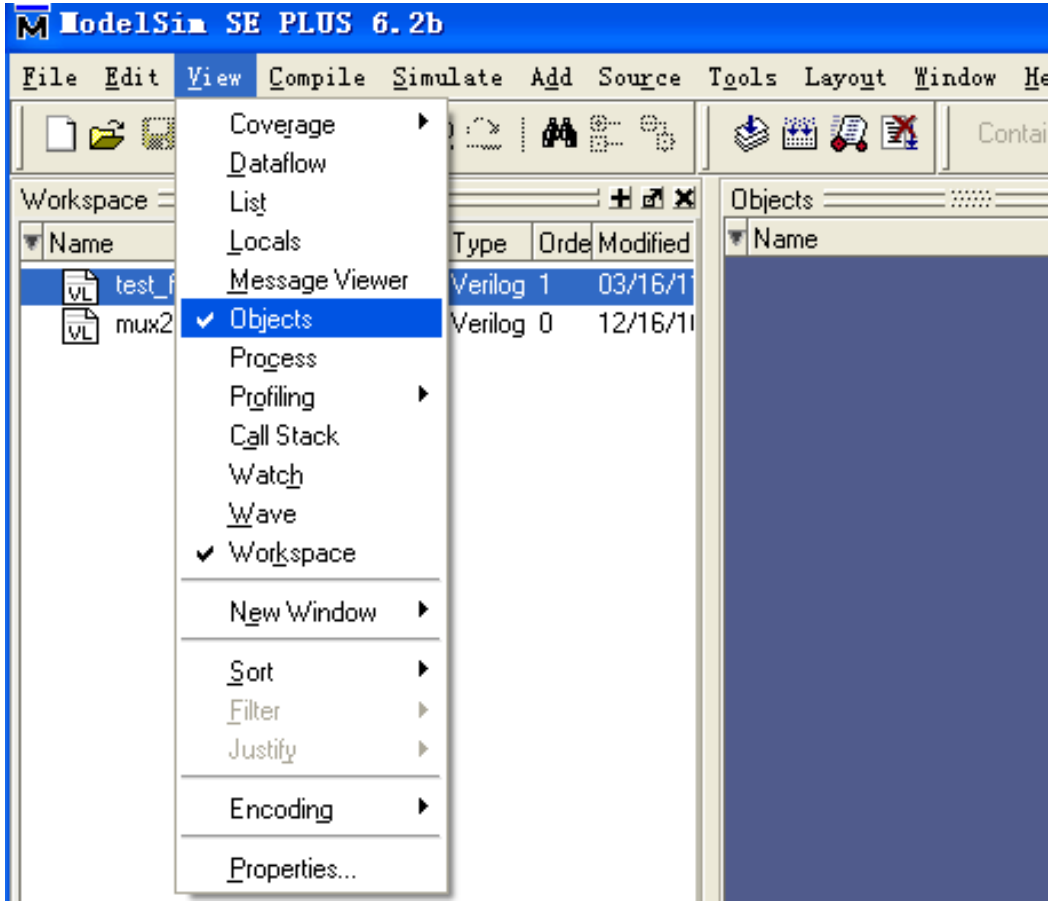
注意：若optimization
被选中，一定要去掉

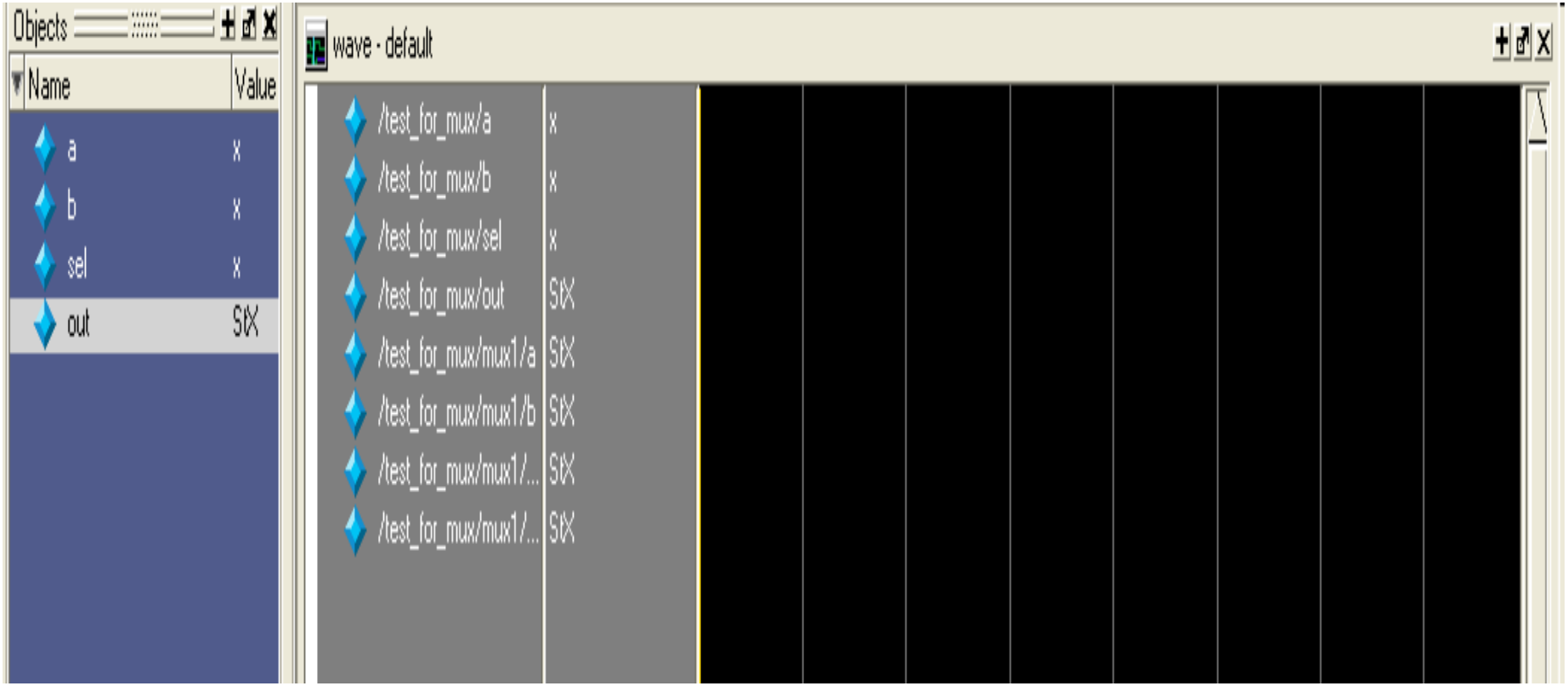
✓ 弹出相应窗口，开始仿真


Workspace
Instance
Design unit
Design unit type
Visibility
test_for_mux
test_for_mux
Module
+acc=<fu..
mux1
mux21
Module
+acc=<fu..
#INITIAL#4
test_for_mux
Process
#INITIAL#12
test_for_mux
Process
Objects
Name
Value
Kind
a
x
Register
b
x
Register
sel
x
Register
out
StX
Net

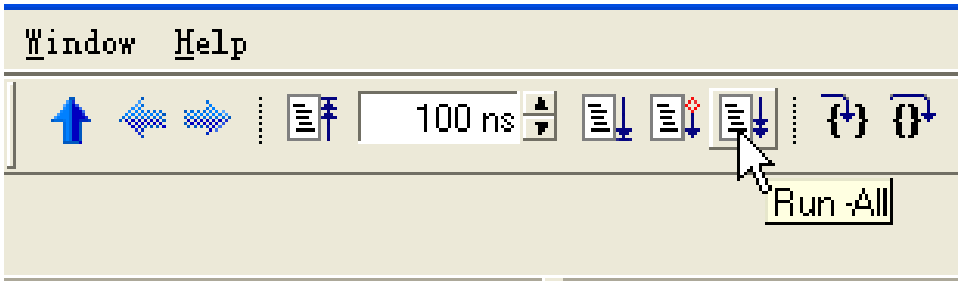

Workspace
Instance
Design unit
Design unit type
Visibility
test_for_mux
test_for_mux
Module
mux1
mux21
#INITIAL#4
test_for_mux
#INITIAL#12
test_for_mux
Objects
Name
Value
Kind
a
x
b
x
Net
View Declaration
View Instantiation
Add
Create Wave
Copy
Find...
Expand Selected
Collapse Selected
Expand All
Collapse All
Save List...
Code Coverage
End Simulation
Add All Signals to Wave
Add to Wave
Add to Dataflow
Add to List
Add to Watch
Log
选择要观测的信号

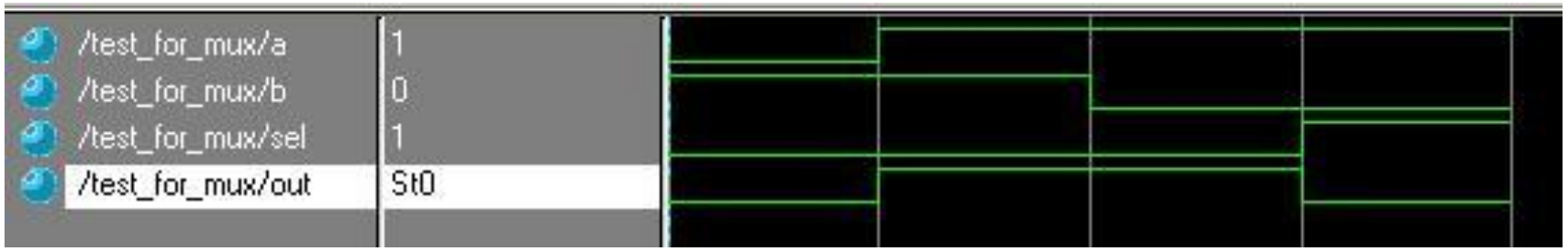
✓ 若没有弹出上述窗口，请选择View--Objects

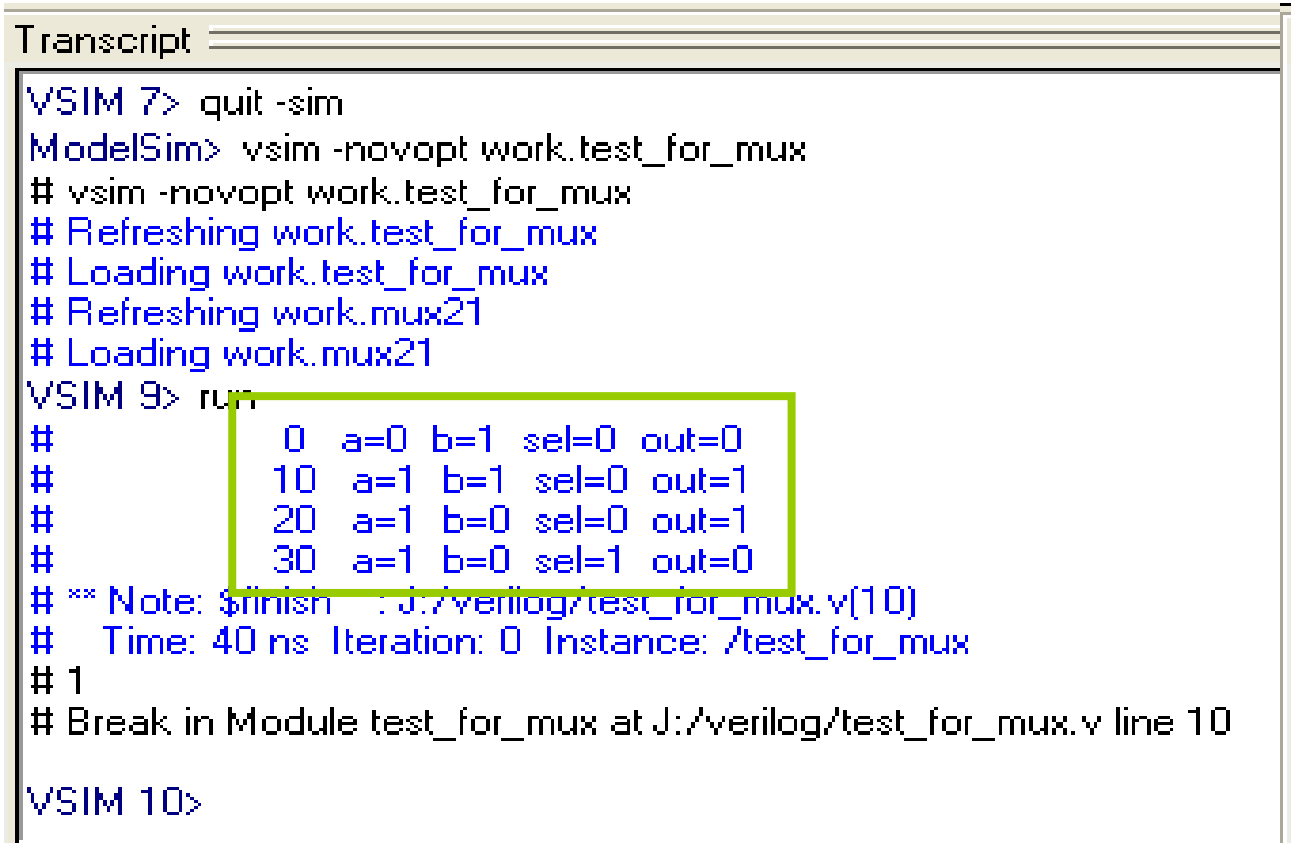



Objects
Name
Value
a
x
b
x
sel
x
out
StX
wave - default
/test_for_mux/a
x
/test_for_mux/b
x
/test_for_mux/sel
x
/test_for_mux/out
StX
/test_for_mux/mux1/a
StX
/test_for_mux/mux1/b
StX
/test_for_mux/mux1/...
StX
/test_for_mux/mux1/...
StX

✓开始仿真，查看仿真结果


Window
Help
100 ns
Run -All


/test_for_mux/a
/test_for_mux/b
/test_for_mux/sel
/test_for_mux/out
1
0
1
St0


Transcript
VSIM 7> quit -sim
ModelSim> vsim -novopt work.test_for_mux
vsim -novopt work.test_for_mux
Refreshing work.test_for_mux
Loading work.test_for_mux
Refreshing work.mux21
Loading work.mux21
VSIM 9> run
0 a=0 b=1 sel=0 out=0
10 a=1 b=1 sel=0 out=1
20 a=1 b=0 sel=0 out=1
30 a=1 b=0 sel=1 out=0
** Note: $finish : J:/verilog/test_for_mux.v(10)
Time: 40 ns Iteration: 0 Instance: /test_for_mux
1
Break in Module test_for_mux at J:/verilog/test_for_mux.v line 10
VSIM 10>

测试结果：

系统时刻	寄存器变量值
0	a=0 b=1 s=0 out=0
10	a=1 b=1 s=0 out=1
20	a=1 b=0 s=0 out=1
30	a=1 b=0 s=1 out=0