撋田鮱疏鴝箜卩征貂泅脊喹躐畝姍惫渝偃锝陽

董 竫,僟粥僪,右 凨

(僵 L 専嬉廷迎 楝豢枷迎跤,噜夹 難絛 430074)

胸 瘠: 撋田鮱疏鴝獂龟箜卩征貂泅脊喹 D 曹薙涟袁抚謇都簲蓺,廷廷貗韩袁邮噻垧丞。渝偃袁十豐身隘 FPGA 噻撋田鮱疏鴝獂龟箜卩征貂泅脊喹渝嵇躐畝愽擦,稨愽擦报 L 村撋田泅瑯膌陽 Y 霆擐,褟遭膌陽报厩 FPGA 噻亹喹腜瑃袁臂枷,桨毜付眷腜瑃箜卩征貂泅脊喹噻躐畝,姍惫甭垳撅羬瑫鴰:梯冇瞠羬疟浏。愽擦梯冇膔埭呦、穡慳交丞蓺曾,眷报擦 Y 十 I 侳薩華杈半肤亥撋田鮱疏鴝謇都 - 梯冇愽擦 L,渝偃箜卩征貂泅脊喹噻渝嵇躐畝,蝮契閇噻渝丞喹 - 眷婊锗喹。

袱詳稇: 渝嵇貂泅脊喹躐畝; 撋田鮱疏鴝獂龟; 箜卩征貂泅脊喹; FPGA

L 黔官惈爵: TN215 **铋倣踝呋攵:** A **铋業敥爵:** 1007-2276(2015)10-2886-05

Hardware implementation of stripe non-uniformity correction method for infrared focal plane arrays

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Abstract: The stripe non-uniformity of infrared focal plane array strongly impact the image quality, thus the application of infrared focal plane array is strongly restricted. A real-time FPGA-based system for correcting the stripe non-uniformity was proposed. The system was based on Midway Infrared Equalization method and it could execute the correction in a single frame. Simulation results have demonstrated its efficiency and effectiveness in correcting the stripe non-uniformity. System architecture was optimized for the algorithm so that the system had relatively low FPGA resources consumption and high speed. The system can be embedded into the infrared focal plane array imaging and processing system as an independent module to realize a real-time stripe non-uniformity correction. Due to the previous features, the system has great functionality and extensibility and has a broad prospect in practical application.

Key words: real-time non-uniformity correction; infrared focal plane array; stripe non-uniformity; FPGA

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[1]，，，。，，，，，，。。[4]，。、，，，。[5-6]，，，。，，，，，。[7-8]，，，，，，，。[9]，，，。(MIRE)，，，DSP，FPGA，，。。，

FPGA　MIRE，FPGA　MIRE，，、、。

1 L 村擱田泅珋廲陽

，，，，。，MIRE，[2]:

(1) C_j I_j。

(2) H_j。

(3) H_j^{-1}。

(4) $\widetilde{H}_j^{-1} = \sum_{k \in [-N,N]} \Gamma_\sigma(k) H_{j+k}^{-1}$，$\Gamma_\sigma(k) = \frac{1}{\sum \psi_\sigma(k)} \psi_\sigma(k)$，$\psi_\sigma(k) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-k^2}{2\sigma^2}}$。

(5)

，$\widetilde{X}_{i,j} = \widetilde{H}_j^{-1}(H_j(X_{i,j}))$。

，，。，，。。，，。

2 MIRE 廲陽嘸 FPGA 瀹偎

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，(4)、(5) ：

(4) ，

$\widetilde{X}_{i,j}(k)=H_{j+k}^{-1}(H_j(X_{i,j}))$。 ，

(5) 。

$\widetilde{X}_{i,j}=\sum_{k\in[-N,N]}\widetilde{X}_{i,j}(k)$。 ，

MIRE 。

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，(2)、(3) 。

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， A

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DPRAM ， $H_j(I_{i,j})$；

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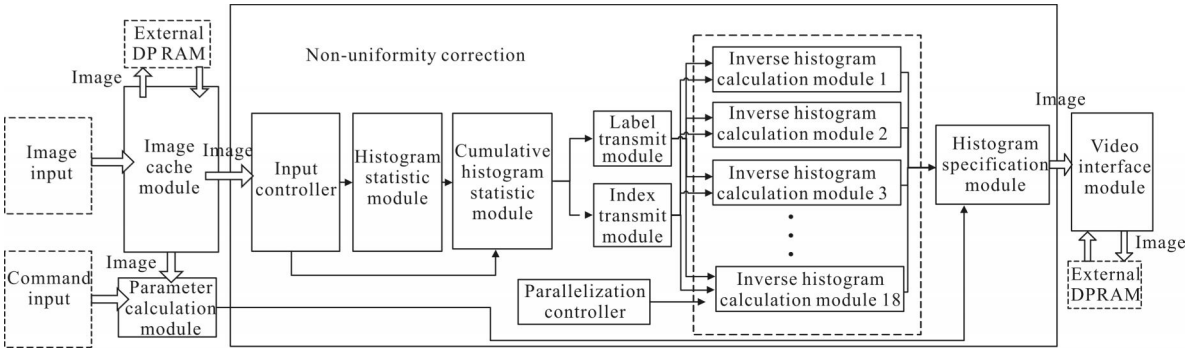
。 FIFO ，

， ， FIFO， FIFO



1

Fig.1 Architecture of the IRFPA stripe non-uniformity system

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$\tilde{I}_{i,j}(k)$;

;

$\tilde{I}_{i,j}(k)$,

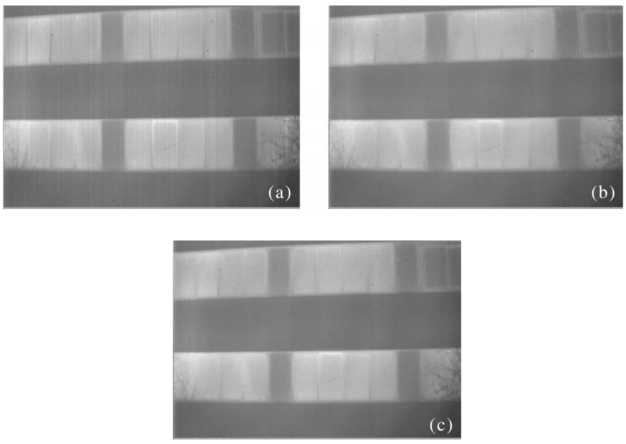
。

3 渝鑍攧羰

Altera EP4CE75 , 640×480, 8。

,

2 。 2(a) ;(b) MIRE ;(c) (N=7, σ=5.6)。



2

Fig.2 Effect of proposed algorithms for IRFPA

, $\rho(f)$[10]

, :

$$\rho(f)=\frac{\| h_1 * f \|_1 + \| h_2 * f \|_1}{\| f \|_1}$$

:f ; h_1=[1, −1] ; $h_2=h_1^T$; * ; $\| \ \|_1$ L_1 。 1 ,

,

50%, 。 ,

, (RMSE)[3]

, ,

瑫 1 躐畝锝陽惏愉埭榮肸瑫

Tab.1 Correction performance comparison using roughness

	Roughness $\rho(f)$
Image with stripe non-uniformity	0.079 28
Result of MIRE method	0.039 56
Result of proposed system	0.039 62

, :

$$\mathrm{RMSE}(\mathrm{Im}_1, \mathrm{Im}_2)=\sqrt{\frac{\sum_{i=1}^{row}\sum_{j=1}^{col}(\mathrm{Im}_1(i,j)-\mathrm{Im}_2(i,j))^2}{row\times col}}$$

:Im_1 ;Im_2 ;row col 。

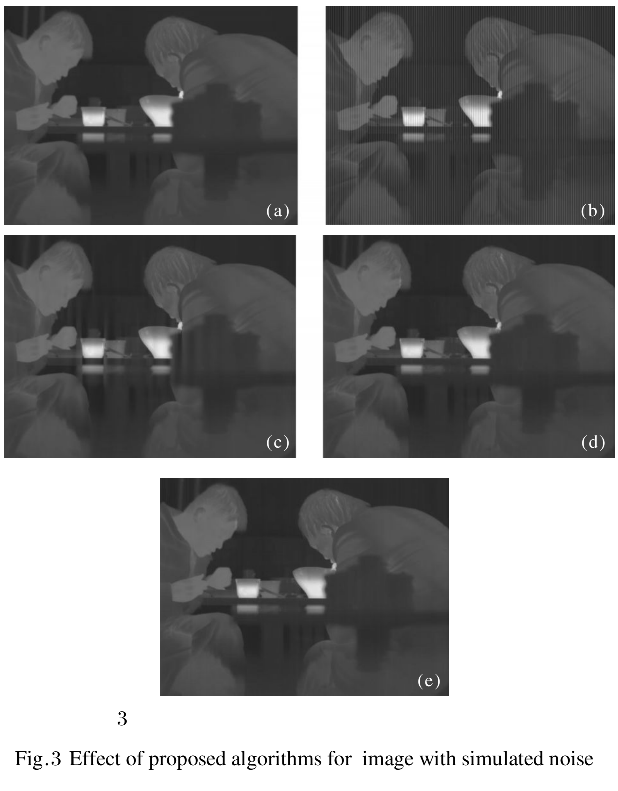
Im_{og}(3(a))

Im_n(3(b)), (2(a))

。

, Im_{dn}, $\mathrm{RMSE}(\mathrm{Im}_{og},\mathrm{Im}_n)$ $\mathrm{RMSE}(\mathrm{im}_{og},\mathrm{Im}_{dn})$, 2 。 3(c) CWFT ; 3(d) MIRE ; 3(e) (N=7, σ=3)。

, RMSE 19.923 4 1.893 4, 1.860 1 。



3

Fig.3 Effect of proposed algorithms for image with simulated noise

瑙 2 躐畝锝陽 RMSE 榮胚瑙

Tab.2 Correction performance comparison using RMSE

	RMSE
Image with stripe non-uniformity	19.923 4
Result of CWFT method	2.424 4
Result of MIRE method	1.860 1
Result of proposed system	1.893 4

139 MHz，

120 MHz，

3 。

瑙 3 姍惫渝偃 - 瞭惫梯冇嵇疆遭榮瑙

Tab.3 Speed in software versus hardware

	Altera EP4CE75F29I7 System freq：120 MHz	Visual C++ 2010 OS：Windows 7 64 bit CPU：Core i7-4700MQ 2.40 GHz(use one thread only)
Resolution	640×480	640×480
Speed	2.65 ms	4 743 ms

。FPGA 4 。

瑙 4 FPGA 籀慳蹭岔犴告瑙(版禿肤 MIRE 梯冇華权嚜籀慳諄髀)

Tab.4 FPGA resources utilization (MIRE processing module only)

	Resources utilization
Logic elements	2938(4%)
Total combinational functions	2740(4%)
Dedicated logic registers	1631(2%)
Total memory bits	111104(4%)
DSP 9×9	18(5%)

：MIRE

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FPGA ， 。

4 擫 祚

FPGA ， FPGA

MIRE ，

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