Quantitative Study of High Dynamic Range Sigma Delta-based Focal Plane Array Architectures

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ABSTRACT

The paper investigates the suitability of $\Sigma\Delta$ modulation based FPA readout schemes for use in Vertically Interconnected Sensor Arrays requiring ultra high dynamic range and frame rate. It is shown that the extended counting scheme is capable of achieving the DR and frame rate requirements but at the expense of high power consumption. Extended counting is also shown to outperform several other HDR schemes in terms of SNR at the ultra high DR and frame rate.

Keywords: IR focal plane array, ROIC, high dynamic range, vertical integration, sigma-delta, extended counting

1. INTRODUCTION

Several methods for extending focal-plane-array (FPA) dynamic range have been developed in recent years.[1–3] In [4], a methodology for comparing these schemes based on their SNR was proposed. Using idealized readout circuit models, this methodology was used in the paper and in a subsequent tutorial[5] to compare several HDR schemes. Motivated by the advent of vertical integration, a recent paper[6] investigated four high fidelity, HDR schemes, namely, time-to-saturation, multiple-capture, asynchronous self-reset with multiple capture, and synchronous self-reset with residue readout. The schemes were again compared based on their SNR, but assuming more realistic circuit models. Implementation and power consumption issues were also discussed.

In this paper we extend our earlier work to study $\Sigma\Delta$ modulation based FPA readout.[2,3,7] This extension is motivated by the ultra high dynamic range (120dB or more) and high frame rate (up to 1000 frames/sec) requirements of the Vertically Interconnected Sensor Array project.[8] We first show that $\Sigma\Delta$ modulation based schemes such as first-order[7] and sampled free-running oscillator[2] extend dynamic range at the high end, but at the expense of reduction in dynamic range at the low end. We then investigate the extended counting scheme introduced in [9]. We show that it is capable of achieving ultra-high DR at high frame rate with acceptable fidelity, but at the expense of high power consumption.

In the next section we provide the background needed. In Section 3, we discuss the $\Sigma\Delta$ based schemes. In Section 4, we compare the extended counting scheme to the schemes discussed in [6] based on their SNR assuming the aforementioned ultra-high dynamic range and high frame rate requirements.

2. BACKGROUND AND PREVIOUS WORK

To be self contained, we repeat here some of the background on the operation of conventional sensors, DR and SNR definitions, and the general readout architecture model for HDR schemes appeared in [6].

Background: Each photodiode in a conventional image sensor converts photon flux into photocurrent i_{ph}. Since this process is linear, i_{ph} is a good measure of the incident photon flux. The resulting photocurrent is typically too small to measure directly, and thus it is integrated into charge. After integration time t_{int}, the charge is converted linearly to a voltage and subsequently digitized and read out. Dark current and additive noise corrupt the output signal charge. Ignoring dark current, noise can be expressed as the sum of four independent components: (i) integrated shot noise, which has zero mean and average power $i_{ph}t_{int}/q$ electron^2, where q is the electron charge, (ii) reset (kTC) noise, (iii) readout circuit noise (including quantization noise) with zero mean and average power $\sigma^2_{\text{Readout}}$, and (iv) offset and gain FPN due to photodetector and device mismatches.

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The output charge from a pixel can thus be expressed as

$$Q(t_{\text{int}}) = \frac{1}{q}(i_{ph}t_{\text{int}} + Q_{\text{Shot}} + Q_{\text{Reset}} + Q_{\text{Readout}} + Q_{\text{FPN}}) \text{ electron,}$$

provided $Q(t_{\text{int}}) \leq Q_{\text{max}}$, the saturation charge, also referred to as *well capacity.*

Assuming that correlated-double-sampling (CDS) is performed, we can eliminate Q_{Reset} and the offset part of Q_{FPN}. If we also assume that gain FPN is negligible compared to shot noise, SNR is given by

$$\text{SNR}(i_{ph}) = \frac{(i_{ph}t_{\text{int}})^2}{qi_{ph}t_{\text{int}} + q^2\sigma_{\text{Readout}}^2}, \quad \text{for } i_{ph} \leq \frac{qQ_{\text{max}}}{t_{\text{int}}}.$$

Note that SNR increases with i_{ph}, first at 20dB per decade when readout noise variance dominates, and then at 10dB per decade when shot noise variance dominates. SNR also increases with t_{int}. Thus it is always preferred to have the longest possible exposure time. Saturation and change in photocurrent due to motion, however, makes it impractical to make integration time too long.

Image sensor DR is defined as the ratio of the largest nonsaturating photocurrent to the smallest detectable photocurrent, typically defined as the standard deviation of the noise under dark conditions. Assuming the above sensor model, $i_{\text{max}} = qQ_{\text{max}}/t_{\text{int}}$ and $i_{\text{min}} = q\sigma_{\text{Readout}}/t_{\text{int}}$ and dynamic range is given by

$$\text{DR} = \frac{i_{\text{max}}}{i_{\text{min}}} = \frac{Q_{\text{max}}}{\sigma_{\text{Readout}}}.$$

Readout Architecture Model: To unify the analysis of the high dynamic range schemes, we use the conceptual sensor readout architecture proposed in [6] shown in Figure 1. It comprises a current modulator that converts i_{ph} into a waveform $s(t)$ and possibly a discrete (in time and value) sequence. The waveform $s(t)$ is then digitized by an ADC at one or more time instances and the output is filtered to produce an estimate of i_{ph}. The modulator is typically implemented per pixel, while the ADC and filter are implemented per group of neighboring pixels. Since the overall system attempts to reproduce the signal i_{ph}, it has unity gain. Thus we can refer the noise to the output when computing the system SNR.
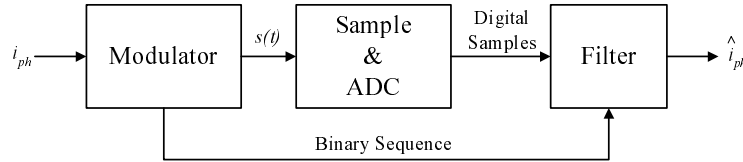

Figure 1. General block diagram.

For a conventional image sensor, the modulator is simply an integrator that saturates when the integrated charge exceeds the well capacity Q_{max}. The output of the modulator is sampled at $t = 0$ (for CDS) and $t = t_{\text{int}}$. The ADC/filter perform the subtraction for CDS, scaling, and digitization.

Reference Sensor: As in [6], we use an optimized conventional sensor, which we refer to as a *reference sensor* for comparison. We denote its average readout noise power as $\sigma_{\text{Readout−Ref}}^2$, its minimum nonsaturating current as $i_{\text{min−Ref}}$, and its DR as the *reference DR*. We assume that $\sigma_{\text{Readout−Ref}}^2$ is not limited by quantization noise and that analog readout circuit noise is minimized, and therefore $\sigma_{\text{Readout−Ref}}^2$ and $i_{\text{min−Ref}}$ are at their practical minimums (for a given t_{int}). We also assume that gain FPN can be ignored within the reference DR.

3. EXTENDED COUNTING $\Sigma\Delta$

We first discuss the first order $\Sigma\Delta$ readout scheme and its variations. In Subsection 3.2, we analyze the extended counting scheme.

3.1. First Order Incremental $\Sigma\Delta$

The block diagram of the first order single-bit $\Sigma\Delta$[7] is shown in Figure 2. At each clock cycle, the integrator output $v(t)$ is compared to the threshold value $V_{\max}/2$. If the comparator flips, $V_{\max}/2$ is subtracted off $v(t)$, thus preventing saturation of the integrator. The subtraction is typically implemented using a switched capacitor circuit. A filter, which can be as simple as a counter, is used to estimate the photocurrent from the binary comparator output sequence. In *incremental* $\Sigma\Delta$,[10] the integrator is reset at the beginning of each frame. Such resetting improves SNR,[11] because, unlike the free-running case, the integrator value at the beginning of each frame is known *. We, therefore, focus on incremental $\Sigma\Delta$.
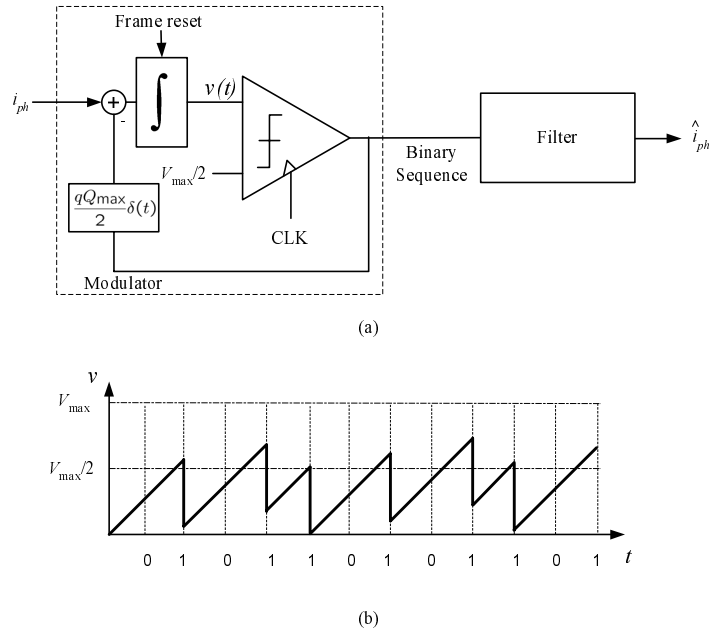

(a)

(b)

Figure 2. Single-bit $\Sigma\Delta$ block diagram.

To quantify the SNR and DR achieved by incremental $\Sigma\Delta$, we use the equivalent integrator output ramp shown in Figure 3. Note that the output sequence from the $\Sigma\Delta$ modulator is identical to the sequence generated by comparing the equivalent ramp to the cumulative sum of the sequence, scaled by and biased by $V_{\max}/2$.

Assuming that a counter is used for decimation, then at the end of integration time, the counter value is

$$n_{\mathrm{counter}}(i_{ph}) = \lfloor 2i_{ph}t_{\mathrm{int}}/CV_{\max} \rfloor.$$

Now, assuming that the $V_{\max}/4$ bias in the counter readout is compensated for, and that quantization noise is signal independent and uncorrelated with other noise sources, the standard deviation of the effective readout noise is approximately given by

$$\sigma_{\mathrm{Readout-eff}} = \sqrt{\frac{(CV_{\max})^2}{48q^2} + n_{\mathrm{counter}}(i_{ph})\sigma_{\mathrm{Switch}}^2 + \sigma_{\mathrm{Reset}}^2},$$

where, σ_{Switch} is the noise due to charge subtraction and σ_{Reset} is the reset noise. The first term in $\sigma_{\mathrm{Readout-eff}}$ corresponds to quantization noise $\Delta^2/12$ with $\Delta = V_{\max}/2$. Therefore, the minimum detectable signal is given by

$$i_{\min} = q\sigma_{\mathrm{Readout-eff}}/t_{\mathrm{int}} \approx CV_{\max}/4\sqrt{3}t_{\mathrm{int}}.$$

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*In smart temperature sensors, the incremental architecture is also used for the same reason.[12]
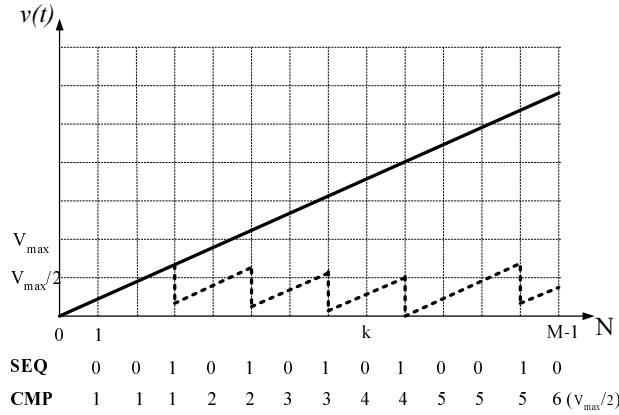
Figure 3. Equivalence of $\Sigma\Delta$ output sequence (SEQ) to the sequence obtained by comparing the equivalent ramp (solid line) to the cumulative sum (CMP) of the sequence scaled and biased by $V_{\mathrm{max}}/2$.

Now from Figure 3, the maximum non-saturating signal is given by

$$i_{\mathrm{max}} = CV_{\mathrm{max}}/2t_{\mathrm{clk}}.$$

Therefore, the maximum achievable dynamic range for a given t_{int} is given by

$$\mathrm{DR} = \frac{2\sqrt{3}t_{\mathrm{int}}}{t_{\mathrm{clk}}}.$$

In order to derive SNR, we need to consider the variation in charge subtraction, which translates into gain FPN. Denoting the standard deviation of charge subtraction by σ_{Offset}, we obtain

$$\mathrm{SNR}(i_{ph}) = \frac{(i_{ph}t_{\mathrm{int}})^2}{qi_{ph}t_{\mathrm{int}} + (q\sigma_{\mathrm{Readout-eff}})^2 + (n_{\mathrm{counter}}q\sigma_{\mathrm{Offset}})^2}.$$

Figure 4 plots SNR versus i_{ph} and compares it with SNR of the reference sensor. Note that with the same Q_{max} and t_{int} the DR of this scheme is shifted to the right with respect to the reference sensor DR, that is, this scheme has very poor low signal performance. Also note that SNR at the low end is quantization limited, whereas at the high end, it becomes gain FPN limited. The reason for the SNR degradation at the low end is the coarseness of the single-bit quantization and the filter used.

Reducing the size of the integrating capacitor or lowering V_{max} may improve low end performance. However, these solutions increase σ_{Offset}, which would degrade SNR at the high end. SNR at the low end can also be improved by using more sophisticated filters such as triangular, zoomer,[13] recursive,[14] optimal,[15] etc. To demonstrate the extent of possible SNR improvement, in Figure 5 we compare the performance using a counter to that using the optimal filter.[15] Note that substantial improvement in SNR is possible, but at the expense of higher circuit complexity and power consumption.

As discussed, SNR at the high end is limited by the gain FPN due to variation in charge subtraction. The sampled free-running oscillator architecture introduced in [2] eliminates charge subtraction (see Figure 6). As shown in the figure, the integrated photocurrent value $v(t)$ is compared to V_{max}. When the comparator flips the integrator is reset and a pulse with period $\geq t_{\mathrm{clk}}$ is produced by the monostable. The binary sequence generated by sampling v_{mon} is then filtered to estimate the photocurrent. It can be shown that in the ideal case, this scheme produces a binary sequence that is identical to a single-bit $\Sigma\Delta$ with twice the well capacity. Even though this scheme eliminates charge subtraction, it suffers from larger σ_{Offset} due to sensitivity to comparator offset.

The extended counting scheme we discuss in the following section solves the coarse quantization problem of the single-bit $\Sigma\Delta$ schemes by quantizing the residue at the end of integration, $v(t_{\mathrm{int}})$, using a multi-bit ADC.
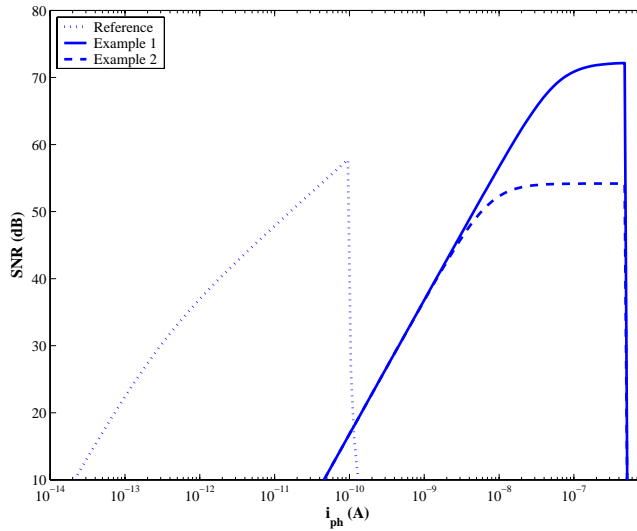
Figure 4. SNR versus i_{ph} for single-bit $\Sigma\Delta$. The reference assumes $Q_{\max} = 625,000e-$, $t_{\text{int}} = 1msec$, $t_{\text{clk}} = 0.1\mu sec$, $\sigma_{\text{Readout}} = 40e-$, $\sigma_{\text{Switch}} = 127e-$ and achieves DR= 83dB. Example 1 assumes $\sigma_{\text{Offset}} = 76e-$ and achieves DR= 80dB. Example 2 assumes $\sigma_{\text{Offset}} = 610e-$ and achieves DR= 80dB.
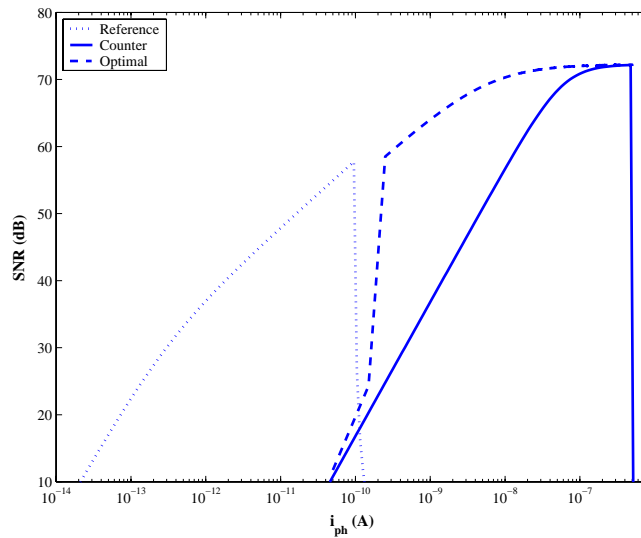

Figure 5. SNR versus i_{ph} for single-bit $\Sigma\Delta$ with counter and optimal filter. The reference assumes $Q_{\max} = 625,000e-$, $t_{\text{int}} = 1msec$, $\sigma_{\text{Readout}} = 40e-$ and achieves DR= 83dB. $\Sigma\Delta$ examples assume $Q_{\max} = 625,000e-$, $t_{\text{int}} = 1msec$, $t_{\text{clk}} = 0.1\mu sec$, $\sigma_{\text{Offset}} = 76e-$, $\sigma_{\text{Switch}} = 127e-$ and achieves DR= 80dB.
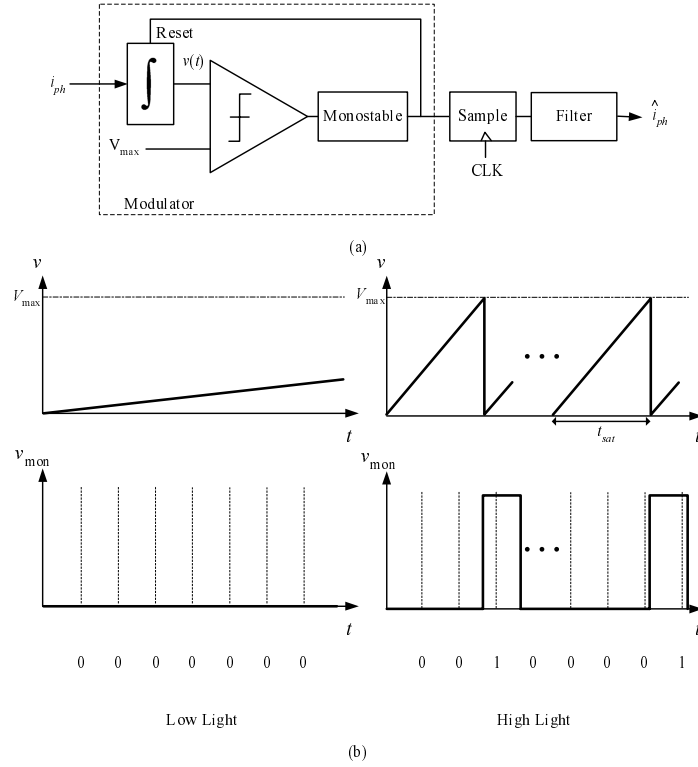
Figure 6. Sampled free-running oscillator block diagram.

3.2. Extending Counting

A block diagram of the extended counting scheme[3] is shown in Figure 7. Except for the additional residue ADC step, the architecture is identical to the single-bit $\Sigma\Delta$ architecture with a counter, discussed in the previous section.

The counter value at the end of the integration time and the digitized residue are combined to estimate the photocurrent as

$$\hat{i}_{ph} = \frac{qQ_{\max}}{t_{\text{int}}} \left(\frac{1}{2} n_{\text{counter}} + \frac{v(t_{\text{int}})}{V_{\max}} \right).$$

In order to calculate DR and SNR, we note that the standard deviation of the effective readout noise is given by

$$\sigma_{\text{Readout−eff}} = \sqrt{\sigma_{\text{ADC−Readout}}^2 + n_{\text{counter}}(i_{ph})\sigma_{\text{Switch}}^2 + \sigma_{\text{Reset}}^2},$$

where, $\sigma_{\text{ADC−Readout}}$ is the quantization noise, σ_{Switch} is the switched capacitor noise due to charge subtraction, σ_{Reset} is the reset noise and $n_{\text{counter}}(i_{ph})$ is the counter output at the end of t_{int}. Thus, the minimum detectable and maximum non-saturating signals are

$$i_{\min} = q\sigma_{\text{Readout−eff}}/t_{\text{int}} = q\sqrt{\sigma_{\text{ADC−Readout}}^2 + \sigma_{\text{Reset}}^2}/t_{\text{int}}, \text{ and}$$

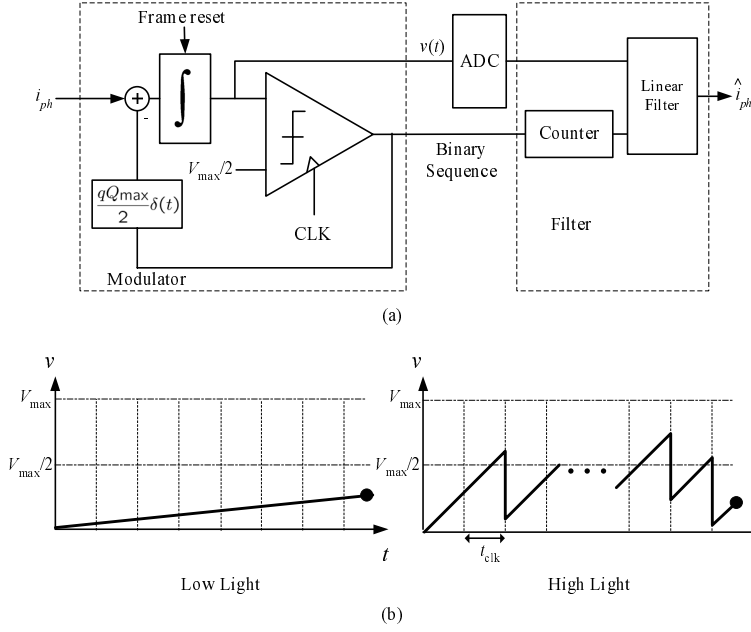$$i_{\max} = CV_{\max}/2t_{\text{clk}}.$$

Figure 7. Extended counting block diagram.

Therefore, the maximum achievable dynamic range for a given t_{int} is given by

$$\text{DR} = \frac{Q_{\max} t_{\text{int}}}{2\sqrt{\sigma_{\text{ADC}-\text{Readout}}^2 + \sigma_{\text{Reset}}^2 t_{\text{clk}}}}.$$

In order to derive SNR, note that any variation of charge subtraction, σ_{Offset} will translate to gain fixed pattern noise. Thus SNR is given by

$$\text{SNR}(i_{ph}) = \frac{(i_{ph} t_{\text{int}})^2}{q i_{ph} t_{\text{int}} + (q\sigma_{\text{Readout}})^2 + (n_{\text{counter}} q\sigma_{\text{Offset}})^2}.$$

SNR is plotted versus signal in Figure 8.

Remarks:

(i) DR at the low end is improved over the single-bit $\Sigma\Delta$ using the residue digitization, which reduces $\sigma_{\text{Readout}-\text{eff}}$. However, $\sigma_{\text{Readout}-\text{eff}}$ is larger than the readout noise of the reference sensor $\sigma_{\text{Readout}-\text{Ref}}$ because CDS cannot be performed in this architecture.

(ii) DR at the high end is directly related to t_{clk} and $Q_{\max}$. To avoid saturation during charge subtraction caused by comparator and charge subtraction offsets, one needs to set the comparison voltage higher than $V_{\max}/2$, which reduces DR at the high end.

(iii) DR can be increased by reducing t_{clk}. To understand the impact of increasing clock speed, consider the typical integrator/ charge subtraction implementation using capacitive transimpedance amplifier (CTIA) and switched capacitor shown in Figure 9. Note that decreasing t_{clk} requires reducing the amplifier time-constant, because for a given SNR the charge subtraction circuit settling time dictates the required gain bandwidth product. As a result, amplifier power consumption increases. Thus, assuming the MOS square-law, amplifier power needs to increase as the square of the factor of increase in DR.
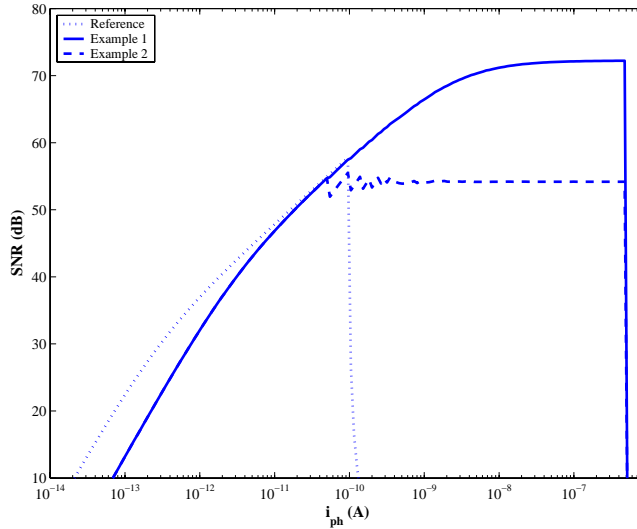
Figure 8. SNR versus i_{ph} for extended-counting. The reference assumes $Q_{max} = 625,000e-$, $t_{int} = 1msec$, $t_{clk} = 0.1\mu sec$, $\sigma_{Readout} = 40e-$, $\sigma_{Switch} = 127e-$ and achieves DR= 83dB. Example 1 assumes $\sigma_{Offset} = 76e-$ and achieves DR= 154dB. Example 2 assumes $\sigma_{Offset} = 610e-$ and achieves DR= 154dB.

Note that the maximum current of the switch in Figure 9 must be controlled to avoid large changes in the detector bias. Controlling the switch current and satisfying the settling time requirement makes it necessary to increase the required amplifier bias.
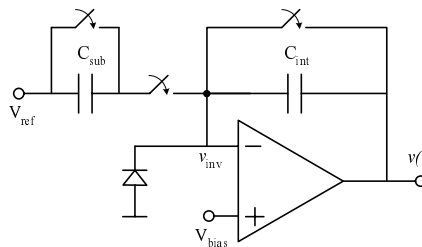

Figure 9. Schematic of the integrator and the subtraction mechanism (digital-to-analog-converter) in each pixel.

(iv) SNR in the extended range is limited by σ_{Offset}, which is mainly due to (a) mismatch[16] in the integrating and subtracting capacitors shown in Figure 9, (b) variation in the pedestal error caused by switching (also mismatch if dummy switches are used), (c) variation in V_{ref} routed to all pixels, (d) variation in the settling time of the switched capacitor, and (e) finite dc gain of the amplifiers.

(v) The dominant source of power consumption in this scheme is the CTIA.

4. COMPARISON OF HDR SCHEMES

In this section we compare the extended counting scheme to the four schemes discussed in [6] for very high dynamic range (120 dB) and high speed (1000 frames/sec) applications. We assume that vertical integration is used in the implementation of these schemes, since it would be difficult if not impossible to achieve the desired DR and frame rate using planar technologies with reasonable size pixels. Vertical integration enables the integration of more circuits at the each pixel, reducing noise coupling and device mismatch, and eliminating the column readout speed and power dissipation bottlenecks.

Block diagrams of the four schemes discussed in [6] are depicted in Figure 10. Even with vertical integration, the only two schemes that can achieve the desired high dynamic range and high speed are synchronous self-reset with residue readout and extended counting. As discussed in [6], synchronous self-reset suffers from low SNR at both the high and low ends of DR. At the high end, it suffers from the underestimation of charge and large gain FPN due to comparator and self-reset offsets. Extended counting does not suffer from charge underestimation and has lower gain FPN, and as a result it performs better at the high end. At the low end, synchronous self-reset and extended counting perform exactly the same. Both schemes underperform the reference sensor due to the fact that reset noise cannot be cancelled.
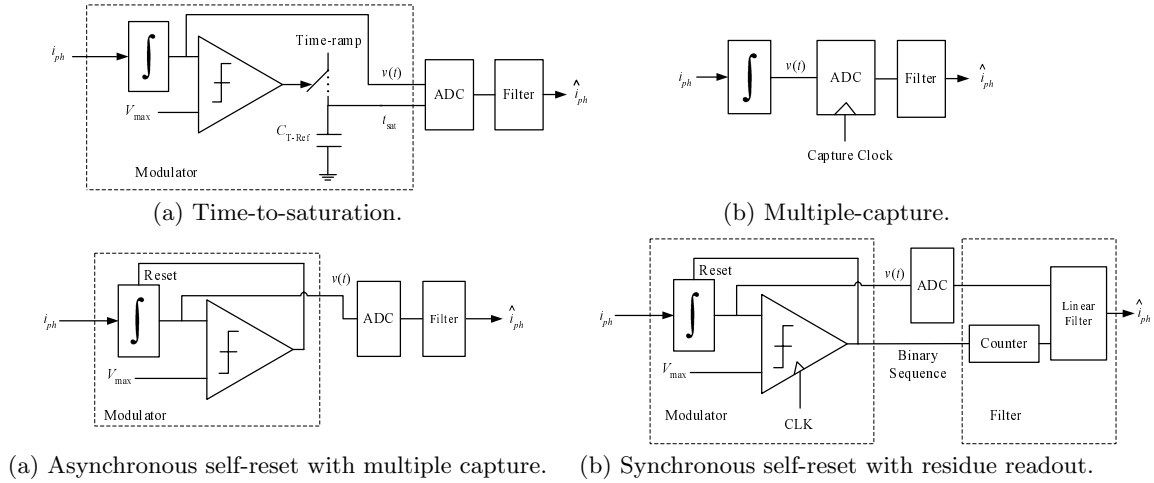

(a) Time-to-saturation.

(b) Multiple-capture.

(a) Asynchronous self-reset with multiple capture.

(b) Synchronous self-reset with residue readout.

Figure 10. Block diagram of all of the studied architectures in the previous work.

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