A 0.18μm CMOS 1000 frames/sec, 138dB Dynamic Range Readout Circuit for 3D-IC IR Focal Plane Arrays

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***Abstract*— A prototype of a new high dynamic range readout scheme targeted for 3D-IC IR focal plane arrays is described. Dynamic range is extended using synchronous self-reset while high SNR is maintained using few non-uniformly spaced captures and least-squares fit to estimate pixel photocurrent. The prototype comprises of a 16×5 readout pixel array fabricated in a 0.18μm CMOS process and achieves 138dB dynamic range and 60dB peak SNR at 1000 frames/sec with energy consumption of 25.5nJ per pixel readout.**

I. INTRODUCTION

Infrared (IR) imaging has recently been finding a growing range of applications in the tactical, industrial, scientific, medical, and automotive arenas. These applications often require imaging of scenes with large intrascene variations in irradiance, due to object temperatures, and imaging systems that can tolerate undesirable scene disturbances, for example, due to sun reflection or laser jamming. The imaging systems must also have highly linear, shot noise limited readout in order to achieve acceptable sensitivity (measured in terms of SNR or Noise Equivalent Temperature Difference (NETD) [1]). Further, in the presence of rapid object motion, the systems must operate at high frame rates to allow for image registration before frame averaging. In [2], it is argued that low power IR focal plane arrays (FPAs) with $>$ 120dB dynamic range and 60dB SNR operating at 1000 frames/sec are needed for such applications. These performance requirements are far more aggressive than is achievable with present-day IR FPAs.

Several high dynamic range (HDR) extension schemes have been recently developed for visible range imaging applications, e.g., [3]–[8]. While these schemes require pixels that are too large to be practical for many visible range imaging applications, they are better suited to IR FPAs where pixel sizes are inherently larger due to the longer wavelengths and the use of bump-bonded detectors, e.g., [9]. Moreover, with the advent of 3D-IC technology whereby multiple wafers can be stacked and vertically interconnected, the effective pixel area available to implement these schemes is increased [2]. However, as discussed in [10], [11], none of the existing HDR schemes can meet the aforementioned IR FPA performance requirements. In [12], a HDR extension scheme denoted by Folded Multiple

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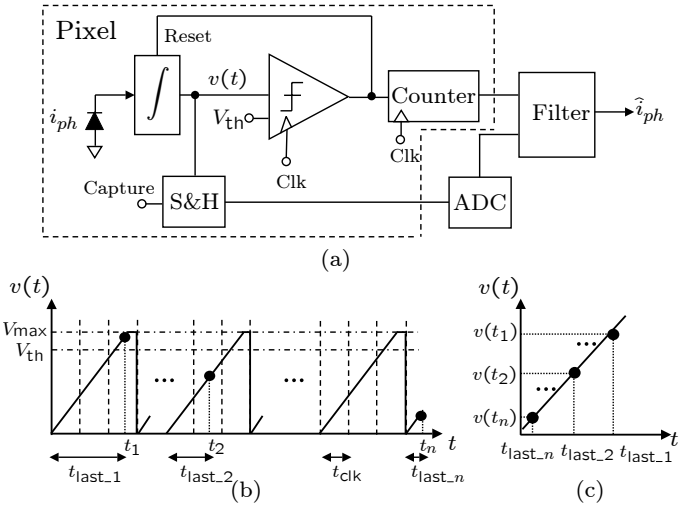


Fig. 1. Above: FMC architecture. Below: FMC operation.

Capture (FMC) that can achieve all the requirements stated in [2] is presented. Low power consumption is achieved while maintaining high SNR by using digital signal processing to relax the demands on the analog front-end (AFE). FMC also provides tolerance to disturbances in the scene that generate large transient spikes of photocurrent. The FMC architecture leverages 3D-IC technology to enable implementation of the fully integrated imaging system.

In this paper we describe the design and characterization of a 16×5 FMC readout pixel array prototype implemented in a 0.18μm CMOS technology. To be self contained, in the following section we describe the architecture and operation of FMC. Section III discusses design and implementation of the prototype and we present experimental results in Section IV.

II. FMC ARCHITECTURE AND OPERATION

A block diagram of the FMC architecture is shown in Fig. 1(a). Each pixel consists of an integrator, with reset that is controlled by a comparator, a counter, and a sample-and-hold (S&H). The S&H output is digitized by a fine ADC, whose output along with the counter values are fed to a filter that generates the photocurrent estimate. At each clock cycle, the integrated photocurrent, $v(t)$, is compared to a threshold voltage V_{th}. The integrator is reset when the comparator output flips creating the folded waveform shown in Fig. 1(b). Meanwhile, the integrator output is sampled and digitized at predefined sampling or capture times $t_1, t_2, \ldots, t_n$.

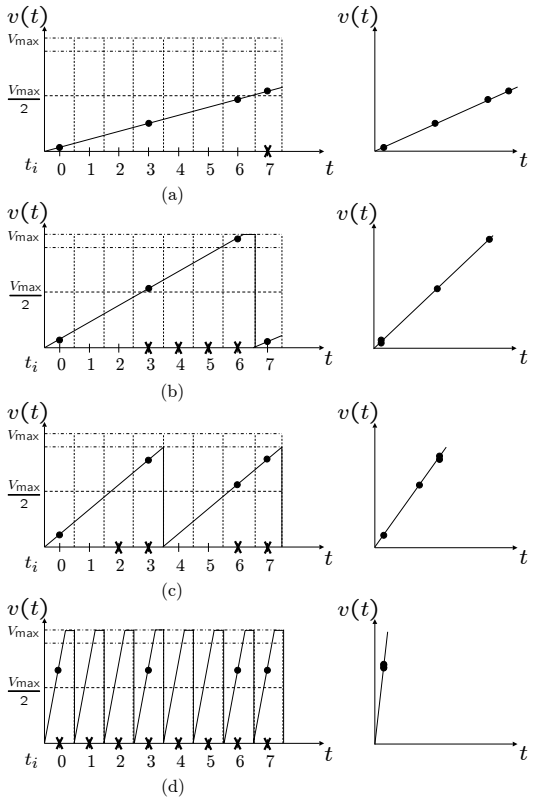


Fig. 2. Integrator output (left) and corresponding least-squares estimate (right) for four photocurrent values with capture times, $(t_1, t_2, t_3, t_4) = (0, 3, 6, 7)t_{\rm Clk}$. The $\times$ indicate capture times that satisfy $Q_{\rm int} > Q_{\rm max}/2$.

The capture times are synchronized with Clk, shifted by $t_{\rm Clk}/2$ to avoid simultaneous reset and capture. The counter is incremented by the clock and reset by the comparator output signal. Its value, which corresponds to the *effective integration time* $t_{\rm last\_i}$ (the time from the last reset), is read out at each capture time. The slope of the linear least-squares fit of the digitized capture values and their corresponding integration times is used to estimate the photocurrent (see Fig. 1(c)). In effect, FMC performs n regular captures during an exposure time and combines them to achieve a high fidelity estimate of the photocurrent. Dynamic range is extended by $2t_{\rm int}/t_{\rm Clk}$ over the integrating capacitor dynamic range. For example, for $t_{\rm int}/t_{\rm Clk} = 1000$, DR increases by 66dB. Fig. 2 shows example waveforms for $t_{\rm int}/t_{\rm Clk} = 8$ and four capture times. A low input photocurrent (see Fig. 2(a)) results in no reset and the scheme reduces to a conventional FPA with Fowler readout [13]. A high photocurrent (see Fig. 2(c, d)) results in periodic reset. Unlike other self-reset schemes [10], however, the number of resets is not used to estimate the signal.

For low power, the number of captures used in achieving the high fidelity estimate of the photocurrent must be small. A surprising fact about FMC is that only 3 to 4 scene-independent globally set captures are needed to achieve uniformly high SNR. For a single capture, assuming shot noise limited FPA operation, SNR $\approx Q_{\rm int}$, where $Q_{\rm int}$ is the integrated charge in electrons. We wish to select capture times to guarantee a minimum SNR of $Q_{\rm max}/2$, for photocurrents $\geq qQ_{\rm max}/t_{\rm int}$, where $Q_{\rm max}$ is the well capacity in electrons. Note that a single capture only guarantees this requirement for a certain range of photocurrents. To illustrate this point, consider the example in Fig. 2 again. A capture at $t_4 = 7t_{\rm Clk}$ satisfies the above SNR condition for the examples in Fig. 2(a),(c),(d). However, using only this capture results in SNR ≈ 0 for example (b). The problem is solved by using another capture, e.g., between $3t_{\rm Clk} \leq t_3 \leq 6t_{\rm Clk}$. It can be shown that capture times $(t_2, t_3, t_4) = (3, 6, 7)t_{\rm Clk}$ for $t_{\rm int}/t_{\rm Clk} = 8$ ensure that for all photocurrent values, at least one of the capture values has a value higher than $Q_{\rm max}/2$. To perform offset cancellation, a low value capture, e.g., at $t_1 = 0$, is also required.

The general capture selection problem can be formulated as follows. Given $t_{\rm int}/t_{\rm Clk}$, $Q_{\rm max}$, and $0 < \alpha < 1$, find the smallest number of captures n and their times $t_1, t_2, \ldots, t_n$ such that the minimum SNR $\geq \alpha Q_{\rm max}$ for photocurrents $\geq qQ_{\rm max}/t_{\rm int}$. This is in general a difficult problem because $t_{\rm last\_i}$, and therefore $v(t_i)$, is a non-convex function of t_i and i_{ph}. In [12], this problem is shown to be equivalent to a combinatorial optimization problem. A fast greedy heuristic is developed and it is shown that only few captures are needed. For example, for $t_{\rm int}/t_{\rm Clk} = 1000$ and $\alpha = 0.33$, there are several feasible 3-capture solutions, including $(t_1, t_2, t_3) = (101, 157, 370)t_{\rm Clk}, (143, 334, 818)t_{\rm Clk}$, and for $\alpha = 0.5$ several 4-capture solutions, including $(143, 157, 335, 502)t_{\rm Clk}, (148, 335, 502, 969)t_{\rm Clk}$, exist.

While the above algorithm guarantees minimum SNR of $Q_{\rm max}/2$, least-squares fit of the captures and corresponding effective integration times to estimate photocurrent further improves SNR by cancelling offsets, e.g., due to integrator and readout, and reducing the read, shot, and 1/f noise (see [13]). A smaller integrating capacitor can therefore be used resulting in smaller AFE area. Note that since all signals in FMC are synchronized with a low jitter clock, SNR is not affected by timing inaccuracies. Further area and power reductions are achieved by relaxing the comparator specifications. As discussed in [10], the variation of the reset period with comparator offsets results in fixed pattern noise (FPN) that typically degrades SNR of HDR schemes. Since in FMC reset periods are not used to estimate photocurrent, the associated FPN is avoided and a simple regenerative architecture can be used for the comparator, obviating the need for a larger, power consuming gain stage. A relaxed comparator design also means that the highest clock frequency is not limited by the comparator speed, but by the settling time of the S&H circuit.

III. Implementation

The FMC prototype is implemented in a 0.18μm double-poly, five metal-layer process. A block diagram of the pixel readout circuit is depicted in Fig. 3 and detailed circuit schematics are given in Fig. 4. To maintain compatibility with IR detectors, we use a Capacitive Trans-impedance Amplifier (CTIA) as an integrator. This is effective in minimizing variation in the detector bias voltage thus avoiding signal dependent dark current. The CTIA is implemented using a single stage telescopic cascode amplifier achieving high gain ($\approx$ 69dB) and low noise within a small area. The integrator output is

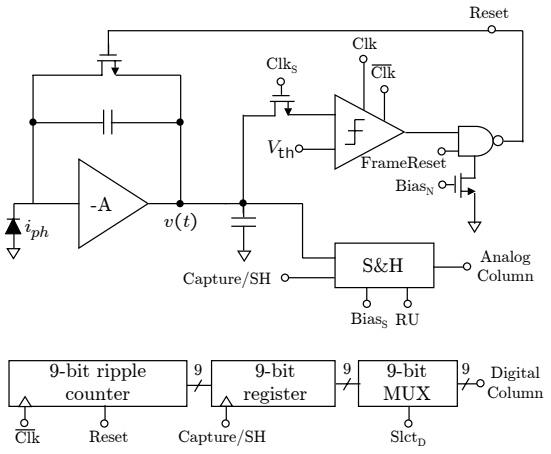


Fig. 3. Pixel block diagram.

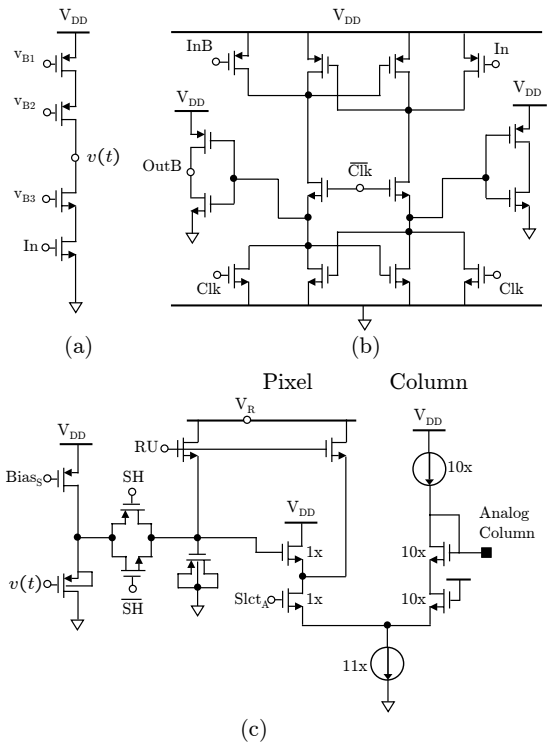


Fig. 4. (a) Amplifier (b) Comparator (c) S&H and column readout.

sampled at the input of the comparator via Clk_S; Clk and $\overline{\text{Clk}}$ control the comparator and the duration of the reset. The comparator is implemented using a regenerative architecture. A slow fall NAND gate is used to reduce the random charge injection on the feedback capacitor. The S&H block consists of a source follower with dynamic bias control followed by the sampling circuit (see Fig. 4(c)) which is followed by column readout circuitry. The S&H bias and size are set to minimize the readout noise and to achieve the required linearity and settling. The column readout circuitry consists of a diff-pair, sized to achieve high linearity, split between the pixel and the column. After readout of a capture value, the S&H capacitor voltage is set high so that charge injection only pulls the $v(t)$ node high. The follower transistor's C_{gs} is also reset to avoid capture to capture cross-talk. All analog circuits operate at

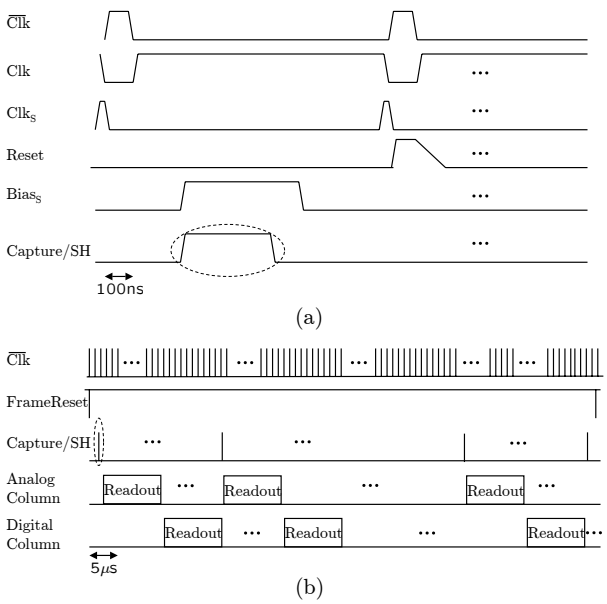


Fig. 5. (a) Comparator and S&H and (b) Chip level timing diagrams.

3.3V. The digital portion of the pixel consists of a 9-bit ripple counter with an output register. All digital circuits operate at 1.8V and a level shifter is used to drive counter reset. Fig. 5(a) shows timing diagrams during a t_{Clk} period for the comparator and S&H operation with a reset immediately after capture. Fig. 5(b) shows the chip level readout timing during one frame. After each capture, the analog capture values and the latched counter values are readout serially from each column off-chip.

The chip micrograph is shown in Fig. 6. Four columns have pixels with NWELL/PSUB diodes and the fifth has pixels driven by external current sources. Provisions have been made for bump-bonding IR detectors adjacent to the diodes. The analog and digital periphery circuits are placed at opposite ends of the pixel array. The Timing Control block generates all control signals. The clock rate (and thus dynamic range) and capture times are programmable via a scan chain. Each pixel occupies an area of $30\mu\text{m} \times 150\mu\text{m}$ (40% analog, 60% digital). The digital section is implemented using standard cells and is readily miniaturized with custom design. Analog area is dominated by the CTIA and S&H to meet the linearity requirement. In a 3D-IC implementation of the fully integrated imaging system [2], each pixel is estimated to be $30\mu\text{m} \times 30\mu\text{m}$ with 2 analog and 1 digital circuit layers.

IV. Experimental Results

A uniform LED illuminator is used as the light source for characterization. The chip analog column outputs, digitized using an on-board ADC, and the chip digital column outputs are transfered to a PC via an FPGA-based data acquisition board. Least-squares fit of the digitized capture values and corresponding effective integration times to estimate photocurrent is then performed in software.

Scatter plots of the readout values for two of the pixels in the array are shown in Fig. 7. Note that in Fig. 7(a) (low light) the counter values are the same as capture times, since no reset occurs, but in Fig. 7(b) (high light) periodic resets

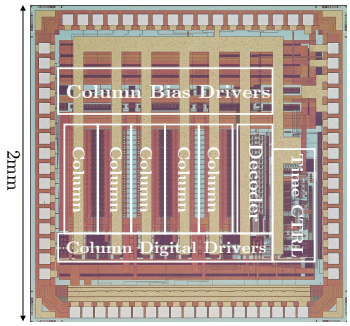
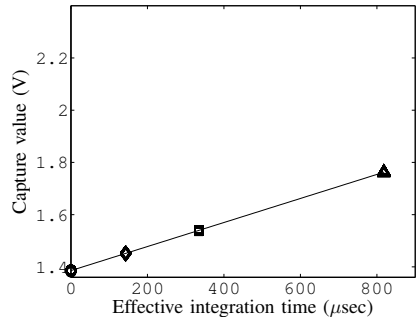
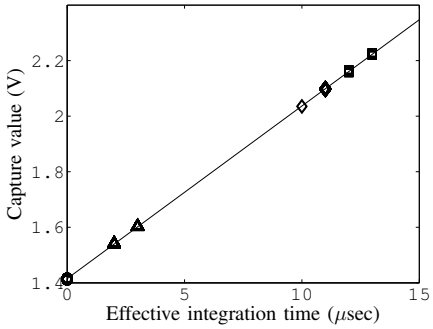


Fig. 6. Chip micrograph.



(a) Pixel with low input photocurrent.



(b) Pixel with high input photocurrent.

Fig. 7. Least-squares photocurrent estimation for two different pixels. The slope corresponds to average photocurrent of the 500 frames shown in the scatter plots. Different captures are denoted by 1: o, 2: ◇, 3: □, 4: △.

occur and the counter values adapt to the input photocurrent. As a result in Fig. 7(b), the third capture value is actually the largest amongst the four captures. Note that the values for captures 2-4 are in two clusters due to the variation in the reset times in different frames as a result of shot and comparator noise. However, this variation has minimal effect on SNR.

Table I summarizes chip characterization results. The linearity and SNR are characterized locally at multiple random intervals. Read noise is expected to be lower with test setup improvements.

The power consumption per pixel is 25.5μW and dominated by the CTIA. This corresponds to energy consumption of 25.5nJ for each pixel readout with DR = 138dB and SNR = 60dB. Note that the CTIA power consumption can be significantly reduced, e.g., using switched biasing, with knowledge of the detector parameters.

TABLE I

PERFORMANCE CHARACTERISTICS

$t_{\rm int}$, $t_{\rm Clk}$	1msec, 1μsec
Capture times used (t_1, t_2, t_3, t_4)	$0, 143, 334, 818\mu$sec
Integrator capacitance	100fF
Integrator voltage swing	1.5V
Frame rate	1000 frames/sec
Dynamic range	138dB
Maximum input current	200nA
System read noise	240μV
Peak SNR	60dB
Linearity	$< 0.1\%$
NETD (estimated for MWIR, F# 2.5)	20mK
Pixel power consumption	25.5μW

V. CONCLUSION

This paper demonstrates the feasibility of a high dynamic range 3D-IC IR FPA readout architecture for high frame rate operation with high SNR and linearity. Digital signal processing is used to achieve the required performance at low power consumption with a small analog-front end area. The readout architecture is also tolerant to undesirable scene disturbances that generate transient spikes of photocurrent.

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