Quantitative Study of High Dynamic Range Image Sensor Architectures

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ABSTRACT

Analysis of dynamic-range (DR) and signal-to-noise-ratio (SNR) for high fidelity, high-dynamic-range (HDR) image sensor architectures is presented. Four architectures are considered: (i) time-to-saturation, (ii) multiple-capture, (iii) asynchronous self-reset with multiple capture, and (iv) synchronous self-reset with residue readout. The analysis takes into account circuit nonidealities such as quantization noise and the effects of limited pixel area on building block and reference signal performance and accuracy. Examples that demonstrate the behavior of SNR in the extended DR and implementation and power consumption issues for each scheme are presented.

Keywords: imagers, CMOS image sensors, high dynamic range, analog front end, ADC

1. INTRODUCTION

Several methods for extending image sensor dynamic range have been developed in recent years .[1–14] In [15], a methodology for comparing such schemes based on their SNR is proposed. The paper uses idealized noise and circuit models to compare well-capacity adjusting to multiple-capture. Similar analysis for logarithmic, local-adaptation, spatially varying exposure and time-to-saturation methods was later presented.[16]

The work in this paper is motivated by the advent of sub-micron CMOS image sensor processes[17] and the promise of 3D integration, where multiple wafers can be stacked and connected using through vias.[18, 19] With these capabilities, more transistors can be integrated in each pixel, enabling the implementation of several high fidelity, HDR schemes. We investigate four such schemes, namely time-to-saturation,[7–9] multiple-capture,[1–3] synchronous self-reset with residue readout[13, 14] and asynchronous self-reset with multiple capture.[4] As in [16], we compare these schemes based on their SNR. To provide meaningful results, given the complexity of the circuits involved, our analysis accounts for circuit nonidealities such as quantization noise and the effects of limited pixel area on building block and reference signal performance and accuracy. In addition to providing analytical formulas and examples of SNR as a function of photocurrent, we briefly discuss the main implementation and power consumption issues for each scheme.

Our analysis and examples show the following:

(i) For time-to-saturation,[7–9] SNR at the high end degrades by limited signal accuracy.

(ii) For multiple-capture,[1–3] SNR does not degrade with dynamic range increase as previously discussed in [15]. However, SNR is limited by the resolution of the per-pixel ADC, which is severely constrained by pixel area and power consumption.

(iii) For synchronous self-reset with residue readout,[13, 14] DR increases at the high end, but at the expense of degradation in SNR.

(iv) For asynchronous self-reset with multiple capture,[4] SNR increases beyond the well capacity limit. However, the increase is limited by gain fixed-pattern-noise (FPN) and DSP complexity.

The rest of the paper is organized as follows. In the next section we introduce the sensor model and definitions of dynamic range and SNR for conventional image sensors and introduce a conceptual model for the HDR architectures. In Sections 3-6 we discuss the four high dynamic range schemes and provide the SNR analysis.

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2. BACKGROUND AND HDR SENSOR MODEL

An image sensor can be viewed as an array of photodetectors followed by circuits for readout. The performance of a sensor is a function of both the photodetector used and its readout circuits. HDR image sensor schemes modify a conventional sensor's readout circuits to improve its DR. Since in this paper we are mainly concerned with comparing the performance of HDR schemes, we focus on analyzing their readout circuits assuming that they all use the same high quality photodetector.

We first briefly review the definitions of SNR and dynamic range for a conventional image sensor such as a CCD or a CMOS APS. We then introduce a model for sensor readout architectures that we use to unify the analysis of the various HDR schemes.

Background: Each photodiode in a conventional image sensor converts incident light into photocurrent i_{ph}. Since this process is linear, i_{ph} is a good measure of incident light intensity. The resulting photocurrent is typically too small to measure directly, and thus it is integrated into charge. After integration time t_{int}, the charge is converted linearly to a voltage and the voltage is digitized and read out. Dark current and additive noise corrupt the output signal charge. Ignoring dark current, noise can be expressed as the sum of four independent components: (i) integrated shot noise, which has zero mean and average power $i_{ph}t_{\text{int}}/q$ electron^2, where q is the electron charge, (ii) reset (kTC) noise, (iii) readout circuit noise (including quantization noise) with zero mean and average power $\sigma^2_{\text{Readout}}$, and (iv) offset and gain FPN due to photodetector and device mismatches.

The output charge from a pixel can thus be expressed as

$$Q(t_{\text{int}}) = \frac{1}{q}(i_{ph}t_{\text{int}} + Q_{\text{Shot}} + Q_{\text{Reset}} + Q_{\text{Readout}} + Q_{\text{FPN}}) \text{ electron},$$

provided $Q(t_{\text{int}}) \leq Q_{\max}$, the saturation charge, also referred to as *well capacity*.

Assuming that correlated-double-sampling (CDS) is performed, we can eliminate Q_{Reset} and the offset part of Q_{FPN}. If we also assume that gain FPN is negligible compared to shot noise, SNR is given by

$$\text{SNR}(i_{ph}) = \frac{(i_{ph}t_{\text{int}})^2}{qi_{ph}t_{\text{int}} + q^2\sigma^2_{\text{Readout}}}, \quad \text{for } i_{ph} \leq \frac{qQ_{\max}}{t_{\text{int}}}.$$

Note that SNR increases with i_{ph}, first at 20dB per decade when readout noise variance dominates, and then at 10dB per decade when shot noise variance dominates. SNR also increases with t_{int}. Thus it is always preferred to have the longest possible exposure time. Saturation and change in photocurrent due to motion, however, makes it impractical to make integration time too long.

Image sensor DR is defined as the ratio of the largest nonsaturating photocurrent to the smallest detectable photocurrent, typically defined as the standard deviation of the noise under dark conditions. Assuming the above sensor model, $i_{\max} = qQ_{\text{sat}}/t_{\text{int}}$ and $i_{\min} = q\sigma_{\text{Readout}}/t_{\text{int}}$ and dynamic range is given by

$$\text{DR} = \frac{i_{\max}}{i_{\min}} = \frac{Q_{\max}}{\sigma_{\text{Readout}}}.$$

Extending dynamic range at the high end requires increasing $i_{\max}$. The techniques we discuss extend DR at the high end in one of the following two ways:

Varying integration time: The integration time is *adapted* to pixel photocurrent providing long integration times for pixels with small photocurrents and short integration times for pixels with high photocurrents. Examples of such techniques are: well-capacity adjusting,[10] time-to-saturation,[7,8] and multiple-capture.[1–3]

Recycling the well: Here $i_{\max}$ is increased by self-resetting[4,13,14] or charge subtraction[12,20] to increase the effective well capacity as will be discussed in Sections 5,6. In theory, such well recycling increases peak SNR. As we show, however, the improvement in peak SNR is limited by several circuit nonidealities and can rapidly drop as DR is increased.

Extending DR at the low end requires reducing $i_{\min}$, which can be achieved by either reducing σ_{Readout} or increasing t_{int}. Except when using multiple-capture, where this can be done by a combination of image blur prevention and weighted averaging of the samples,[21] other HDR schemes only extend DR at the high end.

Readout Architecture Model: To unify the analysis of the high dynamic range schemes, we use the conceptual sensor readout architecture shown in Figure 1. It comprises a current modulator that converts i_{ph} into a waveform $s(t)$ and possibly a discrete (in time and value) sequence. The waveform $s(t)$ is then digitized by an ADC at one or more time instances and the output is filtered to produce an estimate of i_{ph}. The modulator is typically implemented per pixel, while the ADC and filter are implemented per group of neighboring pixels,[1] per column,[22] per chip, or off-chip. Since the overall system attempts to reproduce the signal i_{ph}, it has unity gain. Thus we can refer the noise to the output when computing the system SNR.

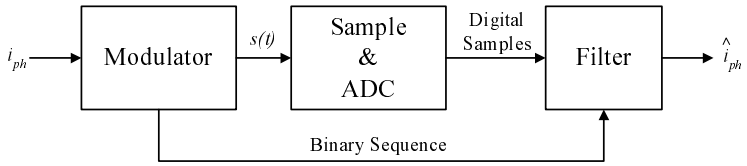

Figure 1. General Block Diagram.

For a conventional image sensor, the modulator is simply an integrator that saturates when the integrated charge exceeds the well capacity $Q_{\max}$. Although in our model the integration is treated as separate from the photodetector, in practice it is typically performed using the photodiode capacitance. The output of the modulator is sampled at $t = 0$ (for CDS) and $t = t_{\text{int}}$. The ADC/filter perform the subtraction for CDS, scaling, and digitization.

Reference Sensor: For comparison purposes, we will use an optimized conventional sensor, which we refer to as a *reference sensor*. We denote its average readout noise power as $\sigma^2_{\text{Readout}-\text{Ref}}$, its minimum nonsaturating current as $i_{\min-\text{Ref}}$, and its DR as the *reference DR*. We assume that $\sigma^2_{\text{Readout}-\text{Ref}}$ is not limited by quantization noise and that analog readout circuit noise is minimized, and therefore $\sigma^2_{\text{Readout}-\text{Ref}}$ and $i_{\min-\text{Ref}}$ are at their practical minimums (for a given t_{int}). We also assume that gain FPN can be ignored within the reference DR. For HDR schemes employing column based or chip based ADCs, we assume that quantization noise can be made as small as needed and therefore $\sigma^2_{\text{Readout}}$ is limited by their analog readout circuit noise. For schemes that use per-pixel ADC, quantization noise cannot be ignored due to the pixel area and power constraints and can be the dominant component of the readout noise. For all schemes we assume that $\sigma^2_{\text{Readout}}$ is not the dominant source of noise at the high end of the photocurrent.

3. TIME-TO-SATURATION

The time-to-saturation scheme[8] attempts to achieve high dynamic range with high SNR by converting each photocurrent i_{ph} into its time-to-saturation $t_{\text{sat}}(i_{ph}) = qQ_{\max}/i_{ph}$. A block diagram of the scheme and plot of the integrator output as a function of time are given in Figure 2 *. After the photodiode and the time reference capacitor $C_{\text{T}-\text{Ref}}$ are reset, the output of the integrator is read out for CDS. Photocurrent is then integrated and converted to voltage, which is compared to a reference $V_{\max}$. Concurrently, $C_{\text{T}-\text{Ref}}$ follows the time-ramp. When the integrator output reaches $V_{\max}$, the comparator flips and $t_{\text{sat}}(i_{ph})$ is stored on $C_{\text{T}-\text{Ref}}$. At the end of integration, $v(t_{\text{int}})$ and t_{sat} are read out. If $t_{\text{sat}} < t_{\text{int}}$, the signal is estimated as $qQ_{\max}/t_{\text{sat}}$, otherwise the signal is estimated using $v(t_{\text{int}})$ only. More details concerning implementation and correction for several nonidealities can be found in.[7,8]

Note that the minimum detectable signal is given by $i_{\min} = q\sigma_{\text{Readout}}/t_{\text{int}}$, which has the same form as that of the conventional sensor. The maximum nonsaturating signal depends on the comparator delay and offset as well as the noise associated with $t_{\text{sat}}(i_{ph})$ due to time-ramp noise, kTC of $C_{\text{T}-\text{Ref}}$, and the readout noise. Let σ_{sat} be

*The implementation in[8] actually uses two time-ramps and two capacitors to reduce σ_{sat}. We account for this indirectly by using small σ_{sat} in the examples.

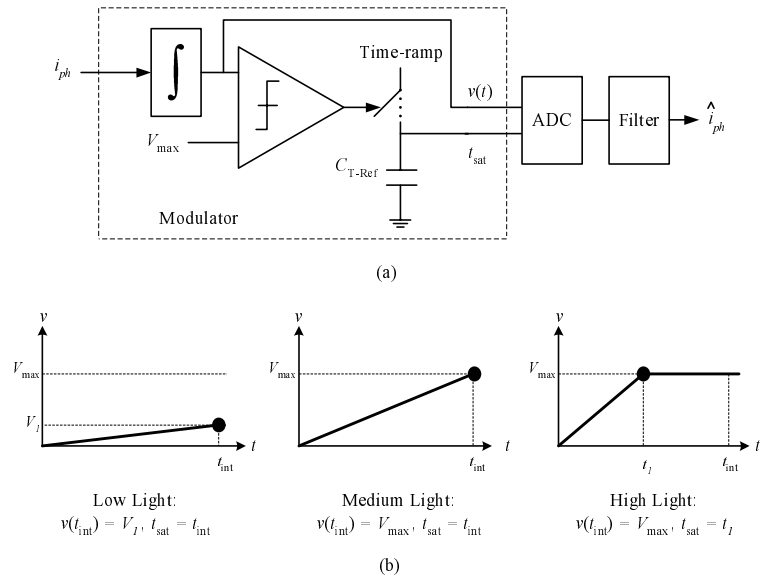

Figure 2. Time-to-saturation scheme.

the total rms of the noise added to $t_{\rm sat}(i_{ph})$, then the maximum detectable signal is given by $i_{\max} = qQ_{\max}/\sigma_{\rm sat}$. Therefore, the maximum achievable dynamic range for a given $t_{\rm int}$ is given by

$$\mathrm{DR} = \frac{Q_{\max} t_{\rm int}}{\sigma_{\rm Readout}\sigma_{\rm sat}}.$$

To evaluate the fidelity of the scheme, note that the total output noise power is given by

$$\sigma_i^2 = \begin{cases} \frac{qi_{ph}}{t_{\rm int}} + \frac{q^2\sigma^2_{\rm Readout}}{t^2_{\rm int}} & \text{if } i_{ph} \le \frac{qQ_{\max}}{t_{\rm int}} \\ \frac{qi_{ph}}{t_{\rm sat}(i_{ph})} + \frac{q^2\sigma^2_{\rm Readout}}{t_{\rm sat}(i_{ph})^2} + \frac{(qQ_{\max})^2\sigma^2_{\rm sat}}{t_{\rm sat}(i_{ph})^4} & \text{if } i_{ph} > \frac{qQ_{\max}}{t_{\rm int}}. \end{cases}$$

The SNR is thus given by

$$\mathrm{SNR}(i_{ph}) = \begin{cases} \frac{(i_{ph}t_{\rm int})^2}{qi_{ph}t_{\rm int}+q^2\sigma^2_{\rm Readout}} & \text{if } i_{ph} \le \frac{qQ_{\max}}{t_{\rm int}} \\ \frac{(qQ_{\max})^2}{q^2Q_{\max}+(i_{ph}\sigma_{\rm sat})^2+q^2\sigma^2_{\rm Readout}} & \text{if } i_{ph} > \frac{qQ_{\max}}{t_{\rm int}}. \end{cases}$$

Figure 3 plots SNR versus i_{ph}. Note that SNR is identical to that of the reference sensor within the reference DR. For larger i_{ph}, SNR drops monotonically as $1/i_{ph}^2$ (-20dB per decade) due to the effect of $\sigma_{\rm sat}$. Thus, DR is increased but at the expense of reduction in SNR.

Remarks:

(i) Note that since in this scheme ADC is performed at the column or chip level, we can assume that $\sigma^2_{\rm Readout} = \sigma^2_{\rm Readout-Ref}$. Therefore, SNR at the low end and $i_{\min}$ are the same as that of reference sensor.

(ii) The main parameter affecting DR and SNR at the high end is $\sigma_{\rm sat}$. Reducing $\sigma_{\rm sat}$ requires reducing comparator offset, comparator delay, time-ramp accuracy, and/or kTC of $C_{\rm T-Ref}$. Comparator offset can be reduced using offset cancellation techniques.[23] This reduction, however, is limited by the size of the cancellation capacitor, which cannot be made too large due to the pixel area limitation. Reducing

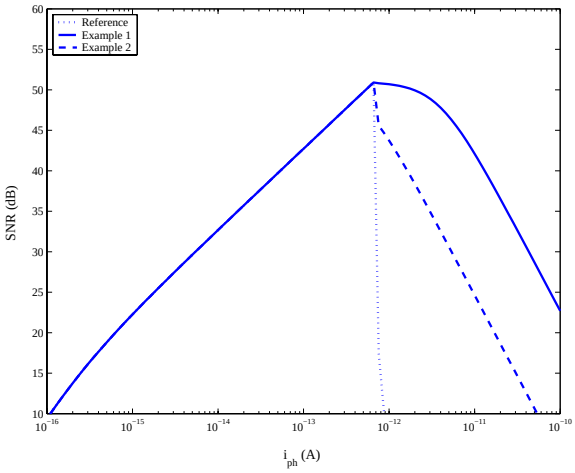

Figure 3. SNR versus i_{ph} for time-to-saturation; assuming $Q_{\rm sat} = 125,000e-$, $\sigma_{\rm Readout} = 5e-$, $t_{\rm int} = 30m$sec. Example 1 assumes $\sigma_{\rm sat} = 0.0005t_{\rm int}$ and achieves DR= 156dB. Example 2 assumes $\sigma_{\rm sat} = 0.004t_{\rm int}$ and achieves DR= 136dB.

comparator delay is severely limited by comparator power consumption. Reducing kTC noise of $C_{\rm T-Ref}$ is also difficult to accomplish due to pixel area limitation. Improving time-ramp accuracy is limited by signal integrity issues due to the high density of the pixel array and the limited number of available interconnect layers.

(iii) The modulator in this scheme is fairly complex, comprising an integrator, a 1-bit comparator and a capacitor, all of which must fit within the pixel. Improving the performance of these components requires increasing pixel area .[24] The accuracy of the analog references, $V_{\rm max}$ and time-ramp, which are critical to the scheme's performance are also limited by the high circuit density and limited pixel area.

(iv) The dominant source of power consumption in this scheme is the comparator, which is always on. Since peak SNR is a strong function of comparator delay and offset, reducing comparator power consumption, e.g., by clocking the comparator,[7] would severely reduce SNR.

4. MULTIPLE-CAPTURE

The multiple-capture scheme[1–3] increases dynamic range by sampling the signal nondestructively multiple times during integration. The HDR image can be constructed using the last-sample-before-saturation algorithm [3] as illustrated in Figure 4. Note that with this algorithm DR is only increased at the high end. DR at the low end can be increased by a combination of image blur prevention and weighted averaging,[21] which requires significant on-chip memory and DSP capability. To define DR and SNR, we assume uniform sampling time $t_{\rm capt}$ and that the filter only performs last-sample-before-saturation and digital CDS. The maximum nonsaturating signal is given by $i_{\rm max} = qQ_{\rm max}/t_{\rm capt}$ and the minimum detectable signal is given by $i_{\rm min} = q\sigma_{\rm Readout}/t_{\rm int}$. Thus

$$\mathrm{DR} = \frac{Q_{\rm max}t_{\rm int}}{\sigma_{\rm Readout}t_{\rm capt}}.$$

To define SNR, let $\phi(i_{ph}) = t_{\rm last-sample}(i_{ph})/(t_{\rm sat}(i_{ph}))$, where $t_{\rm sat}(i_{ph}) = qQ_{\rm max}/i_{ph}$. Then

$$\mathrm{SNR}(i_{ph}) = \frac{(i_{ph}\phi(i_{ph})t_{\rm sat}(i_{ph}))^2}{qi_{ph}\phi(i_{ph})t_{\rm sat}(i_{ph}) + q^2\sigma^2_{\rm Readout}} = \frac{Q^2_{\rm max}}{Q_{\rm max}/\phi(i_{ph}) + \sigma^2_{\rm Readout}/\phi^2(i_{ph})}.$$

For large i_{ph} where shot noise dominates, SNR$\approx \phi(i_{ph})Q_{\rm max}$. Note that when $t_{\rm sat}(i_{ph}) < t_{\rm int}$

$$t_{\rm last-sample}(i_{ph}) = \left\lfloor \frac{t_{\rm sat}(i_{ph})}{t_{\rm capt}} \right\rfloor t_{\rm capt},$$

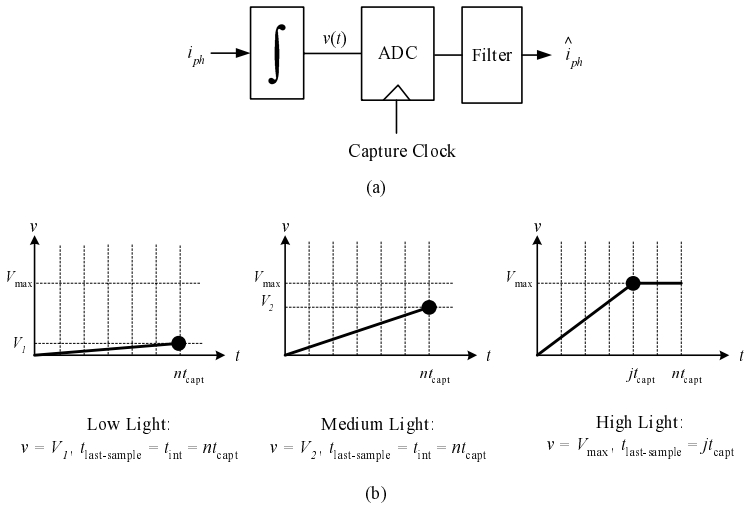

Figure 4. Multiple Capture Block scheme.

and therefore $(1 - t_{\text{capt}}/t_{\text{sat}}(i_{ph}))\, Q_{\max} < \text{SNR}(i_{ph}) < Q_{\max}$. For $t_{\text{sat}}(i_{ph}) \geq t_{\text{int}}$, the SNR follows that of a conventional sensor.

Figure 5 plots SNR versus i_{ph} . Note that unlike time-to-saturation, SNR does not degrade in the extended range, since $t_{\text{last}-\text{sample}}$ has the same accuracy as the multiple capture clock. However, DR suffers at the low end due to the large quantization noise of the per pixel ADC.

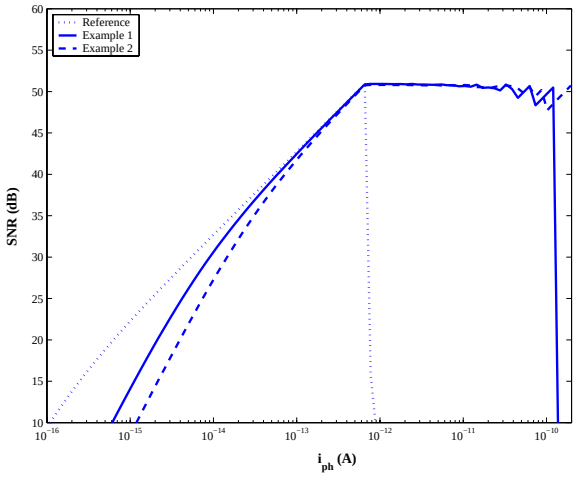

Figure 5. SNR versus i_{ph} for multiple-capture,assuming $Q_{\text{sat}} = 125,000e-$, $t_{\text{int}} = 30m$sec. Example 1 assumes 10 bit ADC, $\sigma_{\text{Readout}} = 35e-$, $t_{\text{capt}} = 150\mu$sec and achieves DR= 117dB. Example 2 assumes 9 bit ADC, $\sigma_{\text{Readout}} = 70e-$, $t_{\text{capt}} = 100\mu$sec and achieves DR= 114dB. The parameters t_{capt} and σ_{Readout} assume comparison time of 100ns and readout time per row per bit of 10nsec and 512×512 pixel array.

Remarks:

(i) Note that because the general implementation of the multiple-capture scheme requires per-pixel ADC,[3] the quantization noise component of σ_{Readout} cannot be ignored. As discussed, this results in DR decrease at the low end relative to the reference sensor. DR can be extended at the low end as discussed in[21]

using a combination of weighted averaging of each pixel's samples to reduce σ_{Readout} and by detecting and preventing image blur to increase t_{int}.

(ii) DR at the high end is directly related to t_{capt}. Increasing $i_{\max}$ requires decreasing t_{capt}. Such decrease can be accomplished by reducing the array readout time and/or the pixel-level ADC time. For large arrays, readout time is the dominant component of t_{capt} and is difficult to reduce. For a given pixel area and power consumption budget, the ADC time can only be decreased by reducing resolution, which results in SNR reduction at the low end.

(iii) The modulator in the multiple-capture scheme is simply an integrator. The ADC is implemented per pixel or per group of neighboring pixels using a 1-bit comparator and digital buffer.[2,3] The ADC requires a global analog reference signal. Similar to the time-to-saturation scheme, the accuracy of the comparator and reference signal are limited by the high array density. Note that $t_{\text{last-sample}}$ is very accurate because of the negligible capture clock jitter. Digital CDS can be used to reduce pixel offsets and kTC noise.

(iv) The dominant sources of power consumption in the multiple-capture scheme are the digital readout and DSP. The pixel level ADC power is typically quite small due to its low operating speed. Readout power can be reduced without greatly affecting SNR by using fewer nonuniform capture times.[25]

5. ASYNCHRONOUS SELF-RESET WITH MULTIPLE CAPTURE

Schemes using self reset attempt to increase DR and SNR at the high end by increasing the effective well-capacity. This can have the additional benefit of increasing peak SNR beyond well-capacity. In this section we investigate the asynchronous self-reset with multiple capture introduced in [4]. The scheme is described in Figure 6. After global reset, photocurrent is integrated and converted into voltage $v(t)$. When $v(t)$ exceeds $V_{\max}$, the comparator flips resetting the integrator asynchronously. The voltage $v(t)$ is sampled at regular time intervals t_{capt} and the digitized samples are used to estimate the photocurrent. To find dynamic range, note that $i_{\min}$ has the same

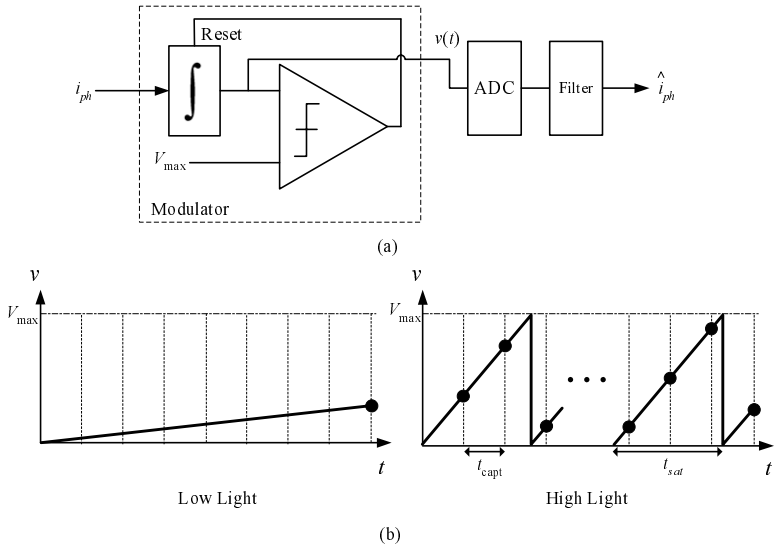

Figure 6. Asynchronous self-reset with multiple capture scheme.

form as that of a conventional sensor. The maximum nonsaturating current is given by $i_{\max} = qQ_{\max}/t_{\text{capt}}$. Thus

$$\text{DR} = \frac{Q_{\max} t_{\text{int}}}{\sigma_{\text{Readout}} t_{\text{capt}}}.$$

In order to calculate SNR, note that the estimation can be viewed as charge integration over the effective integration time

$$t_{\text{int}-\text{eff}} = t_{\text{int}} - n_{\text{reset}} t_{\text{capt}} = t_{\text{int}} \left(1 - \frac{t_{\text{capt}}}{t_{\text{sat}}(i_{ph})}\right), \text{ for } t_{\text{sat}}(i_{ph}) > t_{\text{capt}}.$$

Thus,

$$\text{SNR}(i_{ph}) = \frac{(i_{ph} t_{\text{int}-\text{eff}})^2}{q i_{ph} t_{\text{int}-\text{eff}} + q^2 \sigma^2_{\text{Readout}} + \sigma^2_H (i_{ph} t_{\text{int}-\text{eff}})^2}.$$

The σ^2_H term represents gain FPN due to the photodetector and integrator nonuniformity, which cannot be ignored in this scheme due to the very high i_{ph} in the extended range.

Figure 7 plots SNR versus i_{ph}. Note that SNR increases in the extended DR beyond $Q_{\max}$ as i_{ph} (10dB per decade) before it saturates due to gain FPN and ultimately signal saturation.

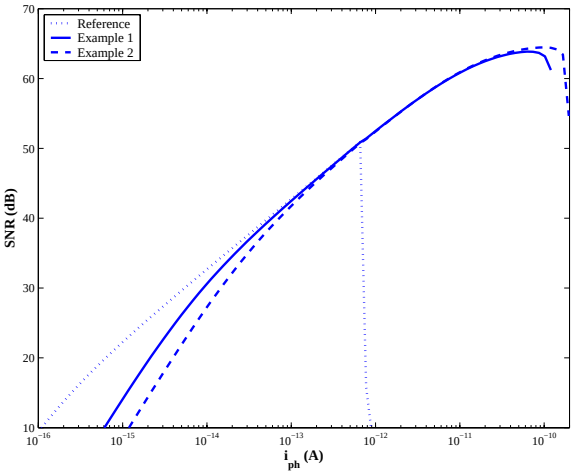

Figure 7. SNR versus i_{ph} for asynchronous self-reset with multiple capture, assuming $Q_{\text{sat}} = 125,000e-$, $t_{\text{int}} = 30m\text{sec}$, $\sigma_H = 0.05\%$. Example 1 assumes 10 bit ADC, $\sigma_{\text{Readout}} = 35e-$, $t_{\text{capt}} = 150\mu\text{sec}$ and achieves DR= 117dB. Example 2 assumes 9 bit ADC, $\sigma_{\text{Readout}} = 70e-$, $t_{\text{capt}} = 100\mu\text{sec}$ and achieves DR= 114dB.

Remarks:

(i) Readout noise for this scheme is the same as that of multiple-capture and can be reduced by weighted averaging. Note that averaging can be more effective in this case due to the random phase induced by the asynchronous self-reset. Also note that weighted averaging also improves SNR in the extended range.

(ii) SNR at the high end can indeed be extended beyond the well capacity limit. However, such extension is limited by gain FPN, which cannot be ignored in this case.

(iii) Since this scheme is the same as multiple-capture with an additional self-reset mechanism, the accuracy of the comparator is relaxed. The accuracy of the self-reset mechanism is also relaxed, since the photocurrent is estimated using the slope of the modulator output waveform.

(iv) Power consumption for this scheme is dominated by digital readout and DSP. Unlike for the multiple-capture scheme, the capture times for this scheme must be uniform.

6. SYNCHRONOUS SELF-RESET WITH RESIDUE READOUT

In this section we discuss the synchronous self-reset with residue readout scheme proposed in [14]. The scheme is described in Figure 8. The photocurrent is integrated and converted into voltage $v(t)$, which is periodically compared to a reference voltage $V_{\max}$. If $v(t) \geq V_{\max}$, the comparator switches, the integrator is reset, and the

counter is incremented. At the end of integration, the digitized value of $v(t_{\text{int}})$ and the reset count are combined to estimate the photocurrent. Let n_{Reset} be the number of resets, then

$$\hat{i}_{ph} = \frac{qQ_{\max}}{t_{\text{int}}} \left(n_{\text{Reset}} + \frac{v(t_{\text{int}})}{V_{\max}} \right).$$

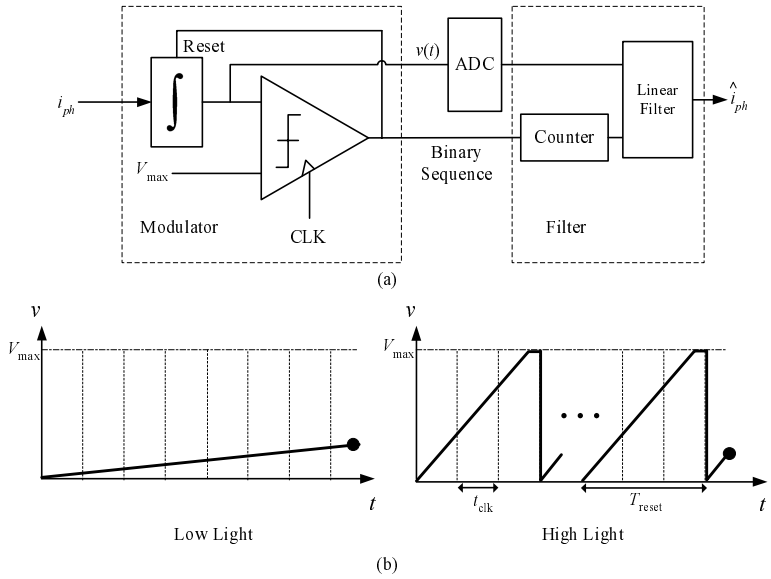

Figure 8. Synchronous self-reset scheme.

To compute DR and SNR, we first compute the distortion due to the underestimation of charge resulting from saturation before synchronous resetting takes place (see the waveform in Figure 8(b)). At the high end, assuming no noise $T_{\text{reset}} = \lceil qQ_{\max}/(i_{ph}t_{\text{clk}}) \rceil \, t_{\text{clk}}$, and the counter output is given by $n_{\text{Reset}} = \lfloor t_{\text{int}}/T_{\text{reset}} \rfloor$.

Therefore, we can write

$$i_{ph} - \frac{i_{ph}t_{\text{clk}}}{t_{\text{int}}} \times \left\lfloor \frac{t_{\text{int}}}{\lceil qQ_{\max}/(i_{ph}t_{\text{clk}}) \rceil \, t_{\text{clk}}} \right\rfloor < \hat{i_{ph}} < i_{ph}.$$

The total average distortion power is therefore given by

$$\sigma^2_{\text{Distortion}} = \frac{1}{3} \left(\frac{i_{ph}t_{\text{clk}}}{t_{\text{int}}} \times \left\lfloor \frac{t_{\text{int}}}{\lceil qQ_{\max}/(i_{ph}t_{\text{clk}}) \rceil \, t_{\text{clk}}} \right\rfloor \right)^2.$$

To find the total noise power we need to add contributions from shot noise, reset noise, residue readout noise, and gain FPN. To estimate the average noise power due to shot noise, we approximate the total integration time for shot noise by t_{int}. Gain FPN in the extended DR is due in part to the comparator and reset offsets that result in offset variation, σ_{Offset}, in $Q_{\max}$. Combining these noise terms with the distortion, we obtain the total noise power

$$\sigma_i^2 = \sigma^2_{\text{Distortion}} + \frac{qi_{ph}}{t_{\text{int}}} + (n_{\text{Reset}} + 1) \left(\frac{q\sigma_{\text{Reset}}}{t_{\text{int}}} \right)^2 + \left(\frac{q\sigma_{\text{Readout}}}{t_{\text{int}}} \right)^2 + \left(\frac{q\sigma_{\text{Offset}} n_{\text{Reset}}}{t_{\text{int}}} \right)^2 + (\sigma_H i_{ph})^2.$$

Therefore SNR is given by

$$\text{SNR}(i_{ph}) = \frac{(i_{ph}t_{\text{int}})^2}{(\sigma_{\text{Distortion}}t_{\text{int}})^2 + qi_{ph}t_{\text{int}} + (n_{\text{Reset}} + 1)(q\sigma_{\text{Reset}})^2 + (q\sigma_{\text{Readout}})^2 + (q\sigma_{\text{Offset}}n_{\text{Reset}})^2 + (\sigma_H i_{ph}t_{\text{int}})^2}.$$

To compute DR for the scheme, note that $i_{\min}$ is given by $i_{\min} = q\sqrt{\sigma^2_{\text{Readout}} + \sigma^2_{\text{Reset}}}/t_{\text{int}}$ and $i_{\max} = \sqrt{3}qQ_{\max}/t_{\text{clk}}$. Therefore,

$$\text{DR} = \frac{\sqrt{3}Q_{\max}t_{\text{int}}}{\sqrt{\sigma^2_{\text{Readout}} + \sigma^2_{\text{Reset}}}t_{\text{clk}}}.$$

Figure 9 plots SNR versus i_{ph} for two examples. Note that SNR in the extended DR first increases as i_{ph} (10dB per decade) then drops as $1/i^2_{ph}$ (-20dB per decade). In particular note the sudden decrease in SNR for the example with high σ_{Offset}.

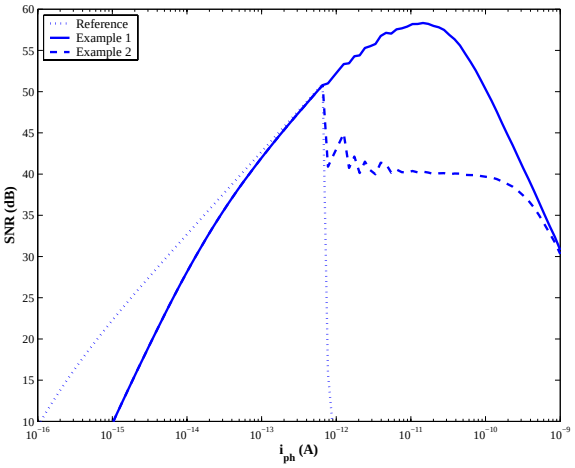

Figure 9. SNR versus i_{ph} for synchronous self-reset , assuming $Q_{\text{sat}} = 125,000e-$, $\sigma_{\text{Readout}} = 35e-$, $t_{\text{int}} = 30m$sec, $t_{\text{clk}} = 1\mu$sec, Example 1: $\sigma_{\text{Offset}} = 0.001Q_{\max}$, Example 2: $\sigma_{\text{Offset}} = 0.01Q_{\max}$, both achieve DR= 161dB.

Remarks:

(i) In [14] CDS is not performed and residue digitization is performed at the pixel level. As a result σ_{Readout} is larger than $\sigma_{\text{Readout}-\text{Ref}}$.

(ii) DR at the high end increases as t_{clk} is decreased. If the counter is integrated in the pixel, DR can be extended with far less power consumption than in other schemes, but at the expense of much larger pixel area. As t_{clk} decreases, however, the speed of the comparator must be increased, which results in higher σ_{Offset} and thus lower SNR.

(iii) The modulator in this scheme comprises an integrator, a comparator, and reset circuit mechanism. The counter and ADC are implemented per pixel. Unlike the asynchronous self-reset with multiple capture scheme, fidelity of the estimated signal is strongly dependent on the offset of the comparator and reset. Moreover, to reduce signal distortion in the extended DR, a faster clock is required resulting in very high power consumption.

(iv) Power consumption of this scheme is dominated by the comparator and digital circuits including the counter.

7. SUMMARY AND CONCLUSION

The paper analyzed SNR for four high dynamic range schemes, time-to-saturation,[8] multiple-capture,[1] asynchronous self-reset with multiple capture,[4] and synchronous self-reset with residue readout.[14] Table 1 summarizes our findings and discussion of the schemes.

In summary all four schemes discussed extend dynamic range at the high end, with synchronous self-reset extending it the most. However, in terms of signal fidelity in the extended DR, synchronous self-reset does

Scheme	Time-to-saturation	Multiple-capture	Asynchronous self-reset	Synchronous self-reset
$i_{\min}$	$= i_{\min-\mathrm{Ref}}$	$\geq i_{\min-\mathrm{Ref}}$	$\geq i_{\min-\mathrm{Ref}}$	$> i_{\min-\mathrm{Ref}}$
$i_{\max}$	$\propto 1/\sigma_{\mathrm{sat}}$	$\propto 1/t_{\mathrm{capt}}$	$\propto 1/t_{\mathrm{capt}}$	$\propto 1/t_{\mathrm{clk}}$
SNR in extended DR	drops as $1/i_{ph}^2$	constant $\approx Q_{\max}$	increase as i_{ph} then saturates	increase as i_{ph} then drops as $1/i_{ph}^2$
Power	comparator	readout/ DSP	readout/ DSP	comparator/digital circuits

Table 1. Summary of results.

not fare well due to the underestimation of charge. Achieving very high DR also requires integrating a counter in each pixel, which results in much larger pixel area than for other schemes. Multiple-capture, on the other hand, does not increase DR as much, but has the advantage of having high fidelity throughout the extended DR. Asynchronous self-reset with multiple capture can achieve even better fidelity in the extended DR, but at the expense of more complex implementation. All schemes except for time-to-saturation have the disadvantage of increasing $i_{\min}$ over the reference conventional sensor. This is most pronounced in the synchronous self-reset scheme, since CDS is not performed. The multiple-capture schemes can mitigate this problem by averaging, but at the expense of additional DSP requirement.

Our discussion of the implementation and power consumption issues was only qualitative, since a quantitative analysis of these issues would require more specific circuit implementations, which is beyond the scope of this paper.

Finally we note that similar analysis of other high fidelity, high dynamic range schemes will be presented in a future paper.[26]

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