Compact DQPSK Demodulator with Interwoven Double Mach-Zehnder Interferometer using Planar Lightwave Circuit

T. Hashimot(1), Y.Nasu(1), Y.Sakamaki(1), K. Hattori(1),
Y. Inoue(1), H. Takahashi(1), H. Kawakami(2), and E. Yoshida(2)
1:NTT Photonics Labs., NTT Corp., 3-1, Morinosato, Atsugi, Kanagawa 243-0198, Japan.
t_hashi@aecl.ntt.co.jp
2:NTT Network Innovation Labs., NTT Corp.

Abstract

We propose a new PLC design for a 43 Gb/s DQPSK demodulator. The design reduces both the module size and the power consumption without degrading any of the module characteristics.

.

Introduction

Optical DQPSK is a promising modulation format for improving the spectral efficiency and PMD tolerance of a 40 Gb/s transmission [1][2]. We have already developed a demodulator using a planar lightwave circuit (PLC) for optical DQPSK [3]. The advantages of using a PLC are reliability, mass producibility and a fast tuning speed. Since PLC technology can provide a highly integrated optical circuit with the flexibility of an optical circuit layout, we can expect to realize very compact optical devices with this technology.

In this paper, we propose a new optical circuit design to reduce the chip size by 60% and show the feasibility of the device.

Optical circuit design

A delayed interferometer for DQPSK demodulation conventionally includes two Mach-Zehnder interferometers (MZIs), which provide approximate one symbol delayed time. There is a λ/4 length difference between the MZIs for the in-phase channel (I-ch) and the quadrature-phase channel (Q-ch), which corresponds to a π/2 phase shift. The input signal is divided with a splitter and sent to each MZI, and the signals are detected with balanced receivers as shown in Fig. 1(a). To reduce the chip area, we have already proposed a compact optical circuit design where I/Q-ch signals are simultaneously demodulated with a common single MZI and separated by a 90º hybrid circuit serially connected to the MZI using a PLC [4] as shown in Fig. 1(b). Although the configuration reduced the optical circuit size, we still needed to make certain improvements. One was to reduce the circuit length, which was increased by the serial connection of the MZI and the 90º hybrid circuit. Another was to improve the asymmetric configuration caused by the use of the 90º hybrid circuit since a symmetric MZI configuration is preferable in terms of installing a

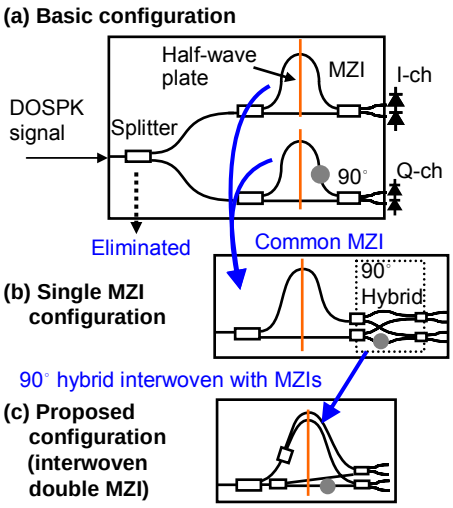

Fig. 1 Miniaturized delayed interferometer

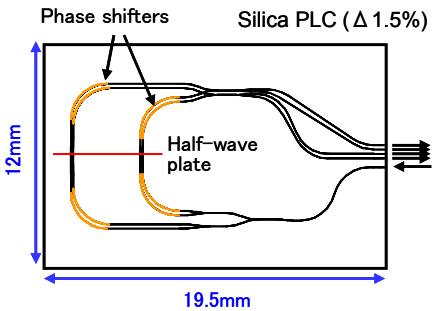

Fig. 2 Fabricated PLC chip and arrangement in 4-inch wafer

half-wave plate to eliminate the polarization dependence caused by the waveguide birefringence.

Figure 1(c) shows our new circuit design for DQPSK demodulation. The 90º hybrid circuit is interwoven with two MZIs, which occupy most of the area of the PLC chip. Note that this is topologically different from the basic configuration in Fig. 1(a). The function that divides the optical signal into the MZIs is incorporated in the interferometers, while the basic configuration needs an additional optical

978-1-4244-2229-6/08/$25.00 ©2008 IEEE

splitter in front of the MZIs. We can reduce the chip size effectively with the new design.

Fabrication of Delayed interferometer and its performance

Figure 2 shows a PLC chip for a 43 Gb/s DQPSK demodulator. The chip was fabricated with a silica PLC with a refractive index difference of 1.5%, and the free spectrum range (FSR) was designed to be 21.5 GHz. The circuit was folded so that it could be connected to the optical fibres at a single facet. Thin film heaters were fabricated on the waveguide as phase shifters for wavelength locking and precise 90º phase control. A half-wave plate was installed in the centre of the MZIs. The phase shifters were symmetrically placed on the MZI arms. This symmetrical design suppressed the difference between the birefringence values of the MZI arms on both sides of the wave plate and reduced the polarization dependent frequency shift (PDf) of the MZI spectrum. With this configuration, we achieved a 60% reduction in chip size compared with the single-MZI type chip [4]. This, for example, provides a 150% yield improvement with a 4-inch wafer.

We packaged the PLC chip in a compact case as shown in Fig. 3. The chip temperature was controlled with a thermo-electrical cooler (TEC) installed in the case. As a result, we realized a compact demodulator with a size of 40 x 12 x 9.5 mm. Downsizing the chip and adopting a smaller TEC corresponding to the chip size also reduced the power consumption needed for temperature stabilization (a major component of the total power consumption) to 1.3 W. The module size and power consumption were both halved compared with the values in our previous report [4]. Figure 4 shows the transmission spectra of the fabricated demodulator. The loss was less than 5.4 dB over the C-band and each port had the desired relative phase difference at π/4 intervals with an FSR of 21.5 GHz. The measured PDf was less than 0.8% of the FSR over the C-band, which is good enough to receive a DQPSK signal [5]. To confirm the applicability for DQPSK demodulation, we also measured the bit error rate (BER) with a back-to-back configuration by connecting the PLC demodulator to a double channel O/E-converter [6]. We observed clear eye opening and a BER of less than 10-8 at an OSNR of 19.5 dB for a 43 Gb/s RZ-DQPSK signal.

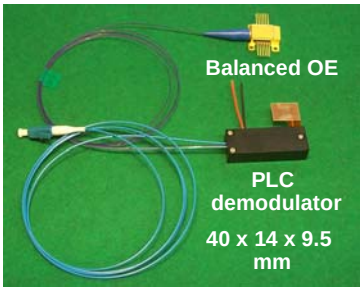

Fig. 3 Assembled demodulator (connected with balanced OE)

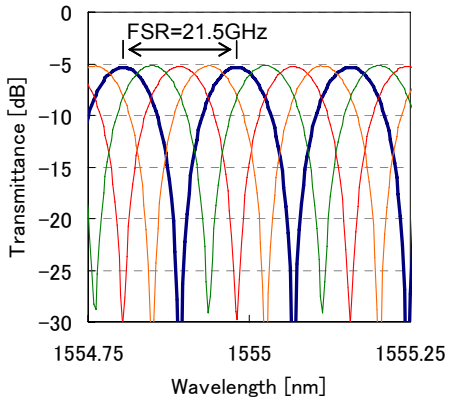

Fig. 4 Spectra of PLC demodulator

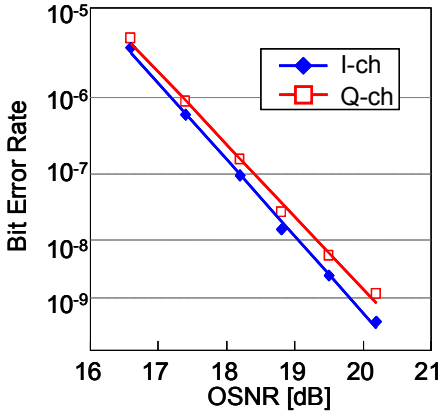

Fig. 5 Reception of 43 Gb/s RZ-DQPSK signal

Conclusion

We proposed a new waveguide design and realized a very compact DQPSK demodulator with half the previous module size and power consumption. The fabricated module exhibited excellent demodulation performance, and we confirmed that it can be employed in a practical DQPSK system

References

1. E. Yoshida, et.al, ECOC2007, 3.1.3, 2007.
2. D. van den Borne, et al., OFC2008, OMQ1, 2008
3. C. R. Doerr et. al, OFC'2005, PDP 12
4. M. Oguma, et. al, ECOC 2007, 10.3.3. 2007
5. H. Kawakami, et. al, Electron. Lett., pp. 122-124, Vol. 43, No. 2, 2007
6. T. Furuta et al., to be published in ECOC2008.