40Gbps, 3-bit Operation of a Semiconductor Optical Digital-to-Analog Converter

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Abstract *We demonstrate 40Gbps, 3-bit-operation of a semiconductor optical digital-to-analog converter consisting of MMI couplers and delay lines. We achieved output with 7-level amplitude with fixed phase successfully for the first time.*

Introduction

Optical packet switch which can operate with high speed and low power consumption is required to process vast data traffic growing in Internet. We have investigated a semiconductor integrated optical digital-to-analog converter(ODAC[1]) type label processor. It converts serial bits of label into a single pulse with multi-level amplitude. So, multiple label signals can be recognized by one step process, and reduction of power consumption, the number of optical devices and the processing step count can be expected.

We have achieved 2-bit operation at 40-Gbit/s[2], but more number of bit processing in one device is desirable due to reduction of number of optical devices and power consumption.

In this report, we demonstrate the first operation of a 40-Gbit/s semiconductor-integrated ODAC with 3-bit processing. Generation of seven-level analog output will be presented.

Principle of 3-bit ODAC

Fig. 1 shows the schematic structure of a 3-bit ODAC. It consists of an input-side 1×3 MMI (multi-mode interference) splitter which also operates as a control of power ratio between three split signals, 1-bit and 2-bit long optical delay lines for 40Gbps operation, and an output-side 3×1 MMI combiner. After a 3bit-digital-to-analog conversion, output signal is split into two, and six-bit processing can be realized by processing the 1st and the 2nd 3-bit processing in parallel. Although the optical gates are not integrated in the semiconductor ODAC in this study, the 3rd and the 6th bit timing for the 1st three bit and the 2nd three bit DA conversion can be extracted by using external optical gates.

The photograph and the device layout are indicated in Fig.2. The waveguide layers were grown on InP substrate by MOCVD. It consisted of a 1.5-μm thick non-doped InP, 0.5-μm thick nondoped InGaAsP (λg=1.06μm), and a 1.5-μm thick non-doped InP. The high mesa structure was formed by deeply etching the epitaxial layer down to InP substrate by iodine-based dry etching[3]. The mesa width was designed to be 2.5-μm for polarization insensitive waveguide. The bending radius was 250μm. The power splitting ratio of the input-side MMI was designed to be 62:33:5 so

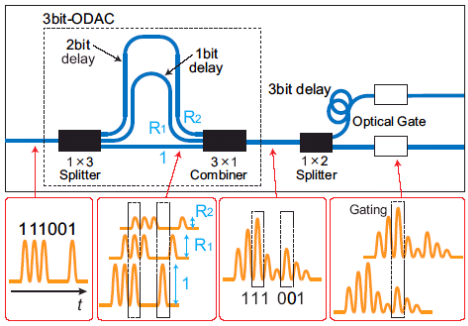

Fig.1 Schematic structure of 3-bit digital-to-analog converter.

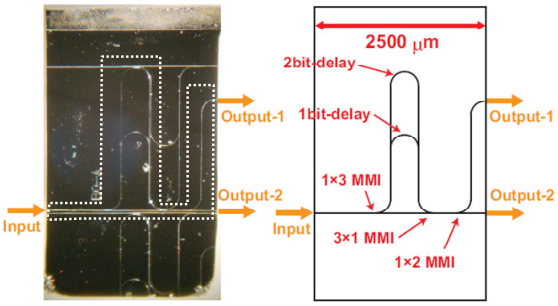

Fig.2 Photograph (left) and the corresponding structure (right) of the fabricated device.

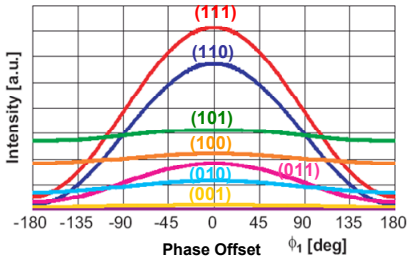

Fig.3 Simulation results of 3-bit digital-to-analog conversion for the designed device.

that the signal to noise ratio for 7-level output signal were close each other. To achieve this splitting ratio, the input port was offset by 4.4μm from the center with 12.8 μm×213.8 μm 1×3 MMI. Phase control between three split signals is performed by thermal control by using a Peltier controller. To obtain arbitrary combination of phase difference between the 1st and the 2nd, and the 2nd and the 3rd delay line, the 2nd and the 3rd delay line length were designed to be +1.4% and -1.3% different from the ideal lengths.

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Device size was 2500μm × 3200μm. The insertion loss was 27dB including fiber coupling loss for both facets.

Simulation of output signal intensity

Simulation results of output light intensity as a function of optical phase offset between the 1st and the 2nd delay line are indicated in Fig.3. Splitting ratio of the designed numerical values was used. We can see that the output light intensity for the optimized phase offset (ϕ_1=0) is aligned according to the label pattern. The difference of each level is not equal because the splitting ratio was not optimized. The optimized splitting ratio could be achieved by the combination of the offset of both input and the output port at the same time.

Experiments and results

The output signal for a semiconductor ODAC was evaluated. Experimental setup is shown in Fig.4. In the ODAC operation observation, the input signal pulse with 40Gbps NRZ, 25ps-wide was used. The input light was coupled using lensed fibers for both input and output port, and the output signal waveform were measured using a sampling oscilloscope. Seven kinds of three-bit input signal patterns except "000" were used as shown in Figs.5(a1) to (g1). Because of the larger loss in the optical delay line, the 1st, 2nd, and 3rd bit in the time domain correspond to the logical 3rd, 2nd and 1st bit, respectively. Temperature was set by a Peltier controller, and it was fixed under the condition for obtaining the output signal intensity aligned to the order of input label patterns. Figs.5(a2) to (g2) show the waveforms of the output signals. And the output signal waveforms drawn on the same graph are indicated in Fig.6. The time slot surrounded by the dotted rectangle corresponds to the output of the digital-to-analog conversion in both cases. Although the target time slot was not gated, different intensity of the output signal was generated from 3-bit ODAC at 40Gbps successfully.

Conclusions

We have fabricated a semiconductor digital-to-analog converter for 40-Gbit/s and 3-bit operation, and we evaluated its operation performance. Seven-level analog output could be achieved successfully for the first time.

References

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3 A. Matsutani et al., Jpn. J. Appl. Phys., vol. 44, no. 19 (2005) pp.L576.

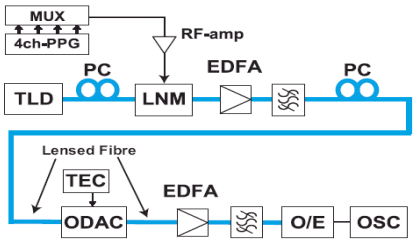

Fig.4 Experimental setup of 40Gbps, 3-bit digital-to-analog conversion performance.

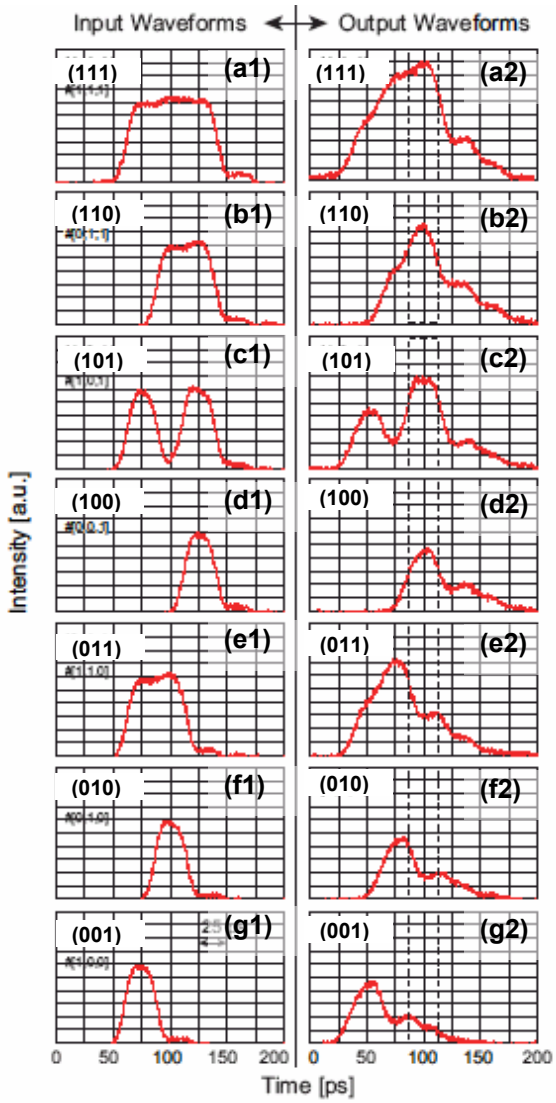

Fig.5 Waveforms of input (left) and output(right) for label pattern (111) to (001) (from top to bottom).

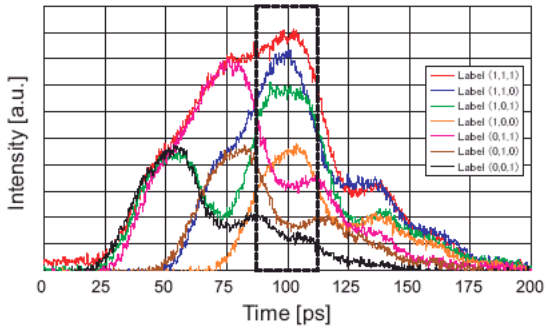

Fig.6 7-level output signals.