OPERA: OPtimization with Ellipsoidal uncertainty for Robust Analog IC design *

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ABSTRACT

As the design-manufacturing interface becomes increasingly complicated with IC technology scaling, the corresponding process variability poses great challenges for nanoscale analog/RF design. Design optimization based on the enumeration of process corners has been widely used, but can suffer from inefficiency and overdesign. In this paper we propose to formulate the analog and RF design with variability problem as a special type of robust optimization problem, namely robust geometric programming. The statistical variations in both the process parameters and design variables are captured by a pre-specified confidence ellipsoid. Using such *optimization with ellipsoidal uncertainty* approach, robust design can be obtained with guaranteed yield bound and lower design cost, and most importantly, the problem size grows *linearly* with number of uncertain parameters. Numerical examples demonstrate the efficiency and reveal the trade-off between the design cost versus the yield requirement. We will also demonstrate significant improvement in the design cost using this approach compared with corner-enumeration optimization.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids

General Terms

Design, Algorithm

Keywords

Statistical optimization

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1. INTRODUCTION

With semiconductor fabrication technologies scaled below 100nm, process variability caused by subwavelength lithography and numerous manufacturing steps impacts the circuit performance and the parametric yield of analog and RF ICs significantly. Design for manufacturability (DFM) technologies are required to enhance the communication across the design manufacturing interface (as shown in Figure 1) so that the process variability can be considered in the early stage of analog circuit design exploration. Therefore, new algorithms and the corresponding methodologies are compulsory to judiciously incorporate the process variability into the analog design flow [1].

Various methods [2, 3, 4, 5] have been proposed to optimize statistical performance including the process variability. Designs Of Experiment (DOE) is usually used to establish the relation between high order process effects and circuit responses. Then, detailed circuit simulations or even Monte Carlo analysis for each design are necessary to find the response surface model that describes the circuit sensi-

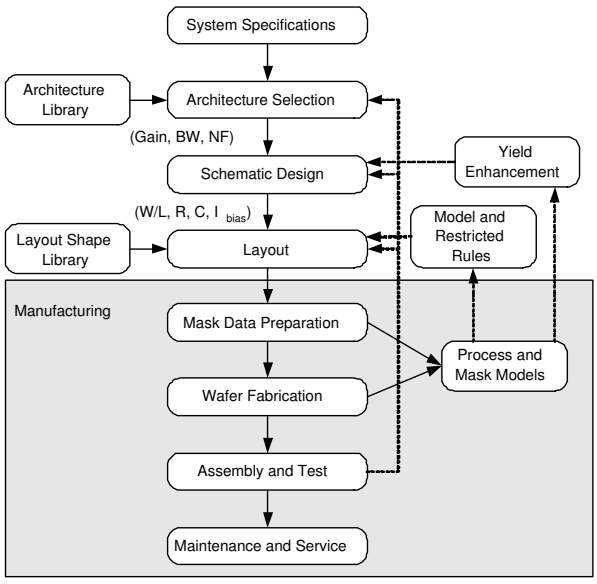

Figure 1: Design-manufacturing interface in modern analog design flow.

tivities and correlations to and among the process parameters and design variables. By centering the design variables in the most insensitive region, maximum parametric yield can be obtained. These methods require accurate characterization of the statistical circuit response at the expense of larger computation especially when the design space is large. Therefore, they are most useful in the production phase as fine tuning methods of the design.

To consider process variability in the early stages of design exploration, the traditional corner-enumeration worst-case design optimization has been the most widely used technique (see, *e.g.*, [6]). The process parameters take values within a certain range which forms a tolerance "box"; the circuit performance is optimized for all of the "corners", or the vertices of the formed polyhedron. This optimization approach assumes minimum knowledge of the process parameters and often leads to a worst-case design. However, the applications of the corner-enumeration optimization approach are limited for the following reasons. First, by assuming process parameters are independently uniformly distributed, this method intrinsically ignores the useful information about the underlying statistical distributions and correlations. Second, the problem size will increase exponentially with the number of uncertain parameters. In addition, even when the process parameters fall inside of the tolerance box, in general there is no guarantee for circuit performance meeting the specifications, consequently, no guarantee for the yield requirement. Furthermore, for a given yield requirement, design for all corners usually results in over-conservative design with substantially degenerated circuit performance.

In this paper we propose a new algorithm, OPERA, in which the design with variability problem is reformulated as a special form of robust optimization, specifically robust geometric programming (GP). In OPERA, the normal variations in both the process parameters and design variables are modeled using ellipsoidal uncertainty of GP parameters. Unlike corner-enumeration worst-case design, the problem size grows *linearly* with number of uncertain parameters. Recent advances in robust optimization show that this type of optimization with ellipsoidal uncertainty can be solved efficiently and accurately [7].

We demonstrate the applications of our robust design via OPERA using two design examples, a ring oscillator and an LC oscillator, because the parametric yield of an oscillator is quite sensitive to the variability of the center frequency. The numerical results reveal that robust designs can be obtained with guaranteed yield bound and lower design cost. In addition, the trade-off curve of design cost versus yield requirement can be easily obtained and analyzed. It is also demonstrated that much less over-design is incurred when compared with the design from corner-enumeration optimization.

This paper is organized as follows. Modeling of the manufacturing variability and formulation of the robust optimization are briefly introduced in §2. In §3, we formulate the design with variability problem as optimization with ellipsoidal uncertainty. We also show how to capture the normal process variations by a pre-specified confidence ellipsoid. In §4 we address several implementation issues that result from reformulating GP in posynomial form with normal process variations as robust GP with ellipsoidal uncertainty. Two robust design examples are given in §5 as demonstration, followed by conclusions in §6.

2. BACKGROUND

2.1 Process variation sources and modeling

The IC performance variability is impacted by two distinct sets of factors: *environmental factors* and *physical factors*. The environmental factors usually include variations in power supply voltage and temperature. The physical factors include variations in the electrical and physical parameters that characterize the behavior of active and passive devices, such as V_{th}, T_{ox}, L_{eff} etc. The process parameter variability can be measured through the ratio of the standard deviation (σ) and the mean value (μ). Table 1 compiled from [8] listed the increasing parameter variability of five technologies in the 250 to 70 nm gate length range.

Year	Tech node	L_{eff}	T_{ox}	V_{th}	W	H	ρ
1997	$0.25\mu m$	10.7%	2.67%	3.33%	8.33%	8.33%	7.41%
1999	$0.18\mu m$	11.1%	2.67%	3.33%	8.72%	10.00%	8.00%
2002	$0.13\mu m$	11.5%	3.25%	3.33%	9.33%	10.00%	9.09%
2005	$0.10\mu m$	13.3%	4.00%	3.81%	10.00%	11.25%	10.56%
2006	$0.07\mu m$	15.7%	5.33%	4.44%	11.11%	11.90%	11.11%

Table 1: Trends of variability (σ/μ) in DSM technologies.

To model this variability, we associate a statistical distribution to each parameter type. We may use a uniform distribution over the range of the specifications for environmental factors. For example, the temperature can be modelled as a uniform distribution random variable from -25 to 125 degree Celsius. The physical parameters are typically represented by some joint probability density function $N(\mu, \Sigma)$, where μ is a vector of means and Σ is a variance/covariance matrix. The correlation of these parameters must be modeled since systematic variations are dominant for most nanoscale technologies [8].

2.2 Robust optimization

The idea of robust optimization [9, 10] is to explicitly incorporate a model of data uncertainty in the formulation of an optimization problem. A large class of robust optimization problems can be formulated as

$$\begin{array}{ll} \text{minimize} & \sup_{u\in\mathcal{U}} f_0(y,u) \\ \text{subject to} & \sup_{u\in\mathcal{U}} f_i(y,u) \le 0, \quad i=1,\ldots,m, \end{array} \tag{1}$$

where y is the optimization variable, u represents the uncertain problem data, and the set $\mathcal{U}$ describes the uncertainty in u,

Note that the robust optimization problem (1) is a convex problem if f_i, $i = 0, 1, \ldots, m$ are convex in y for each $u \in \mathcal{U}$. However, even if the resulting robust optimization problem is convex, it is often much larger and more difficult to solve than the corresponding nonrobust convex optimization problem, so the added robustness of an optimization problem can come at a high price.

3. PROPOSED APPROACH

The circuit design with process variability problem can be cast as an optimization with a specific model uncertainty problem as in the robust optimization formulation (1). Recently, geometric programming [11] has found successful applications in the field of circuit design, *e.g.*, [6, 12, 13]. Therefore, to include the process variability in the early stage of design, we propose to formulate the circuit design with variability problem as robust geometric programming, which can systematically incorporate a model of data uncertainty in a GP and optimize for all the given scenarios under this model. Then, the various sources of variations can be modeled as the ellipsoidal uncertainty.

3.1 Optimization with ellipsoidal uncertainty

Assuming that (A_s, b_s) is uncertain, but known to belong to the image of a set $\mathcal{U} \subset \mathbb{R}^L$ under the affine mapping

$$\left(\tilde{A}_s(u), \tilde{b}_s(u)\right) = \left(A_s^0 + \sum_{j=1}^{L} u_j A_s^j, b_s^0 + \sum_{j=1}^{L} u_j b_s^j\right), \tag{2}$$

where $A_s^j \in \mathbb{R}^{K_s \times n}$, $b_s^j \in \mathbb{R}^{K_s}$, $j = 0, 1, \ldots, L$. The corresponding robust geometric program in *convex* form can then

be formulated as

$$\begin{array}{ll}\text{minimize} & c^T y \\ \text{subject to} & \sup_{u\in\mathcal{U}} \mathbf{lse}\left(\tilde{A}_s(u)y + \tilde{b}_s(u)\right) \le 0,\ s = 1,\ldots,m,\end{array} \tag{3}$$

where $\mathbf{lse}(z) \triangleq \log(e^{z_1} + \cdots + e^{z_k})$ is called the *log-sum-exp* function. In addition, in this paper we assume the robust GP (3) has *ellipsoidal uncertainty*, in which $\mathcal{U}$ is an ellipsoid:

$$\mathcal{U} = \left\{ \bar{u} + P\rho \;\middle|\; \|\rho\|_2 \le 1,\ \rho \in \mathbb{R}^L \right\}, \tag{4}$$

where $\bar{u} \in \mathbb{R}^L$ and $P \in \mathbb{R}^{L\times L}$.

It is not known whether the robust GP (3) with ellipsoidal uncertainty (4) can be reformulated as a tractable (convex) optimization problem. However, a tractable approximation method that yields a good compromise between solution accuracy and computational efficiency has been proposed. Refer to [7] for more details.

3.2 Capturing process variations by confidence ellipsoid

Recall that a normal random variable $u \in \mathbb{R}^n$ with mean $\bar{u}$ and covariance matrix $\Sigma = \Sigma^T > 0$, *i.e.*, $u \sim N(\bar{u}, \Sigma)$, has the probability density function (pdf)

$$p_u(\xi) = (2\pi)^{-n/2}(\det\Sigma)^{-1/2} e^{-1/2(\xi-\bar{u})^T\Sigma^{-1}(\xi-\bar{u})}. \tag{5}$$

Obviously $p_u(\xi)$ is constant for $(\xi-\bar{u})^T\Sigma^{-1}(\xi-\bar{u}) = \gamma$, *i.e.*, on the surface of ellipsoid

$$\mathcal{E}_\gamma = \{\xi \mid (\xi-\bar{u})^T\Sigma^{-1}(\xi-\bar{u}) \le \gamma\}. \tag{6}$$

Here $\mathcal{E}_\gamma$ is called a *confidence ellipsoid* of u. It is well-known that the nonnegative random variable $(u-\bar{u})^T\Sigma^{-1}(u-\bar{u})$ has a chi-squared distribution with degree n, *i.e.*,

$$\mathbf{Prob}(u \in \mathcal{E}_\gamma) = F_{\chi_n^2}(\gamma), \tag{7}$$

where $F_{\chi_n^2}$ is the cumulated distribution function of χ_n^2.

If the process variations are normally distributed with the density function (5), a pre-specified amount of mass of probability $0 < \alpha < 1$ can be captured by the confidence ellipsoid $\mathcal{E}_\gamma$ (6) with $\alpha = F_{\chi_n^2}(\gamma)$, as illustrated in Figure 2.

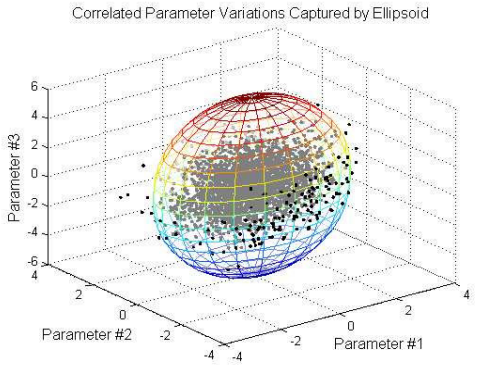

Figure 2: Capturing correlated process parameter variations by a confidence ellipsoid.

3.3 Yield-guaranteed robust design

Suppose the uncertainty parameter $u \in \mathbb{R}^L$ in the robust GP (3) is *random* and normally distributed with the density function (5). Given $0 < \alpha < 1$, we say $\hat{y} \in \mathbb{R}^n$ has *yield* no lower than α if

$$\mathbf{Prob}\left(\mathbf{lse}\left(\tilde{A}_i(u)\hat{y} + \tilde{b}_i(u)\right) \le 0,\ \ i = 1,\ldots,m\right) \ge \alpha.$$

The yield-guaranteed robust design can be obtained as follows. Let the ellipsoidal uncertainty set $\mathcal{U}$ in (4) to be the confidence ellipsoid $\mathcal{E}_\gamma$ define in (6). In this case, all the feasible solutions of the robust GP (3) have yield no lower than $F_{\chi_n^2}(\gamma)$. Therefore, in the robust GP framework, we can capture both the independent and the correlated normal randomness by the ellipsoidal uncertainty (6), and the resulting feasible solutions always have guaranteed yield bound $F_{\chi_n^2}(\gamma)$.

4. IMPLEMENTATION ISSUES

4.1 Lognormal approximation of narrow normal distributions

Let u be normally distributed with mean μ and variance σ^2; assume u is *narrow*, *i.e.*, $\sigma \ll \mu$. We know that its mass of probability is mostly concentrated in the small interval $[\mu-3\sigma,\ \mu+3\sigma]$. To approximate the narrow normal random variable u by a lognormal random variable, of which pdf is defined on *positive* real numbers, here we assume $\mu - 3\sigma > 0$ such that most of u (with high probability) is distributed within a positive interval. Therefore, for all $\xi \in [\mu-3\sigma,\ \mu+3\sigma]$, $\xi/\mu \simeq 1$, which further implies $\log(\xi/\mu) \simeq \xi/\mu - 1$. Hence for all $\xi \in [\mu-3\sigma,\ \mu+3\sigma]$,

$$\begin{aligned} p_u(\xi) &= (2\pi)^{-1/2}\sigma^{-1} e^{-(\xi-\mu)^2/(2\sigma^2)} \\ &\simeq (2\pi)^{-1/2}((\sigma/\mu)\xi)^{-1} e^{-(\log\xi-\log\mu)^2/(2(\sigma/\mu)^2)}. \end{aligned}$$

Therefore, narrow normal distributions can be accurately approximated by lognormal distributions:

$$\sigma \ll \mu: \quad N(\mu,\sigma^2) \simeq LN(\log\mu, (\sigma/\mu)^2). \tag{8}$$

(The proof of the generic lognormal approximations of normal distributions can be found in [14].)

4.2 Incorporate process variations in GP of posynomial form

Many optimization-based circuit designs result in geometric programs of *posynomial* form. When process variations are incorporated, the robust design with guaranteed yield bound can be formulated as the following optimization problem:

$$\begin{array}{ll}\text{minimize} & c^T x \\ \text{subject to} & \mathbf{Prob}(f_s(x,p) \le 1,\ s = 1,\ldots,m) \ge \alpha,\end{array} \tag{9}$$

where $0 < \alpha < 1$ is the required yield bound, $x \in \mathbb{R}^{n_x}$ are the design variables, $p \in \mathbb{R}^{n_p}$ represents the process parameters, and

$$f_s(x,p) \triangleq \sum_{k=1}^{K_s}\left(d_{ks}\prod_{i=1}^{n_p}(p_i+\delta p_i)^{b_{iks}}\prod_{j=1}^{n_x}(x_j+\delta x_j)^{a_{jks}}\right). \tag{10}$$

Here the process variations in the process parameter p_i and design variable x_i are modeled by the random variables δp_i and δx_i respectively. Another implicit assumption is that $f_s(x,p)$ is posynomial in x and p when we let $\delta p_i = 0,\ i = 1,\ldots,n_p$ and $\delta x_j = 0,\ j = 1,\ldots,n_x$.

4.2.1 Variance-linked-to-mean variations in process parameters

Consider the robust design (9) with required yield bound α. Assume $\delta x_j = 0,\ j = 1,\ldots,n_x$ in (10), *i.e.*, no variation in the design variables. We model the variance-linked-to-mean, normal variations in process parameters by

$$\delta p_i/p_i \sim N(0,\sigma_{p_i}^2), \quad i = 1,\ldots,n_p,$$

$$f_s(x,p) \;\simeq\; \sum_{k=1}^{K_s}\left(d_{ks}\prod_{i=1}^{n_p}(p_i e^{\delta p_i/p_i})^{b_{iks}}\prod_{j=1}^{n_x}x_j^{a_{jks}}\right) \;=\; \sum_{k=1}^{K_s}\exp\left[\left(c_{ks}+\sum_{i=1}^{n_p}b_{iks}q_i\right)+\sum_{i=1}^{n_p}b_{iks}u_i+\sum_{j=1}^{n_x}a_{jks}y_j\right] \tag{11}$$

where $\sigma_{p_i} \ll 1,\ i=1,\ldots,n_p$ are given. Let $\Sigma_p = \Sigma_p^T > 0$ be the covariance matrix of $\delta p_i/p_i,\ i=1,\ldots,n_p$. For values of δp_i with high probability, $f_s(x,p)$ can be inferred from (11), in which $c_{ks} = \log d_{ks}$, $q_i = \log p_i$, $u_i = \delta p_i/p_i$, and $y_j = \log x_j$. Therefore, $f_s(x,p) \le 1$ can be reformulated as a log-sum-exp constraint

$$\mathbf{lse}\left(\left(A_s^0+\sum_{j=1}^{n_p}u_jA_s^j\right)y, b_s^0+\sum_{j=1}^{n_p}u_jb_s^j\right) \le 0 \tag{12}$$

with appropriate A_s^j and $b_s^j,\ j=0,1,\ldots,n_p$. We can reformulate each constraint $f_s(x,p)\le 1$ of (9) in form of the above log-sum-exp constraint and then obtain a robust GP of the form (3) with the ellipsoidal uncertainty:

$$\mathcal{U} = \{u\in\mathbb{R}^{n_p} \mid u^T\Sigma_p^{-1}u \le \gamma\}, \tag{13}$$

where γ satisfying $F_{\chi^2_n}(\gamma) = \alpha$. Assume $\hat{y}\in\mathbb{R}^{n_x}$ is a feasible solution of the resulting robust GP. Then $\hat{x}_j = e^{\hat{y}_j},\ j = 1,\ldots,n_x$ satisfy (9), *i.e.*, $\hat{x}\in\mathbb{R}^{n_x}$ has yield no lower than α.

4.2.2 Variance-not-linked-to-mean variations in design variables and process parameters

Consider the robust design (9) with required yield bound α. Assume upper and lower bounds for each design variable are given:

$$0 < L_j \le x_j \le U_j, \quad j=1,\ldots,n_x. \tag{14}$$

We model the variance-not-linked-to-mean, normal variations in process parameters and design variables by

$$\delta p_i \sim N(0,\sigma_{p_i}^2), \quad i=1,\ldots,n_p,$$
$$\delta x_j \sim N(0,\sigma_{x_j}^2), \quad j=1,\ldots,n_x.$$

Here we assume $\sigma_{p_i} \ll p_i,\ i=1,\ldots,n_p$. In addition, we assume $\sigma_{x_j} \ll x_j,\ j=1,\ldots,n_x$. (Note that in general we can verify if this assumption holds since in many circuit designs it is easy to determine reasonable range of values for each design variable, *e.g.*, (14).) We also assume $p_i - 3\sigma_{p_i} > 0,\ i=1,\ldots,n_p$ and $x_j - 3\sigma_{x_j} > 0,\ j=1,\ldots,n_x$. Therefore, by (8),

$$p_i+\delta p_i \;\simeq\; LN\left(\log p_i, (\sigma_{p_i}/p_i)^2\right), \quad i=1,\ldots,n_p,$$
$$x_j+\delta x_j \;\simeq\; LN\left(\log x_j, (\sigma_{x_j}/x_j)^2\right), \quad j=1,\ldots,n_x.$$

Recall that a lognormal random variable $v\sim LN(\mu,\sigma^2)$ can be inferred from $v = e^{\mu+\sigma u}$ with $u\sim N(0,1)$. Then $f_s(x,p)$ can be inferred from (15), in which $c_{ks} = \log d_{ks}$, $q_i = \log p_i$, and $y_j = \log x_j$. Here $u_i \sim N(0,1),\ i = 1,\ldots,n_p$ and $\hat{u}_j\sim N(0,1),\ j=1,\ldots,n_x$; $\alpha_j+\beta_j y_j,\ j = 1,\ldots,n_x$ are linear approximations of e^{-y_j} subject to $y_j\in[\log L_j, \log U_j],\ j=1,\ldots,n_x$ respectively. (Many methods, *e.g.*, least-square fitting, can be used to find good linear approximations for e^{-y_j} within the interval $[\log L_j, \log U_j]$.) Therefore, we can reformulate each constraint $f_s(x,p)\le 1$ in (9) as a log-sum-exp constraint (like (12)) to obtain a robust GP of the form (3) with the ellipsoidal uncertainty:

$$\mathcal{U} = \{\xi = (u,\hat{u}) \mid \xi^T\Sigma_\xi^{-1}\xi \le \gamma,\ \xi\in\mathbb{R}^{n_p+n_x}\}, \tag{16}$$

where γ satisfying $F_{\chi^2_n}(\gamma) = \alpha$, and $\Sigma_\xi = \Sigma_\xi^T > 0$ is the covariance matrix of $u_i,\ i=1,\ldots,n_p$ and $\hat{u}_j,\ j=1,\ldots,n_x$. Assuming $\hat{y}\in\mathbb{R}^{n_x}$ is a feasible solution of the resulting robust GP, then $\hat{x}_j = e^{\hat{y}_j},\ j=1,\ldots,n_x$ satisfy (9), *i.e.*, $\hat{x}\in\mathbb{R}^{n_x}$ has yield no lower than α.

5. ROBUST DESIGN EXAMPLES

5.1 Robust design of an RF ring oscillator

The first example we will show is the robust design of a 5GHz Ring Oscillator (RO). The specific RO topology we consider here is shown in Figure 3. This is a widely used building block to characterize process variations. The performance and design variable relation has been extensively studied, *e.g.*, [15, 16, 17].

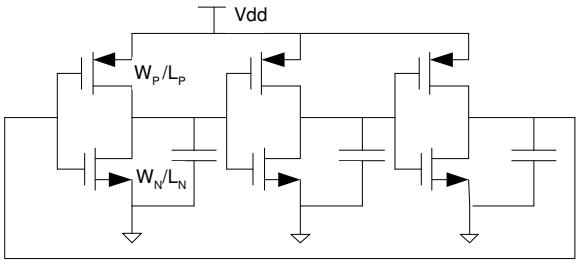

Figure 3: Topology of the ring oscillator.

To simplify the robust GP formulation, we consider three design variables and three performance specifications for this RO design. The three design variables are: effective width $W_{\text{eff}} = W_n + W_p$, gate length $L = L_n = L_p$, and gate over drive ΔV. They are related to the sizing and biasing of the NMOS and PMOS transistors.

The RO is designed to consume minimal dynamic power for a certain center frequency. In addition, the phase noise must be kept below a given threshold. The design optimization can be formulated as:

$$\begin{array}{ll} \text{minimize} & P(W_{\text{eff}}, L, \Delta V) \\ \text{subject to} & N(W_{\text{eff}}, L, \Delta V) \le N^{\max}, \\ & f_{\text{resonant}}(W_{\text{eff}}, L, \Delta V) = f_0, \end{array} \tag{17}$$

where f_0 is the given resonant center frequency, P is the consumed dynamic power, N is the phase noise and $N^{\max}$ denotes its maximum allowable value.

In this example, we consider four variance-not-linked-to-mean independent normal variations in process parameter and design variables. They are the gate width variation ΔW, the gate length variation ΔL, the gate oxide thickness variation ΔT_{ox} and the threshold voltage variation ΔV_{th}. Here the gate oxide thickness variation ΔT_{ox} is reflected by coefficient perturbation in the GP of posynomial form (*i.e.*, δp_i in (10)), and other three parameter variations are reflected by design variable perturbation (*i.e.*, δx_i in (10) and ΔV_{th} is considered as the gate overdrive voltage perturbation). Then the design optimization (17) can be formulated as the GP of posynomial form considered in §4.2.2, which can be further reformulated in form of the robust GP (3) to carry out robust design with guaranteed yield bound, as described in §3.3.

The process parameter values used in the numerical example are extracted from the IBM 7HP 0.18μm BiCMOS technology. The design is optimized when the confidence ellipsoid captures 90% of process variations and the center frequency is relaxed by 20%, *i.e.*, within the interval

$$f_s(x,p) \simeq \sum_{k=1}^{K_i}\left(d_{ks}\prod_{i=1}^{n_p}\left[\exp\left(\log p_i + \frac{\sigma_{p_i}}{p_i}u_i\right)\right]^{b_{iks}}\prod_{j=1}^{n_x}\left[\exp\left(\log x_j + \frac{\sigma_{x_j}}{x_j}\hat{u}_j\right)\right]^{a_{jks}}\right)$$
$$\simeq \sum_{k=1}^{K_i}\exp\left[\left(c_{ks}+\sum_{i=1}^{n_p}b_{iks}q_i\right)+\left(\sum_{i=1}^{n_p}b_{iks}\frac{\sigma_{p_i}}{p_i}u_i+\sum_{j=1}^{n_x}a_{jks}\sigma_{x_j}\alpha_j\hat{u}_j\right)+\sum_{j=1}^{n_x}a_{jks}y_j+\sum_{j=1}^{n_x}a_{jks}\sigma_{x_j}\beta_j\hat{u}_j y_j\right] \quad (15)$$

[4GHz, 6GHz]. The design resulting from robust GP is compared with the design resulting from GP as listed in Table 2 and their performance mean values are listed in Table 3.

Design variable	GP design	Robust GP design
W_{eff}	4.53μm	6.68μm
L	0.26μm	0.24μm
ΔV	0.42V	0.387V

Table 2: RO design results.

Performance mean	GP design	Robust GP design
Power	1.87mW	2.59mW
Phase noise	-100dBc/Hz	-101dBc/Hz
Frequency	5GHz	4.85GHz

Table 3: RO performance mean values.

A Monte Carlo analysis with 10,000 sample points is used to evaluate the performance variability and the parametric yield. Histograms of the phase noise performance of two designs resulting from GP and robust GP optimization are shown in Figure 4. It can be concluded that higher yield can be obtained through the robust design with more design cost compared with the nominal design.

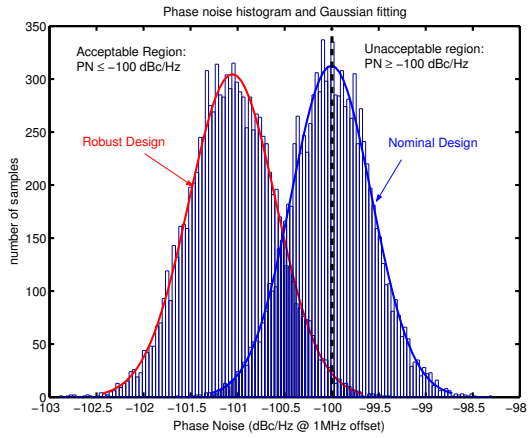

Figure 4: Phase noise histograms.

We further use the concentric ellipsoids $\mathcal{E}_\gamma$ (16) with various values of γ to capture different percentages of process variations. The trade-off between the design cost and the yield bound is shown in Figure 5, where the design cost (power consumption in this example) increases when higher yield bound is requested. It is also observed that a drastic increase in the design cost will be incurred to obtain yield close to 100%.

5.2 Robust design of an LC oscillator

We next use a 2.1GHz LC oscillator design example based on the topology and tank model shown in Figure 6 to compare the robust optimization and the corner-enumeration optimization.

Five design variables and five performance specifications are considered for this LC oscillator design. The five design

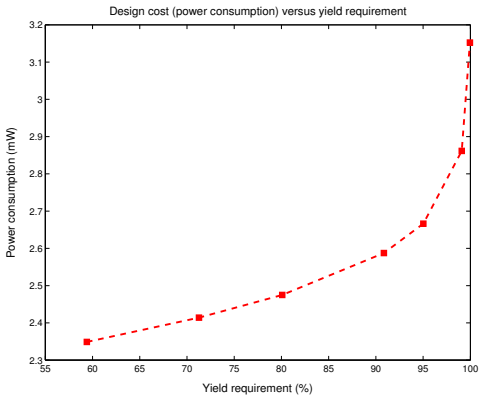

Figure 5: Ring oscillator: design cost versus yield requirement.

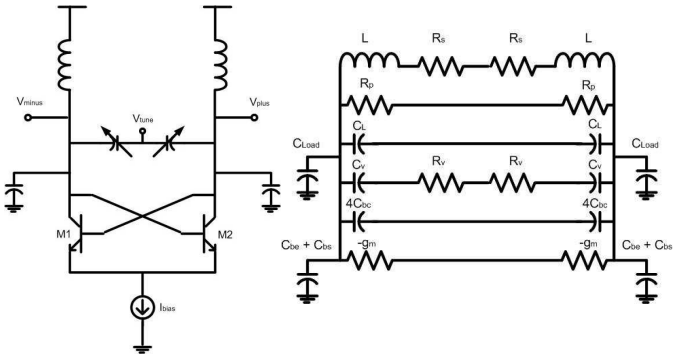

Figure 6: Topology and lumped tank model of an LC oscillator.

variables are: the biasing tail current I_{bias}, the output swing voltage V_{SW}, the inductance L, the tank conductance g_{tank}, and the tank capacitance C_{tank}. The latter three are key design variables in the lumped tank model.

The LC oscillator was designed to consume minimal dynamic power for a certain center frequency [13]. The design optimization has the following form:

$$\begin{array}{ll} \text{minimize} & P(I_{\text{bias}}) \\ \text{subject to} & N(I_{\text{bias}}, g_{\text{tank}}, C_{\text{tank}}, L, V_{\text{SW}}) \le N^{\max}, \\ & f_{\text{resonant}}(C_{\text{tank}}, L) = f_0, \\ & G(I_{\text{bias}}, g_{\text{tank}}) \ge G^{\min}, \\ & V_{\text{SW}} \le V_{\text{dd}}, \\ & V_{\text{SW}} \le \frac{I_{\text{bias}}}{g_{\text{tank}}}, \end{array} \quad (18)$$

where f_0 is the resonant center frequency, P is the consumed dynamic power, N is the phase noise, G is the loop gain, V_{dd} is the power supply voltage, and the minimum or maximum are the upper bound or lower bound of the corresponding specification.

In the LC oscillator design, we consider three variance-linked-to-mean, correlated normal variations in process parameters. They are the relative tank conductance variation $\Delta g_{\text{tank}}/g_{\text{tank}}$, the relative tank capacitance variation

$\Delta C_{\text{tank}}/C_{\text{tank}}$, and the relative inductance variation $\Delta L/L$. Then the design optimization (18) can be formulated as the GP of posynomial form considered in §4.2.1, which can be further reformulated in form of the robust GP (3) to carry out robust design with guaranteed yield bound, as described in §3.3.

In the numerical example, the process parameter values are extracted from the Hitachi 90GHz 0.25μm BiCMOS technology. The design is optimized when the confidence ellipsoid captures 90% of process variations and the center frequency is relaxed within the interval [1.7GHz, 2.5GHz]. Note that the corner cases are defined as the vertices of the regular polyhedron where the ellipsoid used in the robust optimization is inscribed. We compare the robust optimization results with the corner-enumeration optimization results as listed in Table 4. It is shown that the corner-enumeration optimization will incur higher design cost (I_{bias} in this example).

	Optimization with ellipsoidal uncertainty	Optimization using corner enumeration
I_{bias}	2.41mA	2.72mA
C_{tank}	1.33pF	1.26pF
g_{tank}	0.894mS	1.018mS
L	2.83nH	2.82nH
V_{sw}	2.5V	2.5V

Table 4: LC oscillator design results comparison.

We also use the concentric ellipsoids $\mathcal{E}_\gamma$ (13) with various values of γ to capture different percentages of process variations. Design costs (power consumption) of the two optimization schemes will both increase when the yield requirement increases, as compared in Figure 7. For the same yield requirement, the design cost of robust optimization is always lower than that of corner-enumeration optimization. The actual yield of each design is found using 10,000 points in a Monte Carlo analysis. The design cost versus actual yield for the two optimization schemes in compared in Figure 8. It is shown in this example that about 20% overdesign is observed in the corner-enumeration optimization compared with the robust optimization when $\pm 3\sigma$ actual yield is obtained.

6. CONCLUSIONS

In this paper, *optimization with ellipsoidal uncertainty* is proposed to treat the design with variability problem. The statistical variations of the process parameters are captured by a confidence ellipsoid. The linear growth of the problem size is obtained using this formulation. We demonstrate this approach using two examples, in which the robust designs with guaranteed yield bound can be obtained with much less design cost compared with the corner-enumeration optimization.

7. REFERENCES

[1] J. Carballo and S. Nassif. Impact of design-manufacturing interface on SoC design methodologies. *IEEE Design & Test of Computers*, 21(3):183–191, May-June 2004.

[2] S. Director, P. Feldmann, and K. Krishna. Statistical integrated circuit design. *IEEE JSSC*, 28(3):193–202, March 1993.

[3] T. Mukherjeee, L. Carley, and R. Rutenbar. Efficient handling of operating range and manufacturing line variations in analog cell synthesis. *IEEE TCAD*, 19(8):825–839, August 2000.

[4] A. Dharchoudhury and S. Kang. Worst-case analysis and optimization of VLSI circuit performance. *IEEE TCAD*, 14(4):481–492, April 1995.

[5] P. McNamara, S. Saxena, and C. Guardiani *et al.* Design for manufacurability characterization and optimization of mixed-signal IP. In *Proc. IEEE CICC*, pages 271–274, 2001.

[6] M. Hershenson, S. Boyd, and T. H. Lee. Optimal design of a CMOS op-amp via geometric programming. *IEEE TCAD*, 20(1):1–21, January 2001.

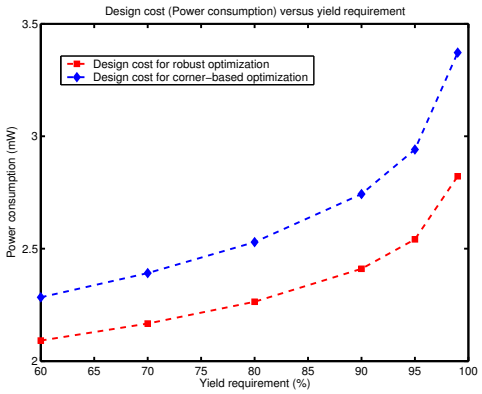

Figure 7: LC Oscillator: design cost versus yield requirement.

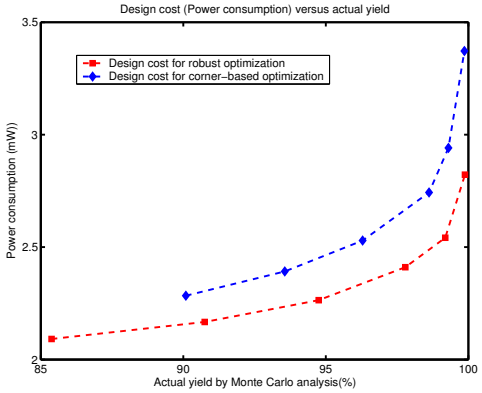

Figure 8: LC Oscillator: design cost versus actual yield.

[7] K.-L. Hsiung, S.-J. Kim, and S. Boyd. Tractable approximate robust geometric programming. Revised for publication in *Mathematical Programming*, April 2005. Available at `http://www.stanford.edu/~boyd/rgp.html`.

[8] S. Nassif. Design for variability in DSM technologies. In *Proc. First Int. Symp. on Quality Electronic Design*, pages 451–454, San Jose, California, March 2000.

[9] A. Ben-Tal and A. Nemirovski. Robust optimization: methodology and applications. *Mathematical Programming Series B*, 92(3):453–480, May 2002.

[10] S. Boyd and L. Vandenberghe. *Convex Optimization*. Cambridge University Press, 2004.

[11] S. Boyd, S.-J. Kim, L. Vandenberghe, and A. Hassibi. A tutorial on geometric programming. Technical report, Electrical Engineering Department, Stanford University, September 2004. Available at `www.stanford.edu/~boyd/gp_tutorial.html`.

[12] W. Daems, G. Gielen, and W. Sansen. Simulation-based generation of posynomial performance models for the sizing of analog integrated circuits. *IEEE TCAD*, 22(5):517–534, May 2003.

[13] M. Hershenson, S. S. Mohan, S. P. Boyd, and T. H. Lee. Optimization of inductor circuits via geometric programming. In *Proc. 36th ACM/IEEE Design Automation Conference*, pages 994–998, June 1999.

[14] M. Romeo, V. Da Costa, and F. Bardou. Broad distribution effects in sums of lognormal random variables. *European Physical Journal*, pages 513–525, May 2003.

[15] K. Chen, C. Hu, P. Fang, M. R. Lin, and D. L.Wollesen. Predicting CMOS speed with gate oxide and voltage scaling and interconnect loading effects. *IEEE Trans. Electron Devices*, 44(11):1951–1957, November 1997.

[16] K. Chen and C. Hu. Performance and V_{dd} scaling in deep submicrometer CMOS. *IEEE JSSC*, 33(10):1586–1589, October 1998.

[17] A. Hajimiri, S. Limotyrakis, and T. H. Lee. Jitter and phase noise in ring oscillators. *IEEE JSSC*, 34(6):790–804, June 1999.