Polarization Multiplexed (D)QPSK InP Receiver Photonic Integrated Circuits

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Abstract: In this paper we review recent developments in the area of receiver photonic integrated circuits for the implementation of polarization multiplexed (differentially coded), quadrature phase shift keying (DQPSK) transmission formats.
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1. Introduction

A large fraction of work done over the last 40 years on InP photonic integration has been for the conventional OOK (on-off keying) modulation format. Fig. 1 shows the progression in the complexity of PIC's to date [1]. Multi-level phase/amplitude modulated transmission formats have been shown to be spectrally more efficient than the conventional OOK format [2]. The receivers for phase modulated signals generally require a local oscillator for detection [2, 3], but those for formats like DQPSK can be implemented with a delay line interferometer [4,5]. We recently reported a 10 channel, 45.6Gbit/s per channel, polarization multiplexed DQPSK, InP receiver PIC [4].

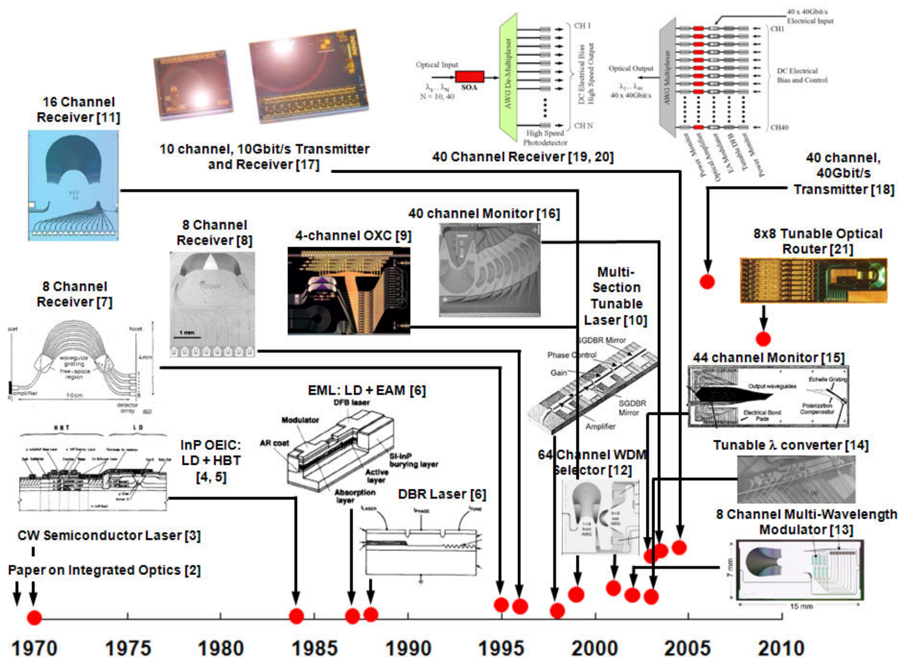

Fig. 1. Historical trend and timeline for complexity in monolithic, photonic integration on InP (Refs next to the devices are from Ref [1]). The vertical scale is linear, and the red filled circles start at 1 and go to 240. The trend shows an exponential growth in PIC complexity in recent years.

2. DQPSK PIC Architecture and Performance

Fig. 2(a) shows the layout of the 10 channel DQPSK receiver PIC that we reported in [4]. The polarization processing block at the input is common to all 10 channels. The input signal is first split into its TE and TM components using a polarization beam splitter (PBS). The TM output of the PBS is then converted to the TE polarization (labeled TE*) using a polarization rotator. The adjacent arm with the original TE component has a variable optical attenuator (VOA) to power balance the two outputs. The TE and TE* outputs are then spectrally demultiplexed using a single AWG (array waveguide grating).

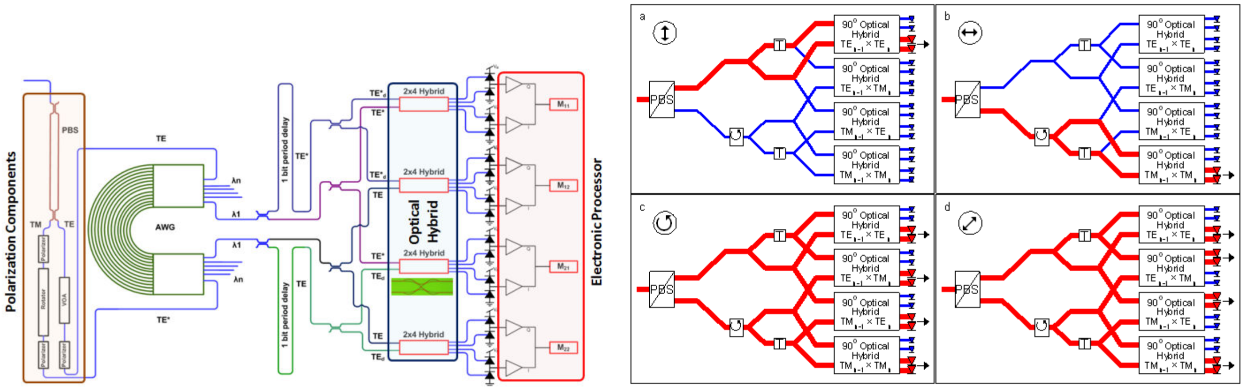

Fig. 2. (a) Polarization multiplexed DQPSK receiver PIC architecture, (b) Implementation of the automatic polrization tracking algorithm

The outputs of the AWG are then fed to the 1-bit delay, optical hybrid network. In the conventional DQPSK decoder the TE and TM components would be separately processed by mixing the original signal with its delayed component (TEd or TMd). In this architecture, we create the following 4 combinations, TE + TEd, TE* + TEd , TE + TE*d and TE* + TE*d. These optical hybrid outputs are then terminated in pairs of high speed photodetectors (PD). The balanced PD pair inputs are 180º out of phase to create a differential signal. The PD outputs are wire bonded to a co-packaged electronic processor ASIC. By performing signal processing, using conventional Least Mean Squares adaptation, on these combinations of the polarization multiplexed incoming signal, we can electronically track the incoming polarization and phase. We do not need any external components for polarization tracking or phase stabilization of the optical hybrid. This significant advantage comes at the expense of doubling the number of PDs required per channel for balanced detection to 16, for a total of 160 PDs for a 10 channel PIC. Details of the polarization tracking algorithm and implementation will be presented during the talk.

Polarization rotators in InP, like ours, are commonly made of asymmetric waveguides [6]. They may also be made of photonic bandgap structures [5]. Fig. 3 shows performance of the polarization rotator. Over the wavelength range shown the TM/TE conversion is well over 90%, typically in excess of 20dB extinction of the unwanted polarization. The insertion loss is less than 0.5dB. Fig. 4 shows the performance of a standalone 2x4 optical hybrid with extinction ratio in excess of 20dB. The optical hybrid, is used to create the 90º phase offset between the I and Q components of the DQPSK signal.

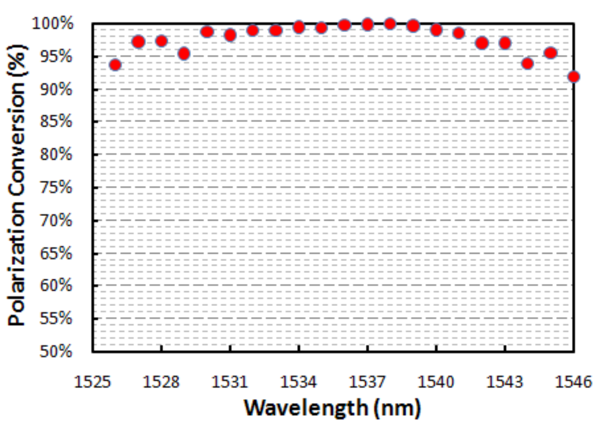

Fig. 3. Performance of the polarization rotator with wavelength.

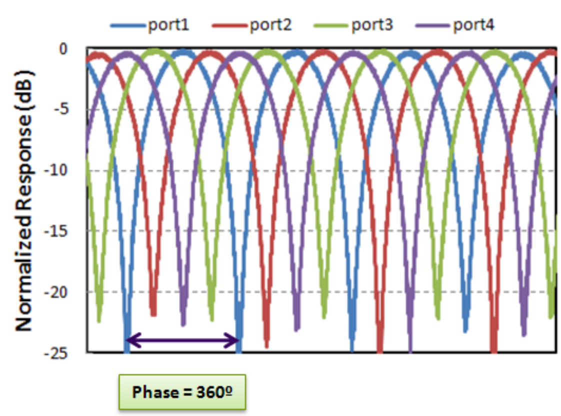

Fig. 4. Performance of standalone optical hybrid test structure.

Fig. 5 shows the S21 response (bandwidth) of the PD. The response of the standalone PD (in a separate test cell) drops only by about 1dB at 20GHz. When the response is measured on the PIC, the result is the characteristic filter response of the 1-bit delay (1-bit delay is biased at the peak of the passband). The electrically measured FSR of the 1-bit delay, 11.4GHz, is in agreement with the optical measurement. Fig. 5 shows the normalized responsivity of the array of 160 PDs. The responsivity measurement is done using a tunable laser source (TLS) first aligned to the TE and then to the TM orientation on PIC. Wavelength sweep of the TLS produces a series of fringes at the PDs. Reported responsivity is the peak value of the composite response at the PD. The total power variation across all channels is within 4dB. This variation has contributions from all the components up to and including the PD's. We can use the VOA, in the TE arm at the input, to achieve power balance between the two input polarizations.

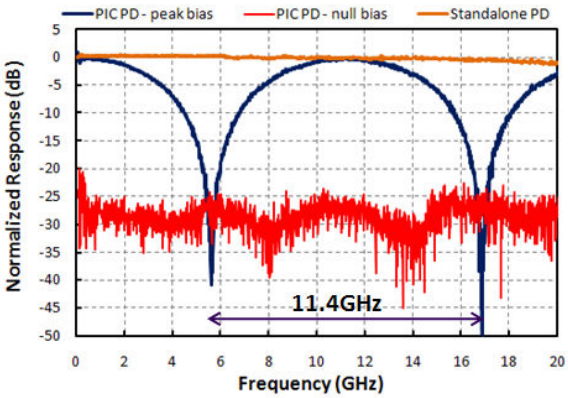

Fig. 5. Power spectral density for the LO.

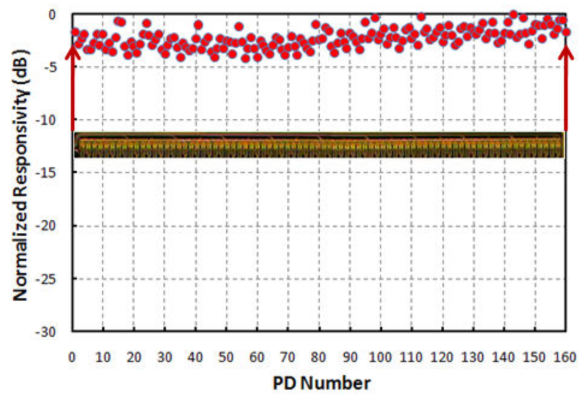

Fig. 6. S21 performance for HSPD.

The PIC and the electronic processor are integrated into a ceramic multi-layer package. The multi-layer design allows complex internal signal and power routings while maintaining good RF signal integrity. The package has an electrical interface providing >1000 I/O connections for data, power and controls, and a single mode fiber input.

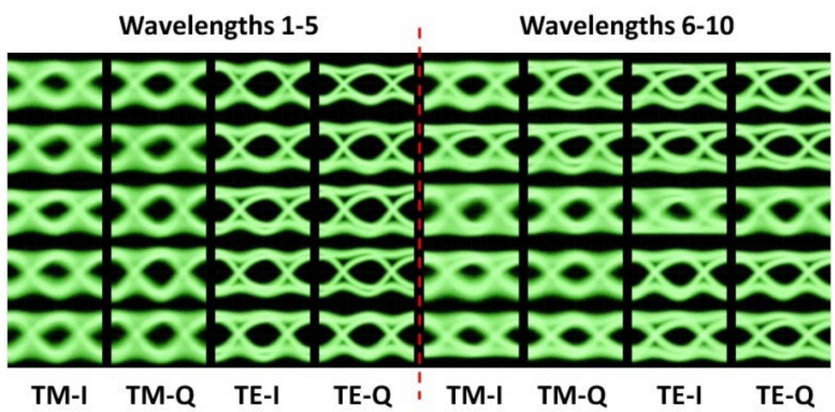

Fig. 7 40, 11.4Gbit/s eye diagrams comprising of the I and Q data for both TE and TM polarizations from a package receiver..

Fig. 7 shows the 40, 11.4Gbit/s eye diagrams of the demodulated DQPSK signal. The BER performance of all the channels is well below the FEC correctable limit. Thus, the package is capable of a total data rate of 456Gbit/s. The module was tested with the TEC nonoperational, i.e., without strict temperature control, and the polarization scrambled at the input. This is possible because the resulting phase variation in the 1-bit delay, and polarization variation at the input were automatically tracked by the electronics.

3. Conclusions

We have demonstrated a InP, 10 channel, PM DQPSK receiver PIC module operating at a data rate of 456Gbit/s without any external components for phase or polarization tracking.

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