Real-Time FPGA-Based Intradyne Coherent Receiver for 40 Gbit/s Polarization-Multiplexed 16-QAM

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Abstract: Real-time detection of a 40 Gbit/s polarization-multiplexed square 16-QAM signal is demonstrated in an FPGA-based intradyne coherent receiver processing 100% of data. A minimum BER of 3.3×10^{-5} is achieved.
OCIS codes: (060.1660) Coherent communications; (060.4510) Optical communications

1. Introduction

As the per-channel bit rate increases to 400 Gbit/s and 1 Tbit/s, multilevel modulation formats such as 16-ary quadrature amplitude modulation (16-QAM) gain increasing attention [1]. But in order to achieve a complete and precise understanding of the performance of the required digital signal processing (DSP), it is crucial to evaluate the corresponding algorithms using real-time prototypes [2]. This is the only way to measure low bit error rates (BER), to investigate dynamic effects and to capture rare events. In addition the hardware implementation of the receiver algorithms allows for a much more precise evaluation of resource requirements as well as latencies and their impact on the performance.

While real-time receiver implementations for quadrature phase shift keying (QPSK) and orthogonal frequency division multiplex (OFDM) have already been studied in detail [3,4], only one real-time implementation of a single-polarization DSP-based intradyne coherent receiver for 16-QAM has been reported [5]. Other experiments carried out so far used either offline processing or pilot-based phase noise cancellation techniques [1,6].

In this paper we report the implementation of a real-time FPGA-based coherent intradyne receiver for polarization-multiplexed 16-QAM transmission. The achieved symbol rate is 5 Gbaud, which corresponds to a data rate of 40 Gbit/s.

2. Polarization-multiplexed 16-QAM transmission system

The setup of the 40 Gbit/s 16-QAM transmission system is shown in Fig. 1. Two four-level drive signals are generated using an arbitrary waveform generator (AWG). The signals are determined using four copies of a binary pseudo-random bit sequence (PRBS) of length 2^{15}-1, which are mutually delayed by 225 bits. Two sequences are considered as most significant bits (MSB_I and MSB_Q), are differentially encoded and define the quadrant of the square 16-QAM constellation. The other two sequences are considered the least significant bits (LSB_I and LSB_Q) and are used without further encoding to select the inphase and quadrature amplitude levels within the quadrant. Equalization is added to the resulting waveform to compensate for low-pass effects in the transmitter and for the nonlinear transfer function of the modulator. The eye diagram of the four-level drive signal is shown in Fig. 1.

The two AWG output signals are amplified and applied to a $LiNbO_3$ Mach-Zehnder (I/Q) modulator. As light source a tunable external cavity laser (ECL) with a power of 12 dBm and specified linewidth of 100 kHz is used.

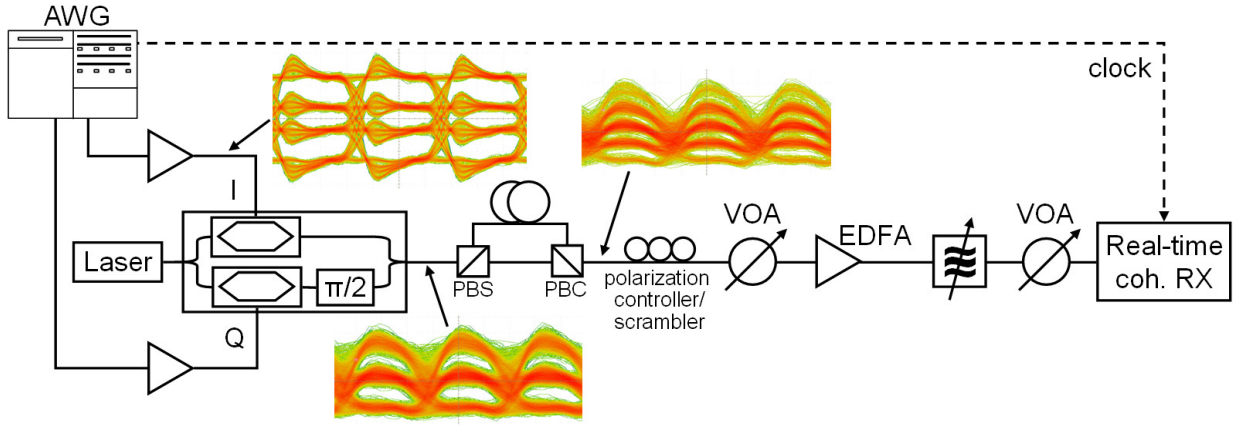

Fig. 1: Polarization-multiplexed 16-QAM transmission system

The 5 Gbaud 16-QAM optical intensity eye diagram with its three intensity levels corresponding to the three rings that make up a square 16-QAM constellation is also shown in Fig. 1. Polarization division multiplexing (PDM) is achieved by splitting the modulator output signal using a polarization beam splitter (PBS), delaying one branch, and recombining the two branches in a polarization beam combiner (PBC). The intensity eye diagram of the resulting 40 Gbit/s polarization-multiplexed 16-QAM signal is depicted in Fig. 1.

The transmitter output signal is passed through a polarization scrambler, a variable optical attenuator (VOA) and is amplified in an erbium doped fiber amplifier (EDFA). An additional VOA following the EDFA and a manual polarization controller are used to control the signal power and state of polarization (SOP) entering the opto-electronic receiver frontend, respectively. There the signal is combined with a local oscillator (LO) laser in a polarization diversity 90-degree optical hybrid. The LO is the same type of ECL as used at the transmitter, and is tuned within approximately ±50 MHz of the received signal's center frequency. The outputs of the hybrid are detected in four single-ended photodiodes, which are connected through amplifiers to the analog-to-digital converters (ADC). The ADCs sample the input signals with 10 Gs/s (*T*/2-spaced sampling) at a nominal resolution of 8 bits. Due to the lack of a clock recovery circuit the transmitter clock is used to clock the receiver. The receiver frontend has a measured 3-dB bandwidth of ~3 Ghz. The two ADCs of each polarization are interfaced with a Xilinx Virtex 5 field programmable gate array (FPGA), in which frontend equalization and IQ correction are performed. The two FPGAs then pass their data to a third identical FPGA, in which polarization control, intermediate frequency (IF) compensation, carrier recovery, data decoding, and bit error counting are implemented. The 3 FPGAs are connected to a personal computer (PC), which calculates the BER and provides a user interface to the receiver.

3. Real-time digital signal processing

The FPGAs process 100% of the 40 Gbit/s data stream and operate with a core clock frequency of 156.25 MHz. Therefore 64 parallel channels are required in FGPA-1 and -2 to process the received symbols. The first step in signal processing is frontend equalization. After removing a possible offset, the data from each ADC is passed through a real-valued 15 tap finite impulse response (FIR) filter to compensate for the low-pass behaviour of the frontend [7]. Then the signal is fed into an IQ correction block, which compensates imperfections of the 90-degree hybrid by minimizing the cross-correlation between the real and imaginary part [8]. Then the data from FGPA-1 and -2 is passed on to FPGA-3.

Due to resource limitations FPGA-3 cannot operate on the oversampled data. Therefore FPGA-3 downsamples the data to 1 sample/symbol, which requires only 32 parallel channels. First the two polarizations are separated using a single tap butterfly filter. The filter coefficients are updated using the standard constant modulus algorithm (CMA) [8]. Again due to resource limitations only one polarization is processed after polarization control. Which polarization to process can be switched through the PC user interface. Then the DSP compensates for the constellation rotation caused by the frequency mismatch between signal and LO laser. As the IF varies rather slowly its estimate can be updated using a feedback algorithm with an integral controller. The differential phase between subsequent symbols is used as error signal. The carrier phase is recovered in a feed-forward structure, using the QPSK partitioning algorithm with sliding window averaging and a filter width of 31 symbols [9].

After data recovery and differential decoding of MSB_I and MSB_Q, all 4 recovered bit streams are fed into bit error counters. The measurement inside the FPGA enables the monitoring of all 4 bit streams in parallel, i.e. all received bits are considered for error counting. The measured bit error numbers are read by the personal computer (PC), in which the BER is calculated.

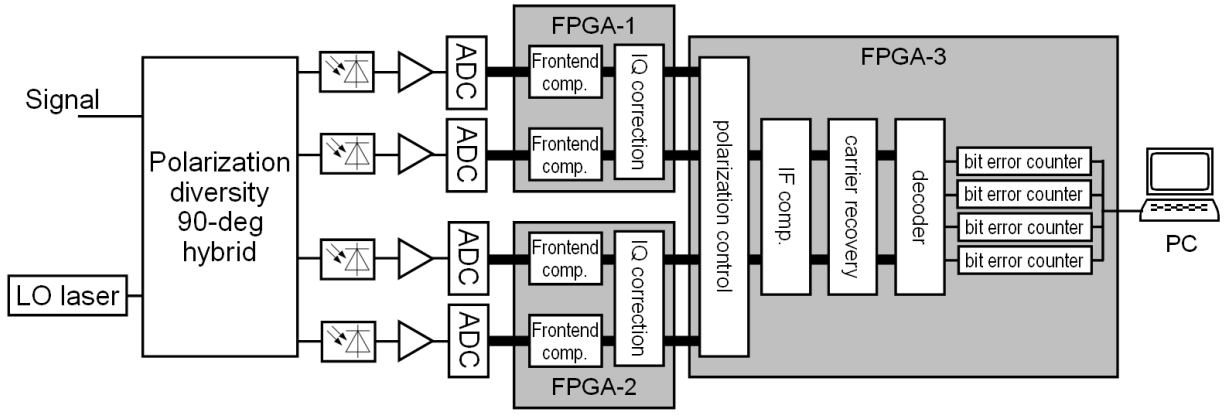

Fig. 2: Coherent receiver frontend and real-time digital signal processing

4. Real-time 16-QAM measurement results

In a first experiment only one polarization is transmitted, the polarization scrambler is switched off, and the SOP is manually adjusted to be aligned with either the x-polarization or the y-polarization of the receiver. In FPGA-3 the polarization control is bypassed, i.e. only IF compensation and carrier recovery are active. The measurement results are depicted in Fig. 3. Both polarizations show a very similar performance and exhibit an error floor at $BER_x = 1.6\times10^{-5}$ and $BER_y = 2.1\times10^{-5}$. The required OSNR for a $BER = 2\times10^{-3}$ is 15dB. From the input constellations (insets in Fig. 3) it can seen that the receiver performance suffers from common mode noise. This is a major limitation of the current setup. The replacement of the single-ended by differential photodetectors can resolve this problem and improve the performance.

In a second experiment the polarization scrambler is turned on (scan rate 8) and the polarization control in the FPGA is enabled. Fig. 4 shows the results for single polarization transmission with static SOP (polarization control disabled) and scrambled SOP (polarization control active), as well as PDM transmission. The receiver sensitivity for single polarization transmission slightly improves by 0.3dB when the polarization control is enabled. This is related to the fact that the CMA not only separates the polarizations, but also compensates for residual amplitude differences between the real and imaginary part of each polarization. For PDM transmission a small excess penalty of 0.4dB beyond the 3dB expected penalty is observed. This might be due to residual polarization crosstalk, as no special 16-QAM adaptation of the CMA was implemented in the receiver.

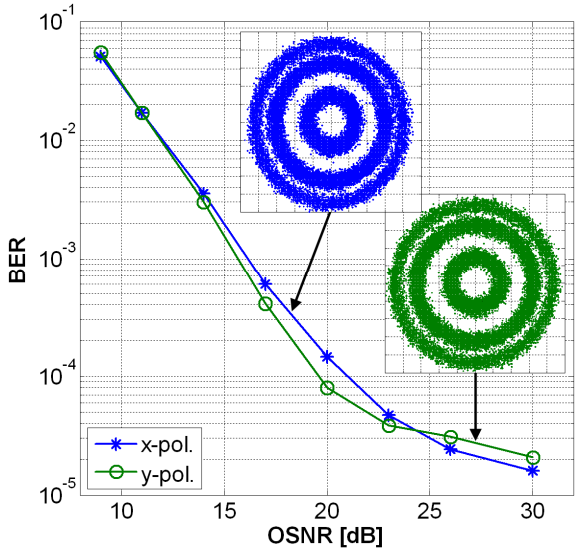

Fig. 3: BER vs. OSNR for single polarization transmission manually adjusted to x- and y-polarization.

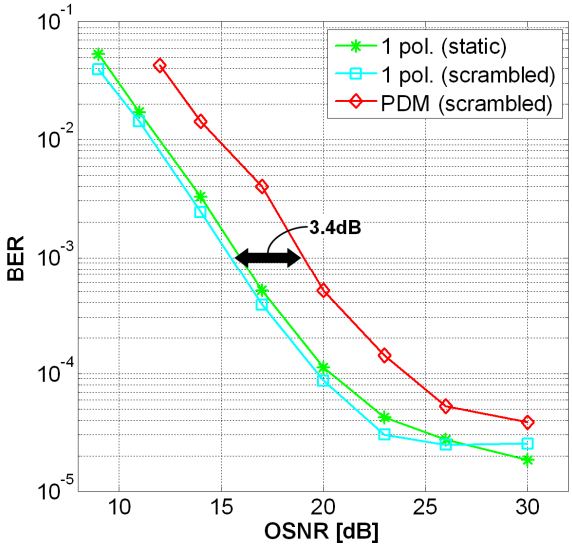

Fig. 4: BER vs. OSNR for single polarization and PDM transmission with static or scrambled SOP.

4. Summary

We have implemented a 5 Gbaud real-time FPGA-based intradyne coherent receiver for optical PDM 16-QAM transmission. At the data rate of 40 Gbit/s the minimum BER in back-to-back transmission is 3.3×10^{-5}, and the required OSNR for a BER of 2×10^{-3} is 18.4 dB.

5. References

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