Fully CMOS Compatible Subwavelength Plasmonic Slot Waveguides for Si Electronic-Photonic Integrated Circuits

Shiyang Zhu, T. Y. Liow, G. Q. Lo, and D. L. Kwong
*Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), 11 Science Park Road, Science Park II, Singapore 117685, Email: zhusy@ime.a-star.edu.sg*

Abstract: Subwavelength horizontal Al/SiO_2/Si/SiO_2/Al plasmonic slot waveguides with SiO_2 width at each side of ~15 nm and Si width of ~136, ~87, and ~43 nm are fabricated on SOI substrates using fully CMOS compatible processes. The propagation losses at 1550 nm TE are ~1.01, ~1.31, and ~1.56 dB/μm, respectively, as measured by the standard cutback method. A simple taper coupler with length of ~0.3–1 μm provides a high coupling efficiency of ~66%–79% between the plasmonic slot waveguide and the standard Si dielectric waveguide. The plasmonic slot waveguide can achieve a direct 90° bend with a very low bending loss of ~0.2–0.4 dB. The propagation, coupling, and bending losses depend weakly on wavelength in the c-band. The results demonstrate the potential for seamless integration of functional plasmonic devices in existing Si electronic-photonic integrated circuits.
OCIS codes: (250.5403) Plasmonics; (230.7370) Waveguides; (250.5300) Photonic integrated circuits.

1. Introduction

Plasmonic waveguides can spatially confine light below the diffraction-limit, thereby potentially enabling to bridge the dimension mismatch between the photonic devices and electronic devices in current Si electronic-photonics integrated circuits (EPICs) [1]. A fundamental limitation of the various plasmonic waveguides proposed so far is the tradeoff between the light confinement and the propagation distance [2]. Theoretically, it was argued recently that hybrid plasmonic waveguides (or metal/multi-insulator/metal waveguides) may provide a longer propagation distance than the metal/insulator/metal waveguides with the same light confinement [3-5]. Experimentally, Au (which is not a CMOS compatible material at present) is commonly adopted as the metal and a special process (such as electron beam lithography) is usually required to fabricate the nanoscale plasmonic devices [6-8]. In the view of practical implementation in the existing Si EPICs, it is highly desirable to use the CMOS compatible metal (e.g., Al or Cu) and industry-standard lithographic processes. Here, we present the first experimental realization, to our best knowledge, of horizontal Al/SiO_2/Si/SiO_2/Al plasmonic slot waveguides, as well as taper couplers and bends, using fully CMOS compatible processes. The demonstrated plasmonic waveguides pave the way to highly functional plasmonic integrated circuits.

2. Waveguide fabrication and measurement

The plasmonic waveguides were fabricated on SOI substrates with a 340-nm-thick top Si layer and a 2-μm-thick buried SiO_2 layer. After 50-nm-thick SiO_2 deposition, the waveguide patterns, including the Si core for the plasmonic slot waveguides (with various lengths (L_p) and widths (W_p)) and the taper couplers (with various taper lengths ($L_{coupler}$)), as shown schematically in Fig. 1(a), were defined by 248-nm deep UV lithography, followed by SiO_2 dry etching, photoresist striping, and Si dry etching down to the buried SiO_2. The Si waveguide has an identical width (W_{Si}) of 500 nm. A direct 90° bend is also designed, as shown in Fig. 1(b). The SEM images after this step are shown in Figs. 1(c) and (d). After a 50-nm-thick SiN layer and a 700-nm-thick SiO_2 layer deposition, windows were opened (the dashed rectangles in Figs. 1(a) and (b)) by dry etching SiO_2 down to the SiN layer, followed by the SiN wet etching. Fig. 1(e) shows the SEM image after this step. One wafer was thermally oxidized whereas the other wafer was not. Then, a 700-nm-thick Al layer was deposited, followed by dry etching of Al outside the plasmonic device area (i.e., the solid rectangles in Figs. 1(a) and (b)). Finally, a 1-μm-thick upper cladding SiO_2 was deposited, followed by a deep trench etching for the Si waveguide facet preparation and wafer dicing. Fig. 1(f) shows the SEM image of the final structure. Figs. 1(g), (h) and (i) show the cross sectional TEM images of the Al/SiO_2/Si/SiO_2/Al waveguides. The height of the Si core is ~340 nm, the sidewall oxide thickness is ~15 nm, and the Si core widths at the middle of the height are ~136, ~87, and ~43 nm, respectively. These three plasmonic waveguides are referred as PWG1, PWG2, and PWG3 hereafter. The other wafer has the same structures but without the thermal SiO_2 layer. A Si waveguide without the plasmonic structures is used as the reference waveguide. The devices were measured by coupling TE-polarized light from a tunable laser to the input silicon waveguide and measuring the transmitted power in the output silicon waveguides using a semi-auto XYZ micrometer piezo-stage for precision alignment.

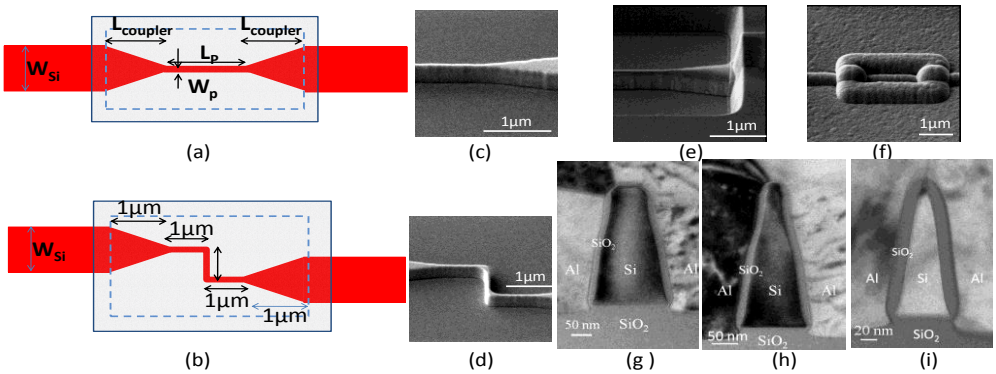

Fig. 1 (a) and (b) Layouts of straight and bend plasmonic slot waveguides which are inserted in the 500-nm-wide standard Si waveguide; (c) and (d) SEM images after the Si dry etching; (e) SEM image after the SiO_2 window opening for Al filling; (f) SEM image of the final structure; (g), (h) and (i) are cross-sectional TEM images of the plasmonic slot waveguides with various Si core widths. They are referred to PWG1, PWG2, and PWG3, respectively.

3. Results and discussion

Figs. 2(a) and (b) show the field distributions for the major component $E_x(x,y)$ of the quasi-TE fundamental mode in the 340-nm-high Al/Si(100 nm)/Al and Al/SiO_2(15 nm)/Si(100 nm)/SiO_2(15 nm)/Al plasmonic waveguides obtained from the 3D FDTD simulation. As expected, the modal power is greatly confined in the thin SiO_2 layer, and accordingly, the effective modal index decreases from 3.86 to 2.32 and the propagation loss decreases from 2.72 to 1.15 dB/μm with the thin SiO_2 layer incorporation. Fig. 2(c) shows the measured transmitted powers at 1550 nm (TE) for waveguides with L_p = 1, 2, 3, 5, 10, 20, and 50 μm and L_{taper} = 1 μm. For the Al/SiO_2/Si/SiO_2/Al waveguides, the transmitted power (dBm) exhibits a good linearity with L_p ranging from 1 to 20 μm, from which the propagation losses are extracted to be ~1.01, ~1.31, and ~1.56 dB/μm for PWG1, PWG2, and PWG3, respectively. The values are in good agreement with that predicted from the FDTD simulation and the measured value of ~0.8 dB/μm for the Au/Si(150 nm)/Au waveguide [6]. The 50-μm-long plasmonic waveguide has the transmitted power of ~-50 – ~-60 dBm, which may arise from light leaking through the bottom SiO_2 layer, as revealed in Fig 2(b). Moreover, if the TM light is launched, the transmitted powers are in the range of ~-32 – ~-60 dBm, and do not exhibit a clear linear dependence on L_p (not shown here), in agreement with the fact that only the TE light can excite the plasmonic mode in horizontal plasmonic slot waveguides. The Al/Si/Al waveguides, to our surprise, exhibit much smaller transmitted powers than those predicted from the FDTD simulation, and the transmitted power does not depend on L_p linearly, making it impossible to extract accurate propagation losses. We suspect that the probable Al-Si reaction at the Al/Si interface may block the plasmonic mode excitation and/or cause a very large light absorption. Hereafter, only the Al/SiO_2/Si/SiO_2/Al waveguides are investigated. Fig. 2(d) depicts the wavelength dependence of propagation losses in the c-band (1520–1620 nm) for PWG1, PWG2, and PWG3. The weak wavelength dependence makes the plasmonic waveguides suitable for wavelength multiplexing.

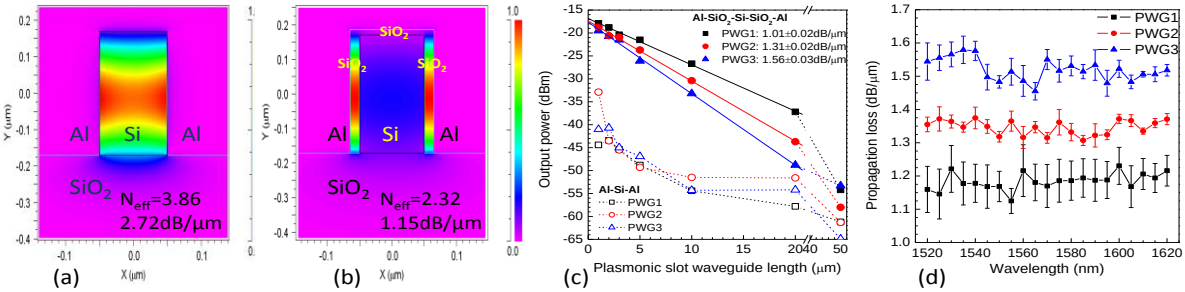

Fig. 2 (a) and (b) The calculated $E_x(x,y)$ distributions of the quasi-TE fundamental mode in the Al/Si(100 nm)/Al and Al/SiO_2(15 nm)/Si(100 nm)/SiO_2(15 nm)/Al plasmonic slot waveguides; (c) the measured transmitted power at 1550 nm (TE) with a function of the plasmonic waveguide length for Al/SiO_2/Si/SiO_2/Al and Al/Si/Al waveguides; (d) Propagation losses extracted from the linearly fitting as a function of the wavelength, the fitting standard deviation is depicted as the error bar.

The light in the standard Si dielectric waveguide can be effectively coupled in and out of the plasmonic waveguide through a simple taper coupler. Fig. 3(a) plots the top-view E_x-field distribution from 3D FDTD simulation for 1550-nm TE light coupling from a 500-nm-wide Si waveguide to the Al/SiO_2(15 nm)/Si(100nm)/ SiO_2/Al waveguide through a 1-μm-long coupler, showing power launched in the Si waveguide is gradually transferred and concentrated in the thin SiO_2 layer of the plasmonic slot waveguide. Fig. 3(b) plots the corresponding side-view field distribution, showing the light propagation from the Si waveguide to the plasmonic

waveguide through the taper coupler. To determine the coupling loss experimentally, we subtract the transmitted power measured from the reference waveguide (~14 dBm) and the propagation loss through the 3-μm-long plasmonic waveguide from the transmitted power measured from the waveguide with L_p=3 μm and $L_{coupler}$ ranging from 0.3 to 2 μm, and then divide by 2. The results are depicted in Fig. 3(c), in good agreement with the FDTD simulation results. We can see that the taper coupler with $L_{coupler}$ of 0.3–1μm provides a low coupling losses of ~-1 – ~1.8 dB. The longer coupler exhibits a larger coupling loss because of the predominant propagation loss along the coupler. Fig. 3(d) depicts the wavelength dependence of coupling loss through the 1-μm-long couplers, showing weak wavelength dependence in the c-band.

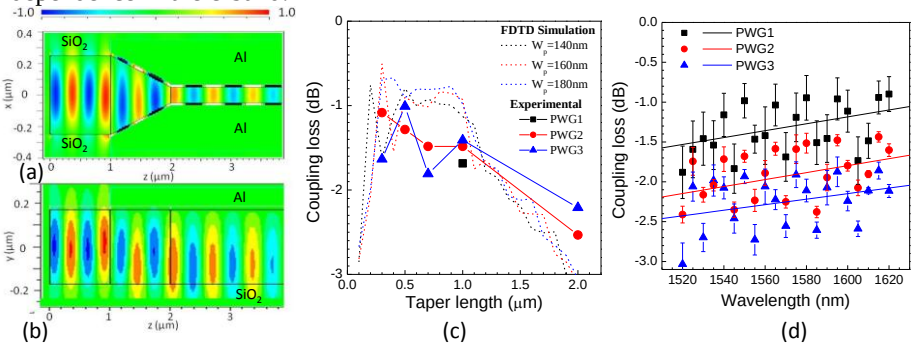

Fig. 3 (a) Top-view and (b) side-view of the calculated $E_x(x,y)$ distributions for 1550-nm TE light laughed from the 500-nm-wide Si waveguide at the left coupling to the Al/SiO_2(15 nm)/Si(100 nm)/SiO_2(15 nm)/Al plasmonic waveguide at the right through a 1-μm-long taper coupler. (c) The measured and calculated coupling loss per coupler as a function of the coupler length. (d) Wavelength dependence of coupling loss between the 500-nm-wide Si waveguide and PWG1, PWG2, or PWG3 through a 1-μm-long taper coupler.

Theoretically, the nanoscale plasmonic slot waveguide can achieve an ultracompact bend with low loss. The 3D FDTD simulation predicts that a direct 90° bend has the pure bending loss (i.e., after subtracting the propagation loss) of ~0.2 dB, as shown in Fig. 4(a). Experimentally, the bend structures with the total plasmonic waveguide length of 3 μm are fabricated, as shown in Fig. 1(b). The pure bending loss is deduced by subtracting the measured transmitted power to that measured from the waveguide with the 3-μm-long straight plasmonic waveguide, and then divided by 2. The deduced pure bending losses are shown in Fig. 4(b) as a function of wavelength. The bending losses also exhibit almost wavelength independent within the measurement uncertainty. The averaged bending loss amounts to ~0.2–0.4 dB for PWG2 and PWG3, in a good agreement with that predicted from the FDTD simulation.

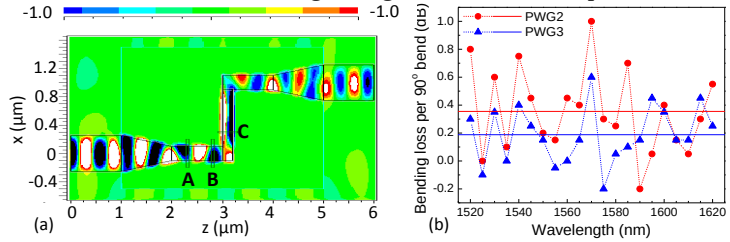

Fig. 4 (a) Top-view of the calculated $H_y(x,y)$ distributions in Al/SiO_2(15 nm)/Si(100 nm)/SiO_2(15 nm)/Al slot waveguides with two direct 90° bends, the pure bending loss of ~0.2 dB is deduced from the powers monitored at A, B and C points. (b) The measured pure bending loss of a direct 90° bend as a function of wavelength for PWG2 and PWG3.

4. Conclusions

Horizontal Al/SiO_2/Si/SiO_2/Al plasmonic slot waveguides, which are inserted in the standard Si waveguides, are fabricated using fully CMOS compatible processes for the first time. The measured results (propagation loss, the coupling loss, and the bending losses) are in good agreement with those predicted from the 3D FDTD simulation, and also are comparable to those fabricated using Au. The results pave the way to seamless integration of functional plasmonic devices in the existing Si EPICs using fully CMOS compatible materials and processes.

[1] W. L. Barnes, A. Dereux, and T. W. Ebbesen, "Surface plasmonic sub-wavelength optics", Nature **424**, 824-830 (2003).
[2] A. V. Krasavin and A. V. Zayats, "Silicon-based plasmonic waveguides", Optics Express **18**, 11791-11799 (2010).
[3] R. F. Oulton, et al, "A hybrid plasmonic waveguide for subwavelength confinement and long-range propagation", Nat. Photonics **2**, 496-500 (2008).
[4] M. Z. Alam, et al., "Propagation characteristics of hybrid modes supported by metal-low-high index waveguides and bends", Optics Express **18**, 12971-12979 (2010).
[5] D. Dai and S. He, "Low-loss hybrid plasmonic waveguide with double low-index nano-slots", Optics Express **18**, 17958-17966 (2010).
[6] L. Chen, J. Shakya, et al, "Subwavelength confinement in integrated metal slot waveguide on silicon", Opt. Lett. **31**, 2133-2135 (2006).
[7] Z. Han, et al, "Experimental realization of subwavelength plasmonic slot waveguides on a silicon platform", Opt. Lett. **35**, 502-504 (2010).
[8] D. J. Dikken, et al "Characterization of bending losses for curved plasmonic nanowire waveguides", Optics Express 18, 16112-16119 (2010).