Compact, Thermally-Tuned Resonant Ring Muxes in CMOS with Integrated Backside Pyramidal Etch Pit

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Abstract: We present add-drop filters manufactured as ring resonators in commercial 130 nm SOI CMOS technology with thermal tuning. Their thermal impedance has been dramatically increased by the selective removal of the substrate resulting in a 20,12x increase in tuning efficiency for 100, 30 micron radius device.
OCIS codes: (130.3120) Integrated optics devices; (230.5750) Resonators; (230.7370) Waveguides

1. Introduction

Silicon on Insulator (SOI) based photonics continue to gain interest in computing system applications owing to the prospects of bringing optics close to the processor chip [1]. Compared to traditional electrical signaling, silicon photonics offers lower latency, higher bandwidth and potentially ultra low power consumption. Si photonic devices can be wafer scale produced on an SOI platform using established CMOS manufacturing practices at high yield and low cost. Furthermore, a WDM point-to-point communication network can be constructed with Si photonic components (MUX /DEMUX and modulators) linking a number of CPU cores and scaling up computing system performance with minimal consumed energy [2]. These devices are based on the resonant effects when built around a waveguide ring in SOI technology. Very compact sizes and low energy per bit have been accomplished in modulating ring resonators for data signaling however the power to tune its resonance to match a laser located on an external ITU grid can be substantially higher [1]. Significant improvements in tuning efficiency as well as a reduction in manufacturing errors for variants in resonators from both the SOI platform and the nanofabrication process modules remain a challenge for this technology. We review the current state of the art for each of these technologies in our presentation.

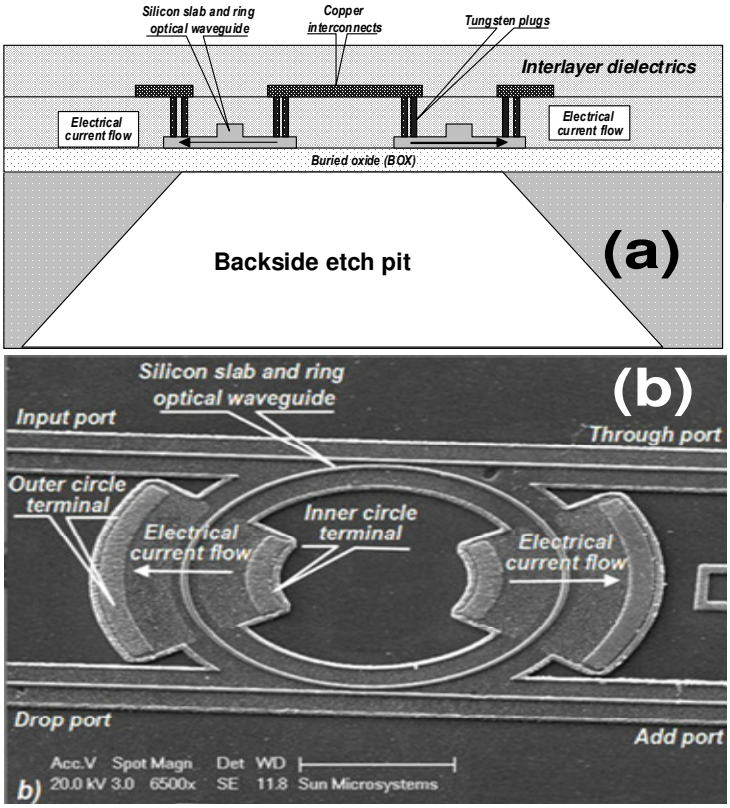

Fig. 1. Thermally tunable resonant waveguide structures: (a) schematic cross-section, (b) SEM image of the silicon waveguide ring with 24 μm diameter and its bus waveguides without the metal interconnects and interlayer dielectrics.

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2. Results and discussion

Recently, we demonstrated a 20X increase in the tuning efficiency for microphotonic add-drop filters manufactured as a 100µm radius ring resonator in a commercial 130 nm SOI CMOS technology by co integrating a back side pyramidal etch pit in the SOI substrate [3]. It's thermal impedance has been dramatically increased because of the selective removal of the SOI Silicon substrate under the device footprint using a bulk silicon micromachining process. Fig. 1 shows the cross section and layout for the device built on a CMOS SOI platform. Several questions remain unresolved with this new device approach that stem from whether it can scale to small device footprint. Additionally, at smaller geometries the device may become mechanically unstable and structurally warp causing their high finesse to be compromised. Finally, can the tuning performance enhancements observed in the 100µm ring continue as the ring miniaturizes. To address scaling these performance questions to smaller device footprint we have integrated a backside etch pit into a 30 and 20 µm radius rings in the same MUX geometry and CMOS node. Fig. 2 illustrates measured tuning performance before and after the backside pit integration for the 30µm radius ring filter. The tuning efficiency in Fig. 2 is 27 mW/nm for the unetched 30µm ring and improves to 2.3mW/nm after the cointegration of the backside etch pit. This equates to a 12X improvement in tuning efficiency as a direct result of the new, but smaller device geometry. When comparing the unetched filters tuning efficiency from our previous result for the 100µm radius ring (83mW/nm) to Fig. 2 performance (27mW/nm) we confirm an inverse dependence for the tuning efficiency versus ring radius that we reported earlier [3]. On the other hand the tuning efficiency improvement before and after the cointegration process is observe to be different as (20, 12)X for the (100, 30)µm radius devices respectively. One difference in scaling tuning enhancement versus ring radius is due in part to the amount of Si substrate beneath the buried oxide removed during the cointegration process (or more specifically on the size of the etch pit beneath the ring). The ratio of etch pit opening area to ring diameter is different in the two cases. This ratio is (30, 10, 5) for the (100, 30, 20) radius devices, respectively. Such an effect is indeed expected because the etch pit disrupts the amount of heat spreading in the Si substrate beneath the buried oxide and correspondingly changes the thermal impedance and hence the wavelength shift per unit of applied power. Nevertheless, as we show here, the measured improvement continues to be significant for 30µm radius rings (shown above) and for even smaller rings (e.g. 20µm radius to be reported at the meeting).

A second characteristic of the cointegration process of interest here is the change in quality factor, Q, associated with our new device geometry. As shown in Fig. 1 the ring sits on a thin membrane of SiO2 that acts as an ideal etch stop layer to the pitting process module. There remains

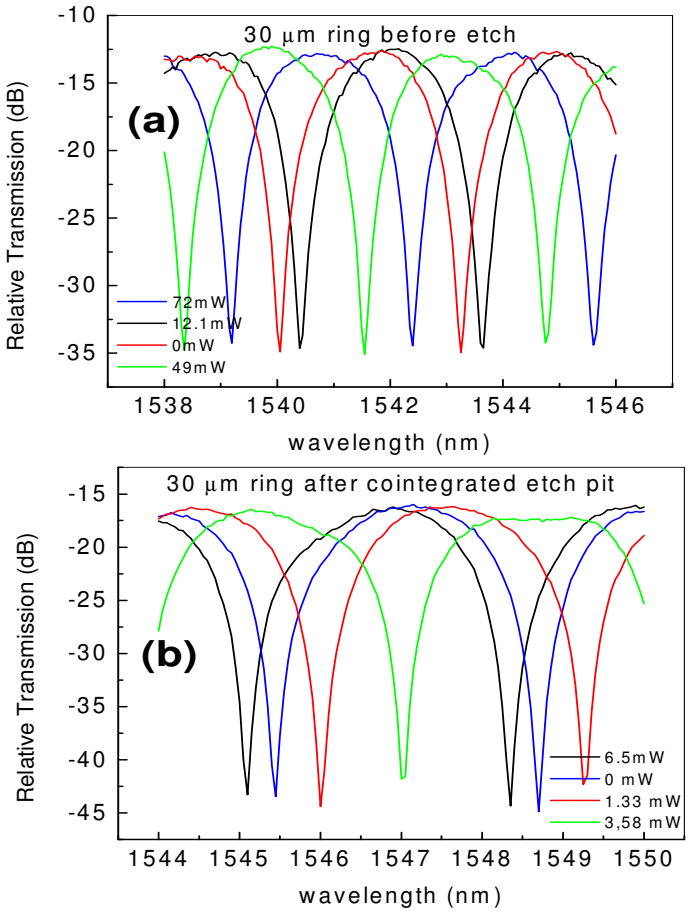

Fig. 2. Spectral response versus applied power before (a) and after (b) etching a 30µm ring.

the question of stresses from the SOI platform; the CMOS process module for Freescale 130nm node and our coinegration etch pit process that could spoil its high fidelity response. Inhomogenity causes added loss and associated linewidth broadening that may only develop at small radius. Under more serious imperfection. the clockwise and counterclockwise mode propagation can lead to splitting detected in TE guided ring geometers as the structure in Fig 1 supports. In Fig. 3 we report the lineshape measured before and after the etched filter response. No change in Q is observed before and after etching for the 100, 30, 20μm rings. Thus our device geometry proves to be fully CMOS compatible. In addition, no detectable degradation in Q can be observed due to structural non uniformities associated with our approach when shrinking the device down 5X in ring radius. Additionally, a number of performance scaling observations have also been deduced from our measurements. First the measured tuning efficiency is observed to be fitted well by an inverse dependence on the device radius for un-etched rings. The amount of power to tune a ring filter across one unit of a Free Spectral Range is independent of the device radius. Also, the improvement in tuning performance upon co-integrating a backside pyramidal pit depends sub-linearly with the size of the pit opening. Finally, we compare our results versus best in class records for tuning ring filters. We classify tuning performance depending upon the heater geometry (direct versus indirect) , the type of waveguide and whether the devices integrate a CMOS dielectric stack up atop the ring.

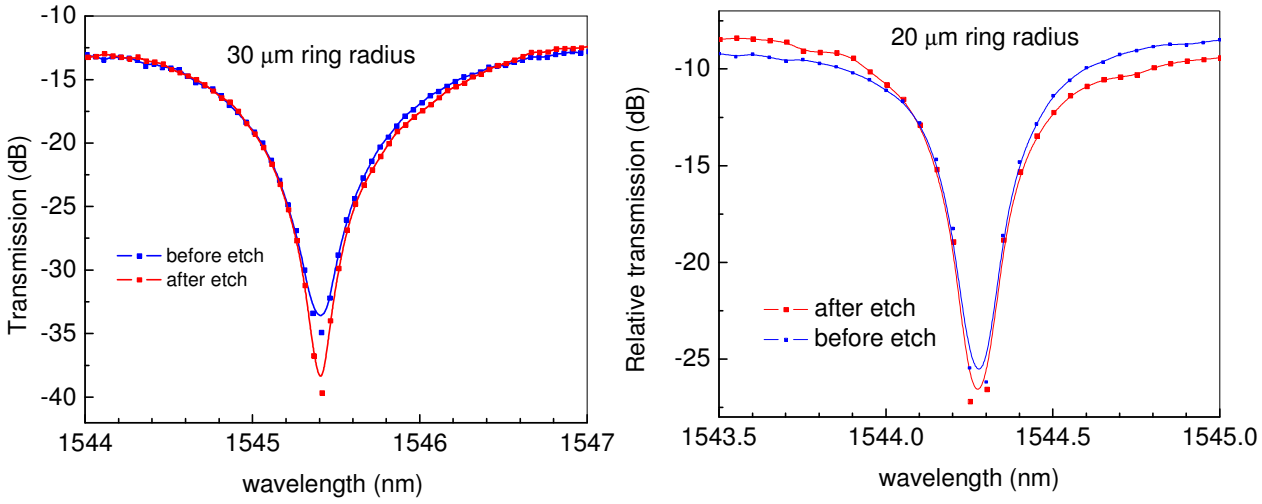

Fig. 3 Transmission versus wavelength before / after cointegration of a backside pyramidal pit.

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