Recent Progress on Real-Time DSP for Direct Detection Optical OFDM Transceivers

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Abstract: We describe recent developments in real-time digital signal processing for direct detection optical OFDM transceivers, including the optimization of high throughput FFT algorithms and receiver synchronization.
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1. Introduction

Optical orthogonal frequency division multiplexing (OFDM) is an attractive candidate for future high capacity optical transmission systems, due to its high spectral efficiency and resilience to fiber dispersion [1]. The continuing growth in digital signal processing (DSP) power, and the development of high-speed signal converters [2, 3], enable the implementation of multi-gigabit per second OFDM. Both direct detection- and coherent-optical OFDM (DDO-OFDM and CO-OFDM) have been investigated in many promising theoretical and experimental studies, e.g. [1, 4]. However, in the majority of experimental work to date, the DSP at both transmitter- and receiver-side has been carried out off-line using software, with high speed arbitrary waveform generators and digital sampling scopes being used for D/A and A/D signal conversion. To rigorously validate the optical OFDM technique, and to evaluate its feasibility for commercial implementation, experimental demonstrations of systems carrying out the signal processing in real time are critical. To this end, a number of groups have recently published work on the construction and testing of real-time OFDM transmitters and receivers [5-11, 13, 16].

This paper summarizes progress made in this area, and identifies some key challenges that are being addressed: optimization of the high throughput (inverse) fast Fourier transform algorithms used to multiplex and demultiplex the sub-channels, real-time receiver synchronization and the design of low cost, low power application specific integrated circuit (ASIC) based transceivers. The paper will mainly focus on direct detection optical OFDM systems, which offer a reduction in hardware complexity in comparison to coherent systems, though at the expense of lower performance, and which may offer a good cost versus performance trade-off in some long-haul, access and multi-mode fiber-based interconnect applications.

2. Summary of real-time optical OFDM experiments

To date, FPGAs, rather than ASICs, have been used to demonstrate real time signal processing for optical OFDM due to the lower cost, shorter development times and the possibility to rapidly reconfigure the design [12]. One of the earliest demonstrations of a real-time DDO-OFDM transceiver, and subsequent developments of this system, reported in [5, 6], were based on Altera Stratix II FPGAs, with DAC/ADC sampling rates of up to 4 GS/s and aggregate bit-rates of up to 11.25 Gb/s, using higher-order modulation formats (64-QAM) The system demonstrated pilot subcarrier-assisted channel estimation [5], achieved a spectral efficiency of 5.625 b/s/Hz and transmission over 25 km of SMF with a BER of 10^{-3} [6].

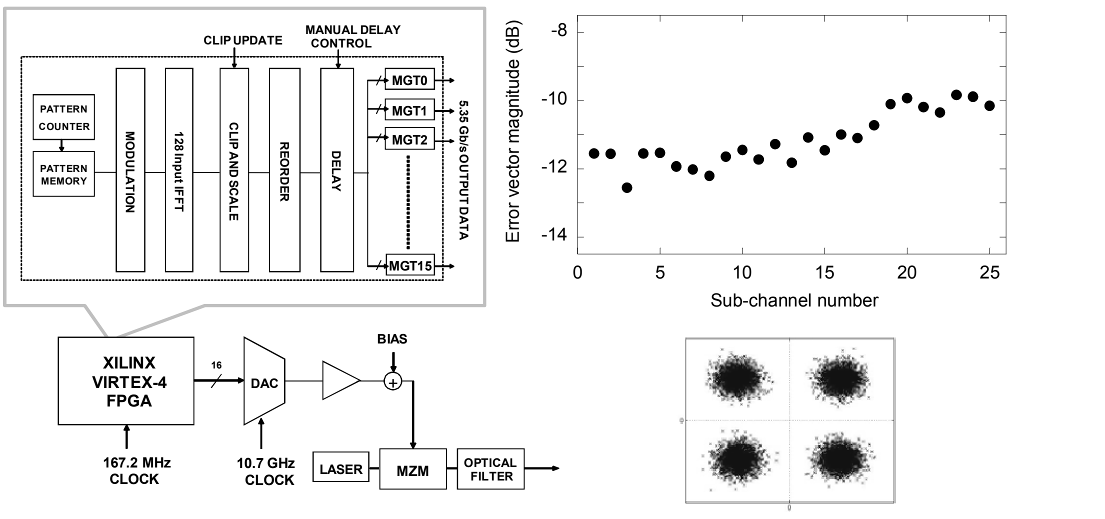
In [7], a 12.1 Gb/s optical OFDM transmitter with a 10 GS/s DAC was demonstrated in WDM transmission experiments with coherent detection, while in [8, 9], we reported a single sideband (SSB) optical OFDM transmitter based on a Xilinx Virtex-4 FPGA, with a 10 bit precision 128-point IFFT core operating at a frequency of 167.2 MHz, driving a DAC with a sampling rate of 21.4 GS/s (Fig. 1). Transmission experiments at 8.36 Gb/s over 1600 km of uncompensated standard SMF using a recirculating loop, with direct-detection and off-line signal processing at the receiver were carried out. In [10], a 3.1 Gb/s coherent receiver was reported, using an Altera Stratix III FPGA. The highest bit-rate reported to date [11], a 41.25 Gb/s direct detection receiver for passive optical network demonstrations, employed 6 parallel 32-point FFTs, implemented with sixteen Xilinx Virtex-5 FPGAs. Table 1 summarizes the system parameters of the various real-time optical OFDM experimental systems. In the next section, some key challenges being addressed in real-time transceiver implementation are discussed.

Table 1. Real-time optical OFDM experimental system parameters

Real-time Tx/Rx	Bit-rate (Gb/s)	DAC/ADC rate (GHz)	(I)FFT size	Distance (km)	Direct/ Coherent detection	Sub-channel format	Group	Refs
Tx + Rx	11.25	4	32	25	DD	QPSK-128QAM	Bangor Univ.	[5, 6]
Tx	12.1	10	256	400	Coh.	QPSK	Alcatel-Lucent	[7]
Tx	8.3	21.4	128	1600	DD	QPSK	UCL/CMU/ Intel	[8, 9]
Rx	3.1	1.4	64	back-to-back	Coh.	QPSK-16QAM	Univ. Melbourne	[10]
Rx	41.25	40	6 × 32	20	DD	8QAM	NEC Labs	[11]

3. Challenges in real-time implementation

OFDM transceivers operating at tens of gigabits per second require IFFT/FFT cores capable of sustaining exceptionally high throughputs. This challenge can be addressed by using novel algorithms that are not typically used in lower speed OFDM systems. In [13], a study is described in which the automated tool Spiral [14], developed at Carnegie Mellon University, was used to explore a wide space of possible algorithmic and datapath options, to choose those best fitting the requirements, and to automatically generate hardware implementations of them. The radix 2 Pease IFFT algorithm is frequently used in hardware implementations. However, in studies of many recursive IFFT algorithms carried out with Spiral, the most efficient was shown to be a mix of radix 8 and radix 16 IFFTs, which offers a reduction, by more than 25%, in the number of multipliers used in the comparable Pease implementation. This allowed an OFDM transmitter based on 12-bit precision 128-point IFFT operating at 167.2 MHz to be implemented on a Xilinx Virtex-4 chip [13], and the use of such optimized FFT algorithms in commercial ASIC-based transceivers is expected to minimize power consumption and chip area.



(a) (b)

Figure 1 (a) Experimental optical OFDM transmitter design top level hardware and FPGA functions (b) Error vector magnitudes per sub-channel after transmission over 1600 km, and back-to-back signal constellations [8, 9, 13]

A second challenge is receiver synchronization. In wireless OFDM, an autocorrelation synchronization technique is conventionally used, developed by Schmidl and Cox [15], in which a known sequence of samples is multiplied by a time-shifted copy of the same sequence. However, in very high throughput systems, in which the processing has to be carried out in parallel due to the low internal clock speed on the chip relative to the ADC sampling rate, this approach results in very high circuit complexity. An alternative synchronization technique has been proposed and investigated in [16]. This exploits the repetition in the signal waveform resulting from the cyclic prefix. Subtraction of the ADC samples separated by *N*, where *N* is the number of points of the FFT, combined with Gaussian windowing, allows the start of the symbol to be identified, and receiver synchronization to be carried out. This approach was demonstrated in a real-time FPGA-based 128-QAM OFDM receiver operating at 6.56 Gb/s in [16].

The next step in commercializing the technology will be the development of ASIC-based transceivers, which will offer lower power consumption than FPGA implementations. A design study, using simulations at the register transfer level (RTL), of key components of a 21.8 Gb/s QPSK-OFDM transceiver operating at 28 GS/s, assessing the power consumption and chip area when implemented with standard 65 nm CMOS libraries was published in [17].

4. Conclusions

Real time transceiver experiments are providing evidence of the feasibility of using OFDM signaling in future high capacity, spectrally efficient optical networks. A number of groups, using various types of FPGA, have carried out experiments at bit-rates of up to 41.25 Gb/s. This work is paving the way for future development and commercial deployment of high speed optical OFDM.

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