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LOW-POWER ASIC DESIGN WITH INTEGRATED MULTIPLE SENSOR SYSTEM

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ABSTRACT

Jafarian, Hossein. M.S.E.C.E, Purdue University, August 2013. Low-Power ASIC Design with Integrated Multiple Sensor System. Major Professor: Kody Varahramyan.

A novel method of power management and sequential monitoring of several sensors is proposed in this work. Application specific integrated circuits (ASICs) consisting of analog and digital sub-systems forming a system on chip (SoC) has been designed using complementary metal-oxide-semiconductor (CMOS) technology. The analog sub-system comprises the sensor-drivers that convert the input voltage variations to output pulse-frequency. The digital sub-system includes the system management unit (SMU), counter, and shift register modules. This performs the power-usage-management, sensor-sequence-control, and output-data-frame-generation functions.

The SMU is the key unit within the digital sub-system is that enables or disables a sensor. It captures the pulse waves from a sensor for 3 clocks out of a 16-clock cycle, and transmits the signal to the counter modules. As a result, the analog sub-system is at on-state for only 3/16th fraction (18 %) of the time, leading to reduced power consumption. Three cycles is an optimal number selected for the presented design as the system is unstable with less than 3 cycles and higher clock cycles results in increased power consumption. However, the system can achieve both higher sensitivity and better stability with increased on-state clock cycles. A current-starved-ring-oscillator generates pulse waves that depend on the sensor input parameter. By counting the number of pulses of a sensor-driver in one clock cycle, a sensor input parameter is converted to digital. The digital sub-system constructs a 16-bit frame consisting of 8-bit sensor data, start and stop bits, and a parity bit.

Ring oscillators that drive capacitance and resistance-based sensors use an arrangement of delay elements with two levels of control voltages. A bias unit which provides these two levels of control voltages consists of CMOS cascade current mirror to maximize voltage swing for control voltage level swings which give the oscillator wider tuning range and lower temperature induced variations. The ring oscillator was simulated separately for 250 nm and 180 nm CMOS technologies. The simulation results show that when the input voltage of the oscillator is changed by 1 V, the output frequency changes linearly by 440 MHz for 180 nm technology and 206 MHz for 250 nm technology. In a separate design, a temperature sensitive ring oscillator with symmetrical load and temperature dependent input voltage was implemented. When the temperature in the simulation model was varied from -50°C to 100°C the oscillator output frequency reduced by 510 MHz for the 250 nm and by 810 MHz for 180 nm CMOS technologies, respectively.

The presented system does not include memory unit, thus, the captured sensor data has to be instantaneously transmitted to a remote station, e.g. end user interface. This may result in a loss of sensor data in an event of loss of communication link with the remote station. In addition, the presented design does not include transmitter and receiver modules, and thus necessitates the use of separate modules for the transfer of the data.

1. INTRODUCTION

1.1 Overview

The development of nano-electronics and semi-conductor technologies in the last decade has resulted in a widespread usage of integrated circuits, replacing traditional circuit design methods. In an integrated circuit, analog and digital designs are placed in a small area, which enhances the capability of implementing several systems-on-chip for various applications. Because the $CMOS$ technology is basic on IC designs, it plays a major role in this achievement. Thus $CMOS$ technology in IC designs is applied to build $ASIC$s.

The proposed system combines analog and digital sub-systems on a single chip that is capable of driving four sensors and also generating serial data output. The prepared output in system-on-chip will be sent to a wireless communication module to transfer data to end user interface unit. To achieve better performance, this integrated system has to satisfy several conditions (i) read and monitor the sensors, (ii) convert captured analog signals to digital data, (iii) and package data in a serial protocol.

The analog sub-system has to satisfy the requirements for achieving higher quality in detection and monitoring the desired sensors. The first requirement is temperature independence of the system, especially for the analog sub-system. The modules applied to the analog unit should be independent of temperature variation. The second requirement is the power consumption of the system. The system should achieve minimum power consumption from the beginning of the process through sensor monitoring till the final data packaging. Finally, sensitivity is an important factor. To

achieve higher sensitivity, the system should respond to small changes in sensor analyte concentration. Two techniques are implemented to achieve higher sensitivity. In the first applied technique, a System Management Unit (SMU) manages all processes and allocates the power supply for the operating modules instead of all modules in the system. After modifying the power assignment and system monitoring, the modules should achieve minimum power consumption. Therefore, the second technique is in designing modules with minimum power consumption.

1.2 Literature Survey

With developments in nanotechnology and the ability to fabricate electronic elements in nanoscale, the system-on-chip has been proposed as a technology with widely ranging capability. The nano and micro technology have created the capability for designers to integrate large scale circuits in small areas. This was a first step to miniaturize the sub-systems and integrate them to achieve a pre-defined operation for integrated circuits. $CMOS$ technology has been proposed for constructing IC and specifically system-on-chip. Considering $CMOS$ technology and system-on-chip, in addition to the large scale of circuits in small areas, the main advantage is to achieve less power consumption while choosing smaller fabrication process technology.

A number of prior researches in the system-on-chip and $CMOS$ technologies have attempted low-power consumption [1–10]. The products could be used in passive systems such as radio frequency identification ($RFID$) [1–3] or other battery-less application [1, 3]. If the designed systems, circuits, or $CMOS$ components dissipated lower power, the harvest energy system could compensate power for system.

Common application for system-on-chip is in health care industry [1, 5–10]. To collect, process, and transmit body signals, the system-on-chip plays a critical role

in body sensor node (BSN). Zhang proposed a Body Sensor Node system-on-chip for data acquisition of Electrocardiogram (ECG), Electroencephalogram (EEG), and Electromyogram (EMG). Therefore, the chip was designed to support 3 data channels. In this work, the authors claimed BSN system-on-chip, which is capable of capturing and processing ECG data while the chip consumes only 19 μW. The low amount of power consumption is suited to utilize energy harvest topology. The proposed BSN system-on-chip included energy harvesting, dynamic power management, low voltage boost circuit, bio-signal front-ends, and radio frequency (RF) transmitter circuit topology. To harvest energy, they utilized two energy sources, thermoelectric and RF. The human body heat was the thermoelectric source. The energy was harvested from the human body with a thermoelectric generator (TEG). The chip was fabricated with 130 nm CMOS technology [1].

Kim et al. proposed a wireless sensor node system-on-chip that system-on-chip included a Profiled Power Management Unit for reducing active power consumption of a battery operated by an interactive home remote controller [2]. The proposed system-on-chip includes an 8-bit embedded microcontroller with 64 Kbytes in-system programmable flash memory, MAC, RF transceiver, and digital baseband. The system-on-chip was fabricated using 180 nm $CMOS$ technology. The proposed system-on-chip reduced active power consumption by about 18 %.

Kim et al. proposed a $CMOS$ transceiver for $RFID$ reader system-on-chip [3]. The authors proposed a system-on-chip that was $CMOS$ transceiver for a multi-standard 13.56-MHz $RFID$ reader. The system-on-chip includes an RF/analog part for modulation/demodulation and a digital part for controlling the transceiver functionality. The transceiver system-on-chip was fabricated with $CMOS$ 180 nm technology [3]. Others proposed the power-tracking embedded buck-boost convertor [4]. The proposed power convertor is designed for system-on-chip. The proposed power-tracking embedded buck-boost convertor is proposed with fast dynamic voltage scal-

ing ($F - DVS$) to achieve power requests for different operation functions of the system-on-chip. In this work, to meet minimum power consumption, the recycling energy is derived during the down tracking period. The chip was fabricated with 250 nm $CMOS$ process. Through $F - DVS$ the tracking speed from 3 to 2 V and vice versa are 15 and 20 μs, respectively, with a high switching frequency of 5 MHz.

Teo et al. proposed a wireless sensor node system-on-chip for health and medical application [5]. The proposed wireless sensor node system-on-chip is a low-power and low-voltage system for continuous real-time application for health monitoring. The system-on-chip consists of a sensor interface circuit, an analog-to-digital convertor, a digital signal processor and a radio-frequency transmitter. However this work uses the off-chip components, which includes crystal and supply decoupling capacitor. The chip is designed for acquisition and transmission of signals. The system-on-chip consumes merely 700 μW at 0.7 V supply voltage. The proposed system-on-chip was implemented in a 180 nm $CMOS$ process.

Verma et al. proposed the EEG acquisition system-on-chip [6]. The system-on-chip is integrated with a feature extraction processor for a chronic seizure detection system. The system-on-chip supports one EEG channel. Depending on the patient, it may correspond up to 18 channels to detect seizures. The system-on-chip contains an instrumentation amplifier, ADC, and digital processor that streams features-vectors to a central device. The complete one-channel system-on-chip operates from a 1 V supply, consuming 9 μW J per feature vector. The system-on-chip is fabricated in a 180 nm $CMOS$ technology with five-metal-two-poly layers [6].

The recent BSN performances are compared in Table 1.1. The system-on-chip can be operated with the energy, which is harvested from thermoelectric, RF and solar sources and stored in capacitor [1, 8]. The passive system-on-chip consists of power management processor, general-purpose microprocessor ($GPPMCU$), and

supply regulator [1, 8]. Based on the level of the stored energy in capacitor, the power management controls the power of the nodes and activates or deactivates the units. The MCU in the chip can process, store, and transmit the data flexibility. In this topology, the most power in the digital part is dissipated in the MCU. The data transmitter (TX) unit in the system-on-chip consumes a high rate of power ($TX - PDC$), when the transmitter is on for hundred percentage of duty cycle, rather than other components [1, 6–10]. Therefore, to achieve lower power consumption in passive system-on-chip, the data is stored in the memory and then the saved data is transmitted in partial of the duty cycle [1, 10]. Other approach for reducing power consumption was merely using memory [7].

Chun Wei Li proposed a $CMOS$ temperature sensor that is highly linear. To overcome the nonlinear effect, the authors suggested utilizing a compensation scheme between two current sources driven in the saturation region with different bias voltage. The authors claim that the maximum temperature error is ± 0.022°C and it consumes 137 μW. The proposed sensor is implemented in $TSMC$ 350 nm $CMOS$ technology [11]. Other authors proposed a micro range power consuming $CMOS$ temperature sensor that is insensitive to device parameters [12]. The proposed sensor was operated by 1 V and was simulated with a standard 350 nm $CMOS$ device parameter by the $HSPISE$. The maximum power consumption is 0.27 μW while the temperature range is from 0 to 100°C. And the temperature sensitivity of the proposed sensor is 1.01 mV/°C.

Souri et al. proposed the design of a $CMOS$ temperature sensor, which is low power and energy-efficient for $RFID$ applications [13]. The proposed sensor achieved an inaccuracy ± 0.15°C from -55 to 125°C. The sensor is implemented in a 160 nm $CMOS$ technology when it consumes 27 nJ per conversion. In other work, the authors proposed the $CMOS$ temperature sensor based on a frequency-to-digital convertor [14]. The proposed sensor utilized a ring oscillator to generate a temperature

dependent frequency. The resolution of the proposed sensor is 0.18°C/LSB and the demonstrated maximum inaccuracy is less than ±1.5°C while the temperature range is from 0 to 110°C. The sensor is fabricated in 65 nm $CMOS$ technology and the entire block consumes 500 μW. The recent temperature sensors performances are compared in Table 1.2.

1.3 Research Objectives

The goal of this research is the realization of low-power $ASIC$ design with integrated multiple sensor system applicable in monitoring vital parameters of human body or environment, which sends the collected information to a remote device, such as a cellphone, for un-interrupted involuntary continuous monitoring. The specific objectives of this work include designing and developing low-power chip that is capable to drive several sensors and easily adaptable for a wide range of applications.

A novel method of power management and sequential monitoring of several sensors is proposed in this work. Goals of the proposed method include managing sequence of sensor operation, reducing power consumption with managing power for each cycle, and generating a serial data output. The proposed system-on-chip comprises of two major sub-systems, digital and analog. In the analog sub-system, different segments will capture voltage variations in each of the sensors. The captured signal will be amplified within the analog sub-system and transmitted to the digital sub-system. In the digital sub-system, the analog signals will be converted to pulses and to digital form by counting the number of pulses per clock cycle. The digitized signal output from the digital sub-system will be transmitted to communication stage.

The function of the digital sub-system is also to control analog sub-system. In fact, the each unit of the analog sub-system is controlled by enable signal from digital

Table 1.1
Performance Comparison of BSN Nodes System-on-Chips

	Zhang et al. [1]	**Kim et al.** [6]	**Verma et al.** [7]	**Chen et al.** [8]	**Rai et al.** [9]	**Yan et al.** [10]
Sensors	EEG, EMG ECG	ECG	ECG	Temperature Pressure	Neural, ECG EMG, EEG	ECG TIV
Supply Voltage	30 mV, -10 dBm	1.2 V	1 V	0.4 V/0.5 V	1 V	1.2 V
Energy Harvesting	Thermal, RF	N/A	N/A	Solar	N/A	N/A
Power Management	yes	N/A	N/A	yes	yes	yes
Supply regulator	yes	N/A	N/A	yes	yes	yes
GPP MCU	yes	N/A	N/A	yes	yes	yes
ADC	yes	yes	yes	yes	yes	yes
Memory	yes	yes	N/A	yes	N/A	yes
$T_x P_{DC}(100\% on)$	160 μW	N/A	N/A	N/A	400 μW	2.8 mW
Digital Power	2.1μW	12μW	2.1μW	2.1μW	N/A	500 μW
Total Chip Power	19 μW	31.1 μW	77.1 μW	7.7 μW	500 μW	2.4 mW
Technology	130 nm	180 nm	180 nm	180 nm	130 nm	180 nm

Table 1.2
Performance Comparison of Temperature Sensors

	Souri, et al. [13]	**Hwang, et al.** [14]	**Lee, et al.** [15]	**Wu, et al.** [16]	**Law, et al.** [17]	**Souri, et al.** [18]	Aita, et al. [19]	Woo, et al. [20]
Sensor Type	BJT	Ring Oscillator	MOSFET	Resistor	MOSFET	BJT	MOSFET	Ring Oscillator
CMOS Technology (nm)	160	65	180	180	180	160	700	130
Supply Voltage (V)	1.5–2	1	N/A	1.2–2	0.9–1.1	1.6–2	3.3	0.8
Temperature Range (°C) (V)	-55 to 125	0 to 110	-65 to 165	0 to 100	0 to 100	-30 to 125	-70 to 130	5 to100
Accuracy (°C)	±0.15	±0.15	±1.9	±0.5	-0.8/+1	±0.2	±0.25	N/A
Power Consumption (μW)	6.12	500	53.4	36	405	7.4	100	0.03

sub-system. The objective for controlling enable signal is to reduce power consumption of the system. The analog subsystem includes four sensor derivers. The sensor derivers work based on frequency change with input voltage or current, which in turn is dependent on sensor parameters such as resistance or capacitance. The analog sub-system will be designed for high sensitivity such that a small change in the input voltage can be detected.

Low power consumption can be achieved by activating a sensor for only a fraction of the clock cycle. For example, in the proposed design a sensor is activated during 3 clocks of 16 clocks cycles while all other sensors remain inactive. The result is that each sensor is activated once every 64-clocks (4×16). Therefore the analog subsystem consumes the power for one sensor during 3 clocks of 16 clocks cycle. With this method, the power consumption is reduced by 82% compared to a configuration where all the sensors are continuously activated. The sensors sampling rate depends on the clock of the system. As a result higher sampling rate can be achieved by using higher frequency. The number of sampling rate for each sensor per second is given by:

$$SampleRate = \frac{1sec}{64 \times \frac{1}{f_c}} \tag{1.1}$$

Where f_c is clock frequency.

After choosing optimal method to monitor the sensor and generate final output, the designed components should satisfy the mentioned requirements especially in analog sub-system. The system will include components such as current-starved-ring-oscillator, temperature sensor based on ring oscillator, variable current source to drive resistance-based sensor, and 8-bit controllable voltage source to control the current source output. Selected designs for all mentioned components will work to minimizing temperature dependency and lowering power consumption.

Based on the defined method, the core of the sensor-drivers is a ring oscillator. Two types of oscillators are proposed, insensitive for most applications and temperature sensitive to be utilized as an integrated temperature sensor. To achieve such oscillators, two methods will be implemented, a different arrangement for delay elements and two levels of voltage bias units. As the threshold voltage is dependent on temperature, the effect is minimized for temperature-independent and maximized for temperature-sensitive ring oscillator designs.

2. THEORY AND DESIGN

The presented system-on-chip includes two major sub-systems, analog and digital, and drives several integrated sensors, manages sensor power consumption and operation sequence, converts sensor analog generated output to digital, and provides a digital data frame to a communication unit. In Figure 2.1, various units of the system are illustrated. Each sub-system includes several smaller components to achieve the system goals. Each small component, which belongs to both main sub-systems, is applied to provide a way for building a system with the desired features. The presented method suggests that analog voltage variation is converted to pulse waves frequencies in the analog sub-system. It means that the width of pulse wave depends on the sensor-generated voltage and by increasing input voltage; the pulse wave width goes to a smaller value, producing higher frequencies. In addition, the other defined duty for the digital sub-system is managing the power consumption and monitoring sensors sequentially. Each suggested segment in both sub-systems is placed based on the described method to achieve the desired defined features.

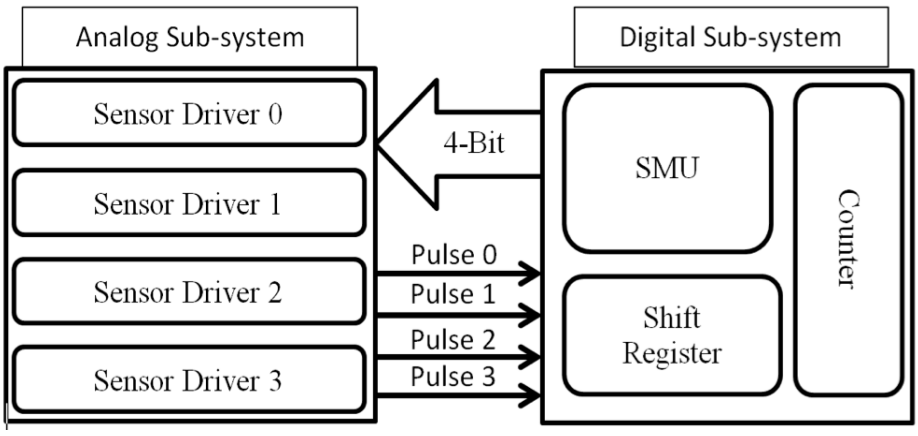

Fig. 2.1. System Block Diagram

The main objective is that the system will be capable of driving four sensors, including their analog sub-system module drivers. The outputs of the analog sub-system consist of four pulse shaped outputs. According to the represented method for sensor monitoring and reading, a frequency of each pulse wave output is changed with the generated range of voltage, which shows a sensor state. Therefore, the sensor-driver modules convert voltage to frequency. To satisfy these requirements such as power consumption, temperature dependency and etc., each sensor-driver includes units to provide the requisites of the system. The main role of the included sensor-driver units is voltage conversion to frequency based on the main defined strategy for the entire system. The sensor-drivers apply modules to generate pulse waves with variable frequency based on voltage crossed over the sensors. The process in each sensor-driver is called pre-processing.

After pre-processing the analog sub-system, the pulse wave will be ready for transferring to the digital sub-system for completing the entire process and generating a final output that consists of 8-bit parallel data, which shows the state of each sensor sequentially. According to the basic strategy of the system, the digital sub-system should call each sensor-driver sequentially to receive the generated pulse wave within the analog sub-system. After receiving pulses, in the next step, the number of pulses is counted per each clock cycle. And in the final stage, the counted number of pulses is packed in a package of data. After data packing, the monitored sensor is forced to become inactive by digital sub-system. To perform each defined step for the digital sub-system, three modules are applied. The main role of digital sub-system is referred to SMU module.

The SMU correlates all components in the system, manages all of its duties, and finally governs order and sequence. To sequential call sensor-drivers, the SMU generates the enabling signal to push on each sensor-driver in its turn. Turned on sensor-driver generates the pulse wave then the SMU captures the generated signal

and sends the captured signal to the counter while enables the counter module to start counting. During a clock cycle, the counter module counts the number of pulses in the received signal. The result of counter output is 8-bit parallel data. To avoid power dissipation, the SMU forces sensor-driver to inactive with changing in enabling signal state from 1 to 0. Now, all sensor-drivers are inactive. Then the SMU addresses to third modules of digital sub-system to pack parallel data in package of series data and prepares the data to transfer for communication module. After pulse counting, the SMU immediately sends the enabling signal to parallel to serial register module. With completing data packing, the SMU sends enable signal for next sensor-driver and repeats all process again for a new sensor-driver. The presented design is implemented in Tanner and Mentor Graphics software for simulation [21, 22]. In this chapter, the presented circuit design images are taken from Tanner Tools.

2.1 Analog Sub-System

2.1.1 Design Overview

According to the main design system method, sensor-driver modules have to be able to generate pulse waves. The frequency of the pulse wave reflects variation in sensor parameters. The sensor factor is shown as an input voltage; therefore, the sensor-driver has to convert input voltage to pulse waves, and its frequency depends on input voltage. As shown in Figure 2.2, the sensor-driver is controlled with two main inputs. First is the enable signal, which is provided by the digital sub-system. Second is input voltage that represents the variation of the sensor factor. When the enable signal goes high, the sensor-driver module starts translating sensor parameters to pulse waves. The applied method for voltage to frequency conversion is to use a voltage controlled oscillator (VCO). To reach the desired results, the utilized VCO in sensor-driver provides stability and sensitivity of the sensor-driver. To achieve

stability and sensitivity, the VCO should be temperature independent, sensitive to small changes of input voltage, and have a wide tuning range.

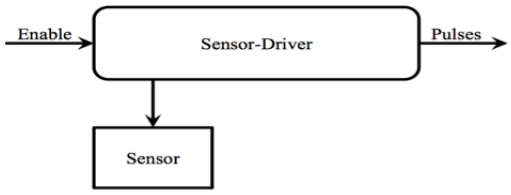

Fig. 2.2. Sensor-Driver Block Diagram

The VCOs desired features play a significant role in achieving sensitive and stable analog system. The first noteworthy feature is temperature stability for the sensor-driver. One goal in this research is to achieve a system with wide range temperature operation of region. To reach this purpose, the frequency of the VCO output should be stable against temperature variation because the output frequency represents the sensor state. So the only desired effective factor on the VCO is the input voltage that is generated by sensors. However, other effective parameters on output frequency should be eliminated or reduced. The significant undesired effective parameter on frequency is the temperature. So the sensor-driver is designed by considering minimum temperature dependency. In order to increase the accuracy of the system, the system should be able to respond to small changes in the sensor state that are proposed with the input voltage of the sensor driver. The input voltage controls the output frequency of the sensor-driver and the frequency is generated by the VCO. The output frequency of the VCO should respond to small changes in input voltage.

Based on the main method in the system design, changing the frequency with a small input voltage will not be enough to achieve more accuracy. The generated output wave pulse is counted per system clock in the digital sub-system. In order to detect a small change in input voltage, the change in frequency should be visible within the clock cycle of the system. This means that in small voltage variations, the

generated difference in frequency should be big enough to be visible during the system clock cycle. If the voltage changes are increased in the number of pulses per clock, the system will be able to detect the voltage change. Therefore, in order to get better accuracy and higher sensitivity, the VCO should vary the frequency that makes a change in the number of pulses during the system clock cycle. If the VCO has a wider tuning range, the chance of detecting small variation in the input voltage is increased.

The main goal of the analog sub-system is driving the sensors of various categories. In this work, the sensors are divided into three main categories (resistance-based, capacitance-based, and $CMOS$-based devices) and the analog sub-system is capable of deriving all the categories. In resistance-based sensors, the sensor models the changes in the environmental parameters with resistance variation. So changing in any of the physical qualities considered creates variation in resistor values, which in there creates change in the input voltage for the VCO. In the capacitance-based sensor, the analog sub-system should be capable of presenting changes in capacitor variation, which shows a specific environmental capacitance-based sensor, with frequency changes in the pulse waves. The third category is the internal sensor that detects temperature variations. Changing temperature variation creates pulse wave, with a frequency that is proportional to temperature. The analog sub-system includes three kinds of sensor-drivers, resistance-based, capacitor-based, and $CMOS$-based devices. In each category of sensor-driver, the specific method is utilized to satisfy the requirements of the strategy to read, monitor, and control the sensor-drivers, and the analog sub-system units associated with them.

2.1.2 Resistance-Based Sensor-Driver

To drive a resistance-based sensor, the output of sensors resistivity should be converted to voltage, which is fed to the VCO. The block diagram in Figure 2.3 shows

the components used to drive the resistance-based sensor. The current sources supply currents for sensors. The monitored environmental parameter is modeled with resistivity in sensors. If the current source drives the sensor with constant current, the across voltage of the sensors are changed with resistant variations. Because the desired design is temperature independent, the generated current should be independent on temperature. Therefore, the current source is designed with minimum dependency on temperature variation. The current source also creates a range of current that makes sensor-drivers capable of the driving resistance-based sensors with different ranges of sensor resistance. The input of the VCO has a constant range of voltage that can generate the signals with different frequencies. Constant current, generated by the current source, provides the input voltage with multiplying with resistance. This means that the input voltage range is built by variation in sensor resistance.

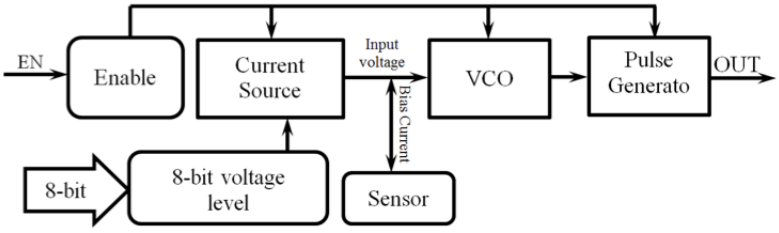

Fig. 2.3. Block Diagram of Resistance-Based Sensor-Driver

To keep the input voltage in a specific range when driving sensors with the sensor-driver, the current source should be able to generate different levels of currents for sensors with different resistance ranges. The result is a sensor-driver that is capable of driving multiple sensors rather than a specific one. To control the current level, a new component is added to the sensor-drivers. The defined duty for the component (8-bit voltage shift level) is generating different levels of voltage to control the output current level of the current source. Therefore, with changes in voltage levels, the current control can generate a wide range of current to drive resistance-based sensors.

To achieve certain requirements for the analog sub-system, the specific characteristics of the VCO should be defined. The main requirement for the units of analog sub-systems is the temperature dependency. The desired state for the analog subsystem is minimum temperature dependency. In the design, it is assumed that the VCO is temperature independent. As shown in Figure 2.4, the VCO consists of a loop of N number of delay elements to generate a periodic signal. This type of VCO is known as a ring oscillator. The signal frequency depends on the delay of each element (τ) and number of the delay elements N (odd). The frequency of the ring oscillator varies by input voltage. Therefore, the delay of the elements in the ring oscillator is a function of the input voltage if N is constant [23–35].

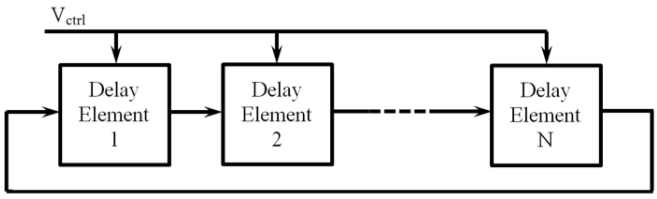

Fig. 2.4. Looped Odd Number of Delay Element for Ring Oscillator

The ring oscillator is enabled or disabled by the Enable (EN) signal from the digital sub-system. As the loop depends on the feedback signal, enabling can be achieved by controlling the feedback path as shown in Figure 2.5 [24, 25].

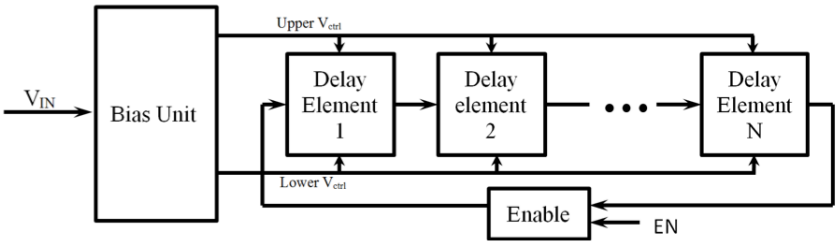

Fig. 2.5. Block Diagram of Ring Oscillator with Enable Component

To provide input voltage for the ring oscillator, the current source is located in the sensor-driver for the resistant-based sensor. The current sources are designed power-supplies voltage insensitive with low temperature sensitivity. To achieve such specifications, the bootstrap bias technique is applied which is a self-biasing technique [36]. The self-biasing technique can significantly reduce power-supply sensitivity. The block diagram of the bootstrap concept is shown in Figure 2.6. The current source and current mirror form the relationship between two main variables in this configuration. These variables are the input and output current, I_{IN} and I_{OUT}. In this concept, the input of the current source is a function of the output current. In comparison with the resistor biasing case, the current sources are made very stable by power-supply voltage variation. If the feedback loop, which is illustrated in Figure 6, is biased in a stable operating point, with wide range of input currents, the output current will be voltage independence [36].

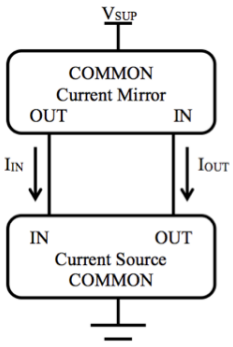

Fig. 2.6. Block Diagram of Current Source

The output current is independent on a wide range of input currents and consequently independent of power-supply voltage; but the output current should be controllable and modified. To achieve this capability, the current source should include a controllable element with out-source voltage. In this concept, a resistor, which is biased with threshold voltage, V_t, creates the output current. The threshold voltage is a constant factor for the $CMOS$ transistor so the resistor has to be controllable.

Therefore, changing the biasing resistor varies the output current and value of the resistor controlled by out-sources voltage. This means that the resistor in the current source is replaced with the element, which acts such as a variable resistor. The resistance value of the replaced element is a function of voltage.

To provide the voltage for controlling the output current, the voltage source generates a range of voltages. Also, the output voltage level is controlled with an 8-bit input that can make 8 levels of voltage as an output of voltage source. The simple method is used to provide different voltage levels. As shown in Figure 2.7, the voltage divider is applied to produce output voltage that is a portion of V_{SUP}. The governed relationship between V_{SUP} and V_{OUT} is

$$V_{OUT} = \frac{R_2}{R_2 + R_1} V_{SUP} \tag{2.1}$$

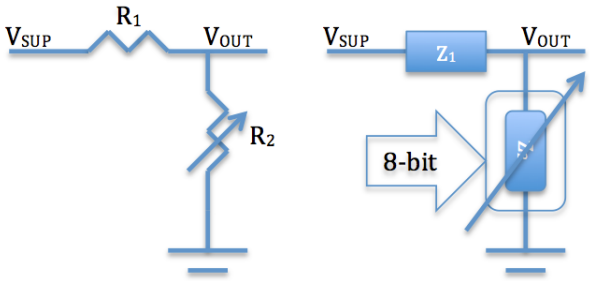

Fig. 2.7. Voltage Divider

Therefore, based on equation 2.1, if the R_1 is constant, with varying R_2, a range of voltage is produced. According to this concept, R1 is replaced by a CMOS element with constant impedance. And for R_2, the chain of $CMOS$ transistors is improvised. The impedance of $CMOS$ chain-transistor is regulated by an 8-bit input. For variation in input bits, the output voltage is changed in 8 levels. The created voltage levels directly connote to the current source for determining the biasing resistance

value. With the proposed technique, the resistance-based sensors are biased with a suitable current that keep crossed voltage over sensors in the operating range of ring oscillator. Therefore, the proposed sensor driver can drive a range of resistance-based sensors instead of a specific sensor.

2.1.3 Capacitance-Based Sensor-Driver

As discussed in resistance-based sensor-driver (2.1.2), the ring oscillator is the key in this kind of sensor-driver. In this case, again for driving a sensor based on capacitive nature, the strategy is using the ring oscillator as a core of the sensor-driver as shown in Figure 'reffi:8. The ring oscillator generates a periodic signal based on a loop of delay elements. Because the sensor-driver is design for sensor with capacitive nature, the sensor can be defined as a delay element. The result is that the sensor variation can make a range of delays as a delay element. Therefore, the capacitance-based element can effect on frequency of ring oscillator output signal. According to this concept, instead of placing the sensor before ring oscillator, the capacitance-sensor is placed after the ring oscillator output. The output of the ring oscillator stimulates the sensor with constant frequency, and then the output frequency is formed with sensor parameter variation. In this method, the capacitance-sensor is derived by a periodic signal.

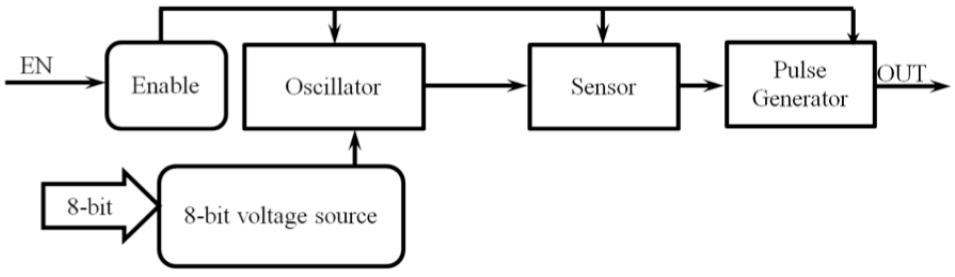

Fig. 2.8. Block Diagram of Capacitance-Based Sensor-Deriver

2.1.4 *CMOS*-Based Temperature Sensor-Driver

The defined method to monitor the sensor variation is based on counting the number of pulses generated by the sensor-driver while the frequency of pulses is the result of voltage converting to frequency in the ring oscillator. Therefore, if the voltage is constant, the output frequency of the ring oscillator should be constant. On the other hand, the only factor in frequency variation is not the input or control voltage of the ring oscillator. Other factors such as temperature can generate differentiation in output frequency. If the ring oscillator in sensor-driver is sensitive to temperature instead of insensitive to it, the result will be a system whose output frequency is much more sensitive to temperature variations. In this work, the explained concept assists to design a *CMOS*-based temperature sensor-driver. According to this concept, to achieve the desirable temperature sensor, the temperature effect on the elements is greatly increased.

In addition, fundamentally the V_{ctrl} variation can affect the output frequency of the ring oscillator. If the control voltage of the ring oscillator is provided by a voltage source, whose output voltage depends on temperature, the output frequency is much more sensitive to temperature. Therefore, two key parameters can make variations in output frequency of ring oscillator, first is inherent response of ring oscillator to temperature variations, and second is the frequency change due to the control voltage value based on temperature variation. According to the ring oscillator definition, the output frequency is a function of the delay of N elements in loop. So the delay in the ring oscillator should be dependent on temperature. In *CMOS* transistors, the significant variable that is dependent on temperature and also can make changes in the delay of the ring oscillator elements is threshold voltage, V_t. Now, based on the strategy for the ring oscillator, the output of the voltage source for controlling ring oscillator should be a function of threshold voltage. Therefore, both significant effects, which can increase temperature sensitivity, are functions of V_t.

The Figure 2.9 shows the configuration of CMOS-based temperature sensor. The core of the temperature sensor is ring oscillator same as other sensor-drivers but in this case, the ring oscillator in temperature sensor-driver is more sensitivity to temperature. Fundamental of ring oscillators are the same. The main deference is the delay element. For ring oscillator in CMOS-based temperature sensor-driver, the delay element depends to temperature but in other cases, the delay element is independent to temperature. The delay of elements in ring oscillator is dependence to threshold voltage. Control voltage of the ring oscillator is provided with the voltage source that depends to threshold voltage. After generating the periodic signal, which its frequency dependent to the temperature, the output of the ring oscillator goes to pulse generating module to form the periodic signal to pulse signal. In this case, the enable method follows the proposed method for other cases. The output of the following block diagram will be a pulse wave that its frequency proposes the environment temperature.

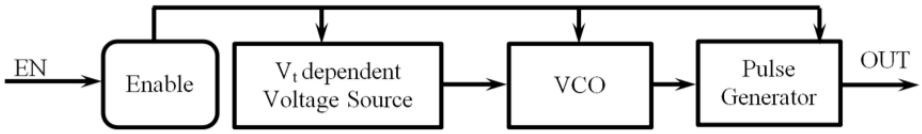

Fig. 2.9. Block Diagram of CMOS-Based Temperature Sensor-Deriver

2.1.5 Theory

Single-ended Current Starved Ring Oscillator

A conventional ring oscillator consists of a series of odd number, N, of inverter, which forms a loop. The oscillation frequency is adjusted with the analog control voltage (V_{ctrl}) [37–40]. Swiping the control voltage will alter the bias current, I_{ctrl}, which crosses over the $PMOS$ and $NMOS$ transistors in each delay stage, current starved

invertor. Changing in current of each stage causes different delay. By controlling the delay time of each stage the oscillation frequency of ring oscillator is adjusted. If each stage generates the same delay (τ), the frequency of oscillation (f_{osc}) is calculated as [38, 39]

$$f_{osc} = \frac{1}{N \times \tau} \tag{2.2}$$

Generated delay for each stage can be calculated by [19]

$$\tau = \frac{V_{osc} C_G}{I_{ctrl}} \tag{2.3}$$

Where C_G is parasitic capacitance of the $NMOS$ and $PMOS$, and V_{osc} shows the amplitude of the oscillator. In this case, assumed C_G is equal for both $NMOS$ and $PMOS$. Frequency is then inversely proportional with the delay generated delay time.

The ring oscillators presented in this work consists of delay elements, which are current starved invertors that have significant role to control generated frequency. In this arrangement, to generate bias current, the current starved invertor with power switching in conventional design is biased by the presented bias unit. With this Structure, the bias unit provides a range of control voltage to increase sensitivity of ring oscillator. The bias unit improves the biasing voltages of the ring oscillator with maximum voltage swing, which eventually increase the sensitivity of the ring oscillator by providing higher oscillatory frequencies.

In addition of frequency stability of the oscillator against temperature variation was one of goals of this work. To increase stability, the control voltage to the bias unit is supplied from a threshold voltage independent source. Threshold voltage in MOS transistor is the temperature dependent factor. Therefore, to overcome the temperature effect on frequency, the ring oscillator should be controlled by source, which is temperature independent. The presented bias unit generates the control voltage for ring oscillator with minimum threshold voltage dependency and consequently minimum temperature dependency.

Current Source

The designed ring oscillator has two voltage inputs applied to both the $PMOS$ and $NMOS$ sides, to control the frequency output. The input voltage depends on the sensor equivalent resistance. Therefore, the resistor-based sensor-driver generates the input voltage based on changing in the desired parameter to monitor. For this purpose the sensor will be derived with constant current as shown in Figure 10. So with changing the physical parameter, the sensor resistance changes to provide a range of input to the input of the oscillator in order to generate the output signal.

As shown in Figure 2.10, the voltage across the resistor will change linearly if the sensor creates linear response to environmental factor. The operation point of the oscillator is between 1 V and 2.5 V. In this range, the oscillator operates in the linear state. Also, the resistor of sensor, R_S, changes in in the Ohms range. Therefore, the magnitude of the output voltage will be determined based on range of values for R_S and constant bias current, I_{BIAS}.

$$R_{min} \leq R_S \leq R_{max} \tag{2.4}$$

$$\rightarrow V_{min} \leq I_{BIAS} \times R_S \leq V_{max} \tag{2.5}$$

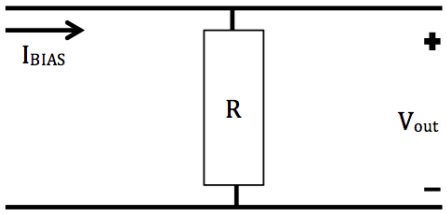

Fig. 2.10. Resistance-Based Sensor Biasing

To drive the sensor, the current bias should be determined following the above equations, and the current source should be designed to provide this current for the

system. An important factor to consider is that the current source should be insensitive to power-supply voltage and temperature variations. Therefore, the bias current is assumed to have has much less variation with small changing in power-supply voltage or temperature, two important aspect of the biasing circuit performance. The sensitivity, S_x^y, is defined as [36]

$$S_x^y = \lim_{\Delta x \to 0} \frac{\Delta y/y}{\Delta x/x} = \frac{x}{y}\frac{\delta y}{\delta x} \tag{2.6}$$

Applying above equation to find the sensitivity of the bias current to small variation in the power-supply voltage gives

$$S_{V_{DD}}^{I_{BIAS}} = \frac{V_{DD}}{I_{BIAS}}\frac{\delta I_{BIAS}}{\delta V_{DD}} \tag{2.7}$$

The well-known bootstrap bias technique, which is also referred to as self-biasing, can greatly reduce the power-supply sensitivity. The following block diagram shows the concept of this technique. If the feedback loop in this form is operated in stable point, I_{IN} and I_{OUT} will be much less sensitive to power-supply voltage. The relation between the input and output current are determined by both the current source and current mirror.

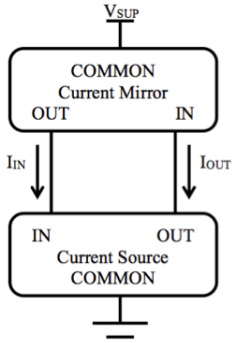

Fig. 2.11. Current Source Block Diagram

The circuit illustrated in Figure 2.12, implemented in tanner tool and redrawn for clarity [21], shows the threshold-referenced MOS. M_1, M_2, and R governing the output current that slightly depends on the input current. Relation between current output and current input is given by [36]

$$I_{OUT} = \frac{V_{GS_1}}{R} = \frac{V_t + V_{ov1}}{R} = \frac{V_t + \sqrt{\frac{2I_{IN}}{k'(w/l)_1}}}{R} \tag{2.8}$$

Where V_t, V_{ov}, and I_{IN} are threshold voltage, overdrive voltage, and drain current respectively for M_1 as indicated in Figure 2.12. The interesting case in design is that the overdrive on M_1 is smaller than the threshold voltage. In practice this can be achieved by a low input current and large $(w/l)_1$. Combining 2.7 to 2.8, give:

$$S_{V_{DD}}^{I_{OUT}} = \frac{V_{ov_1}}{2I_{OUT}R} S_{V_{DD}}^{I_{IN}} = \frac{V_{ov_1}}{V_{GS_1}} S_{V_{DD}}^{I_{IN}} \tag{2.9}$$

In this configuration, the input current (I_{IN}) depends strongly to the power-supply voltage (V_{DD}), thus the sensitivity of input current to power-supply voltage ($S_{V_{DD}}^{I_{IN}}$) is approximately equal to one, $S_{V_{DD}}^{I_{IN}} \approx 1$ [36]. Therefore, the output current sensitivity is given by:

$$S_{V_{DD}}^{I_{OUT}} = \frac{V_{ov_1}}{V_{GS_1}} \tag{2.10}$$

As shown in Figure 2.13, for a wide range of input current, the output current is independent on the input current. In this figure, two intersections or potential operation point are shown. Point A is the desired operation point and point B is an undesired operating point. If the gain of the current mirror circuit is unity, based on the standpoint of the current mirror, the input and output currents are equal but with using bootstrap bias technique, the input and output currents are independent. To determine the operation point, the intersection point between actual curve and

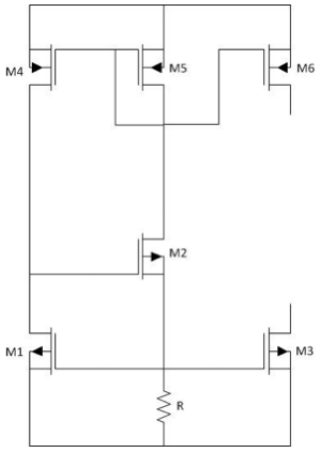

Fig. 2.12. Circuit Schematic of Current Source

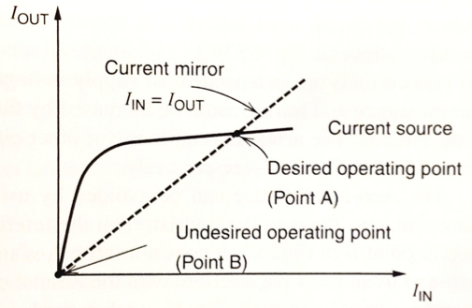

Fig. 2.13. Operation Point of the Current Source [36]

standpoint line can be found.

To avoid the undesired operation point, $I_{IN} = I_{OUT} = 0$, the start-up circuit is used as shown in Figure 2.14 implemented in tanner tool and redrawn for clarity [21, 41].

After assessing power-supply voltage effect on the performance of current biasing circuit, the other important aspect is temperature. The fractional temperature coefficient, TC_F [39] is given by:

$$TC_F = \frac{1}{I_{OUT}} \frac{\delta I_{OUT}}{\delta T} \tag{2.11}$$

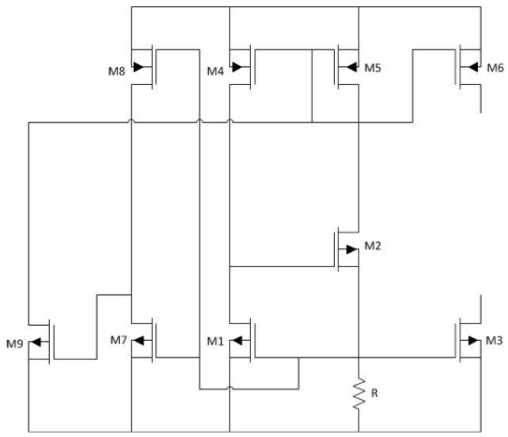

Fig. 2.14. Current Source Schematic with Start-up Circuit

With low input current and large $(w/l)_1$, the I_{OUT} equals

$$I_{OUT} = \frac{V_{GS_1}}{R} \simeq \frac{V_t}{R} \tag{2.12}$$

Using the sensitivity definition given above, first TCF equation can be written as

$$TC_F \simeq \frac{1}{V_t}\frac{\delta V_t}{\delta T} - \frac{1}{R}\frac{\delta R}{\delta T} \tag{2.13}$$

Voltage Level Shift Source

To provide a voltage source with producing different levels of voltage, based on voltage divider strategy as shown in Figure 2.15, the variable resistor should be designed with capability to set with 8-bit digital input.

The transmission gate is shown in Figure 2.16, taken from tanner tool [21]. Based on the transmission gate design, this gate acts as a resistor. The equivalent resistance equals the combined parallel resistors that are function of the gate voltage. Therefore, the equivalent resistance of the transmission gate changes with the gate voltage for

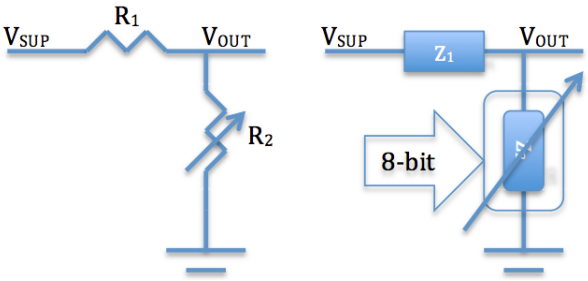

Fig. 2.15. Controllable Voltage Divider

both the $NMOS$ and $PMOS$ transistors. When the gate voltage is high, the equivalent resistance is minimized because both transistors are in conductive region. On the other hand, the device gate terminal turns off the device when the gate voltage is zero. In this case both transistors are in the cut off region and ideally the resistance can be infinity. As result, with varying the gate voltage from 0 to high, the equivalent resistance can be varied from infinity to zero, indicating that the resistance of the transmission gate is voltage dependent.

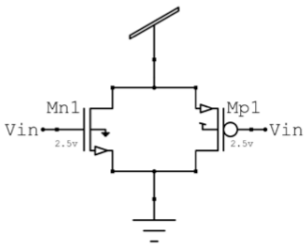

Fig. 2.16. Transmission Gate

The current of any of the two transistors, Mn_1 and Mp_1 shown in Figure 2.16, is controlled by input voltage Vin. The current plot versus input voltage of these devices are shown in Figure 2.17 (indicated as (a) and (b)). As the supply voltage is constant, the total current from the two devices (indicated as (c) in Figure 2.17) controls the equivalent resistance of the two transistors (transmission gate, indicated as (d) in Figure 2.17 [42]. Thus, during the ON state of the transmission gate, with

input voltage sweeping from ground to V_{DD}, the ON current and ON resistance of transmission gate varies as shown in Figure 2.17.

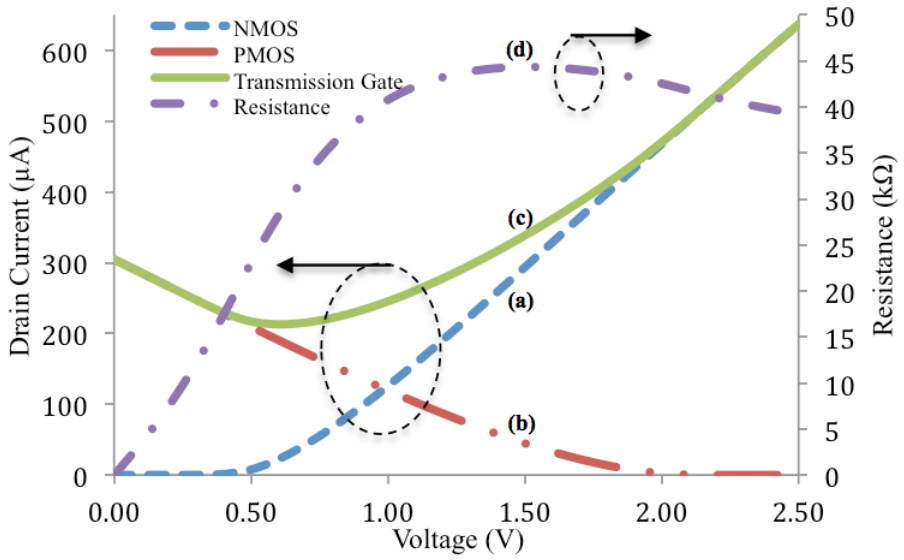

Fig. 2.17. a) NMOS Current, b) PMOS Current c) Transmission Gate Current, and d) Transmission Gate Resistivity

The transconductance (g_m) of the $CMOS$ transistor is related directly to width (w) and inversely to length (l). According to the relationship between g_m and $CMOS$ resistivity, equation 2.14, increasing w will reduce the resistance, while increasing l will increase it. Therefore, the resistance of the transmission gate (r_o) is strongly dependent on l and w of the two transistors shown in Figure 2.16.

$$r_o \propto \frac{1}{g_m} \tag{2.14}$$

Therefore, according to the above discussions, two applications for the transmission gate have been assigned. The first with controlling the gate voltage, the variable resistance is utilized in current source to control the bias current and consequently control the output current. The second has been utilized as a resistor that its resistance is function of w and l for voltage source.

Threshold Voltage Temperature Dependence

The significant factor in temperature sensor is the threshold voltage. The threshold voltage in $CMOS$ transistor is dependent on temperature. For temperature monitoring, the temperature alters the frequency of the ring oscillator based on threshold changing with temperature. In this section, the temperature dependency of the threshold voltage has been surveyed. Other applied strategy for $CMOS$-based temperature sensor-driver is related to temperature dependence of the threshold voltage source used as a control voltage. According to the ring oscillator characteristics, the output frequency of the ring oscillator is varied with the control voltage variation. Therefore, in addition to the ring oscillator transistor threshold voltage effect, the temperature dependency of the control voltage impacts the oscillation frequency.

With applying the bias voltage for $NMOS$ device, in the depletion region, the stored charge density is [36]

$$Q_b = \sqrt{2qN_A\epsilon(2\phi_f + V_{SB})} \tag{2.15}$$

Where q, N_A, ϕ_f,and V_{SB} are electric charge, doping density, Fermi level, and substrate bias voltage. The threshold voltage can be calculated following equation 2.16

$$V_t = \phi_{ms} + 2\phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \tag{2.16}$$

Where Q_{ss} is positive charge density, C_{ox} is gate oxide capacitance, and ϕ_{ms} is work-function difference. If V_{SB} is zero, the threshold voltage can be calculated following equation 2.17:

$$V_t = \sqrt{2qN_A\epsilon(2\phi_f)} + \phi_{ms} + 2\phi_f - \frac{Q_{ss}}{C_{ox}} \tag{2.17}$$

Where ϵ is permittivity of the silicon. If ϕ_{ms}, Q_{ss}, and C_{ox} are temperature independence, the differentiation of threshold voltage on temperature (T) is

$$\frac{dV_t}{dT} = \frac{\sqrt{2qN_A\epsilon(2)}}{2C_{ox}\sqrt{\phi_f}} + 2\frac{d\phi_f}{dT} = \frac{d\phi_f}{dT}[2 + \frac{1}{C_{ox}}\sqrt{\frac{qN_A\epsilon}{\phi_f}}] \tag{2.18}$$

Based on Fermi level definition, the Fermi level ϕ_f depends on temperature variation and its derivative is given by:

$$\frac{d\phi_f}{dT} = -\frac{E_g}{2qT} + \frac{\phi_f}{T} = -\frac{1}{T}[\frac{E_g}{2q} - \phi_f] \tag{2.19}$$

Where E_g is energy gap of silicon. Combining equations 2.19 and 2.18 the threshold voltage derivative can be obtained as given in equation 2.20, which provides the threshold voltage dependency on the temperature [36]:

$$\frac{dV_t}{dT} = -\frac{1}{T}[\frac{E_g}{2q} - \phi_f][2 + \frac{1}{C_{ox}}\sqrt{\frac{qN_A\epsilon}{\phi_f}}] \tag{2.20}$$

Thus increasing the temperature will reduce the threshold voltage [36].

Pulse Generator

The produced periodic signal in ring oscillator is close to a pulse shape wave. In order to reach the pulse signal with better specification, the Pulse Generator has been utilized with the ring oscillator. In the first step, the generated signal is compared with V_{DD}, via AND gate, then the output of the AND gate feeds an inverter. The ratio w/l of the $NMOS$ and $PMOS$ are function of the falling and rising time in the pulse wave. The ratios of $(w/l)_p$ and $(w/l)_n$ are other factor used to reach the pulse wave with better waveform shape.

The generated signal in the ring oscillator should provide enough power for the next stages. This may necessitate that the current needed for the next stages should supply the ring oscillator with the other stages. Furthermore, both the load capacitance and resistance in the output of the ring oscillator can affect the frequency of the ring oscillator and may make it unstable. So using Pulse Generator may avoid the unexpected effect from next stage on ring oscillator.

2.1.6 Circuit Design

Voltage Controlled Oscillator

Figure 2.18, taken from tanner tool [21], shows the arrangement of the delay elements of the three delay stages. The current starved inverter has been utilized in the circuit design. In the bias unit, two level voltages are provided for the ring oscillator. The current starved inverter is controlled by the bias unit where variation in the control voltage changes the delay in inverters. Therefore, the output frequency is also controlled by input voltage. The voltage for the upper side of the $PMOS$ transistor is at high level voltages while at the $NMOS$, the upper side is tied to a low level voltage. Those voltage levels are generated with the bias unit. With increasing the input voltage, the upper voltage level falls and the lower level increases. With sweeping the voltage level for $NMOS$ and $PMOS$, the current delay stage is enhanced. Therefore, the frequency is increasing with current variations. Based on the functionality of the current starved ring oscillator, the bias unit should provide biasing control voltage for maximum voltage swing to achieve wider tuning rang. The presented bias unit is an MOS cascode current mirror which the biasing is improved for maximum voltage swing [36].

In the bias unit, the current of the Mn_3 and Mn_5 current mirror structure drives the Mn_4, which perform as the source follower in bias unit. The requirement for Mn_7, which it is biased in margin between the triode region and active region, is [36]

$$V_{DS7} = V_{ov} \tag{2.21}$$

Where Vov is overdrive voltage and V_{DS7} is drain source voltage of $Mn7$. To reach the equation 2.19, the double overdrive voltage on Mn_2 is required and is achieved by the proportional width and length reduction by a factor of four. And the result is threshold voltage exclusion from output [**?**, X34] Therefore the control voltage is independent of threshold voltage and consequently the temperature effect on ring

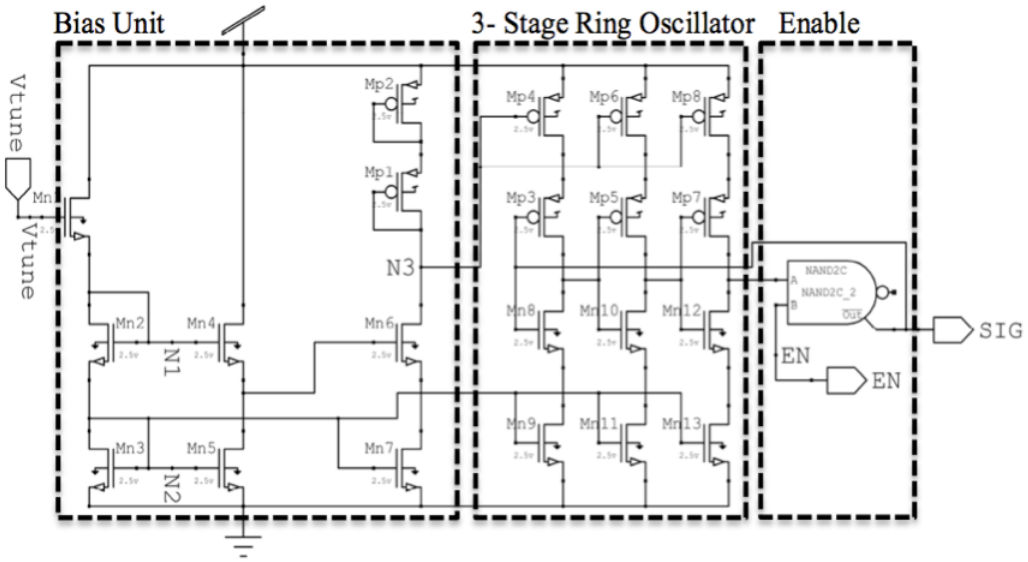

Fig. 2.18. Circuit Design of Current Starved Ring Oscillator with Bias Unit

oscillator is reduced by minimum, because the control voltages of the ring oscillator are supply by V_{N_3} and it is threshold voltage in dependent [36].

To enable the ring oscillator, the AND gate has been placed in the feedback of the ring oscillator [24, 25]. When enabling the signal to high, the system will be closed feedback, and the ring oscillator produces oscillation. Otherwise, the feedback is opened circuited and the ring oscillator is disabled. The enabling signal is provided from the digital sub-system to control the activity of the sensor-driver.

Current Source

Figure 2.19, taken from tanner tool [21], shows the current source circuit used in the design. The output current is function of the resistor of the current source output. According to the current source theory, increasing the resistor reduces the output current and consequently the bias current falls.

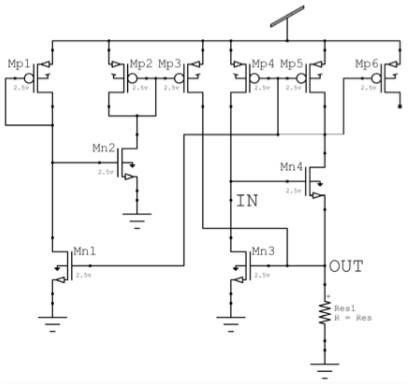

Fig. 2.19. Circuit Design of Current Source

To control bias current, the resistor should be controllable. To control the resistance, the $NMOS$ is utilized as illustrated in Figure 2.20. The gate of the $NMOS$ is controlled with voltage. With the control voltage variation, the resistance of the transmission gate is changed. Therefore, the input voltage controls the resistance of the transmission gate. Other factors such as the width of the device may alter the resistance. The resistor of the current source has been replaced with the $NMOS$ transistor, and. the resistance of the $NMOS$ transistor has been controlled by the out-source voltage. Simultaneously with controlling resistance of $NMOS$ transistor, the output current has been controlled. With this strategy the bias current becomes controllable and as a result, the different ranges of the resistance-based sensor can be derived. The proposed configuration for controllable current source is shown in Figure 2.20, taken from tanner tool [21].

Voltage Shift Level Source

Figure 2.21, taken from tanner tool [21], shows the circuit with 8-bit digital input to control the output voltage level. The 8-bit input should include only one high bit such as 00000001, 00000010.This means that 1 moves from first bit to eighth bit, resulting in an output voltage (V_{ctrl}) that is function of the 1 location within the 8-bit

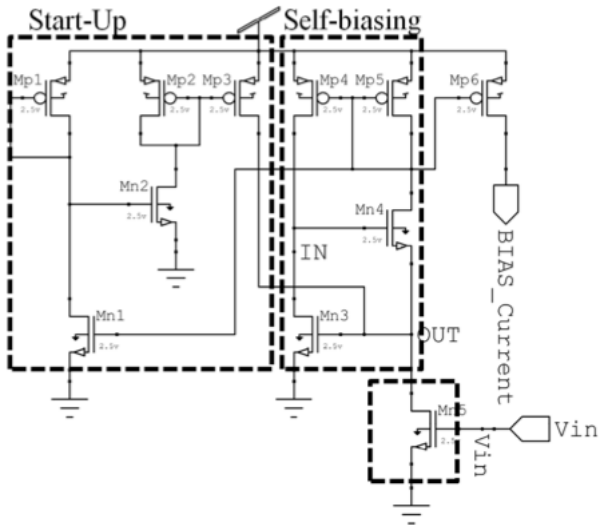

Fig. 2.20. Controllable Current Source

control input. The chain of the transmission gate is connected in serial structure. And each gate is controlled with a $NMOS$ transistor as a switch. When the gate voltage of the $NMOS$ device becomes high, the current passes through all transmission gates before the activated switch. This configuration works as a voltage divider. In fact, the resistance of the chain transmission gate is dependent of the digital input, and it works as a variable resistor that varies the output voltage.

Threshold Voltage Source

Figure 2.22, taken from tanner tool [21], shows the circuit that has been utilized for the threshold voltage source. The output voltage of the circuit is equal to 3 times the threshold voltage. The source gate voltage of the M_1 is equal to the threshold voltage of the $PMOS$ transistor ($\mid V_{tp} \mid$). This voltage applies to the gate of M_2. The resulting gate to source voltage in this case will be 2 V_{tp}, and therefore, the output voltage of the threshold voltage supply is 3$\mid V_{tp} \mid$.

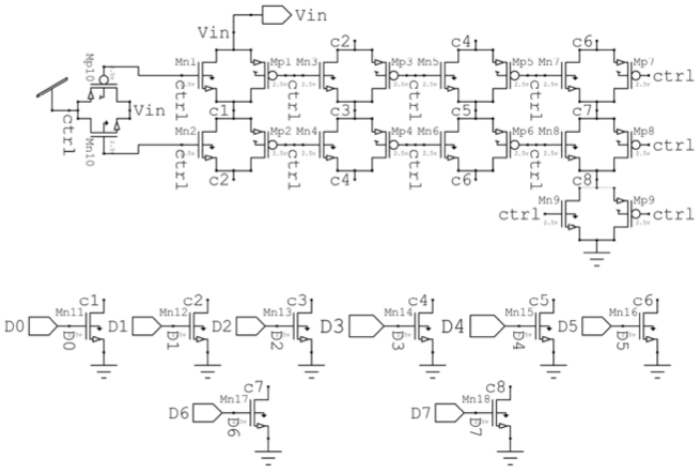

Fig. 2.21. Controllable Voltage Source with Digital Input

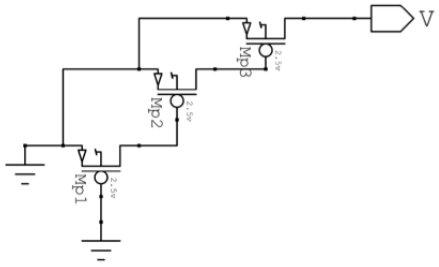

Fig. 2.22. Threshold Voltage Supply

Pulse Generator

The output of the ring oscillator is a periodic signal but it is not completely in pulse shape. According to Figure 2.23, taken from tanner tool [21], with utilizing several logic gates to convert periodic signal to pulse signal, the output of the ring oscillator become more similar to pulse wave [42].

In Figure 2.23, the AND gate compares the output of the ring oscillator with EN signal that is generated from the Digital sub-system. When the EN signal is 0 for a given sensor and AND gate, the output of the pulse generator is 0. As soon as the enable signal goes high, the ring oscillator will be activated and a periodic signal

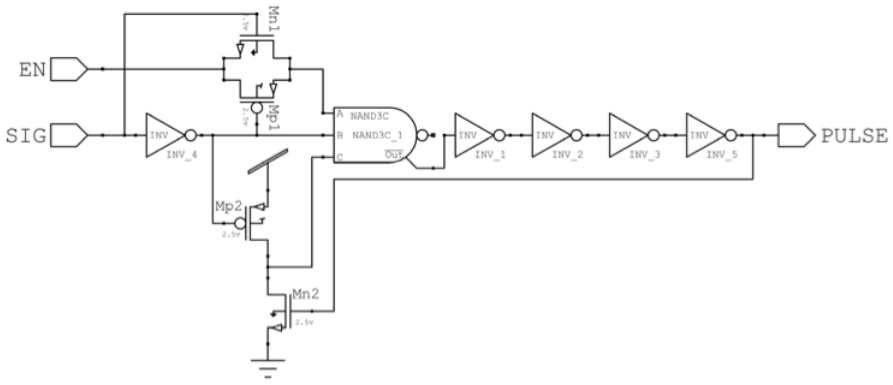

Fig. 2.23. Pulse Generator Circuit Design

based on input voltage will be generated. When the periodic signal is compared with 1, the signal goes high, and the AND gate output goes low. The AND gate output will be high when the signal of ring oscillator is zero.

After enabling the ring oscillator and pulse generator, four inverters are used to generate the rising and filling edges of the periodic signal. In fact, based on the width proportion of $NMOS$ and $PMOS$ devices, the first invertor speeds up the rising and falling periodic time, while the second inverter switches it back to its previous state at faster rise/fall times. This design has led to a fast switching periodic pulse wave for the controller unit.

2.2 Digital Sub-System

2.2.1 Design Overview

There are several significant functions have been defined for the digital sub-system, consisting of the SMU, Shift Register module, and Counter module. The first task was to manage the sensor ordering and signal acquisition. To manage sensors, the SMU produces enable signals to control and enable the sensors in order. For each

sensor, one input has been defined for the SMU. Enabling signals and input signals from sensors are based on system demand. Figure 2.24 details the digital sub-system diagram.

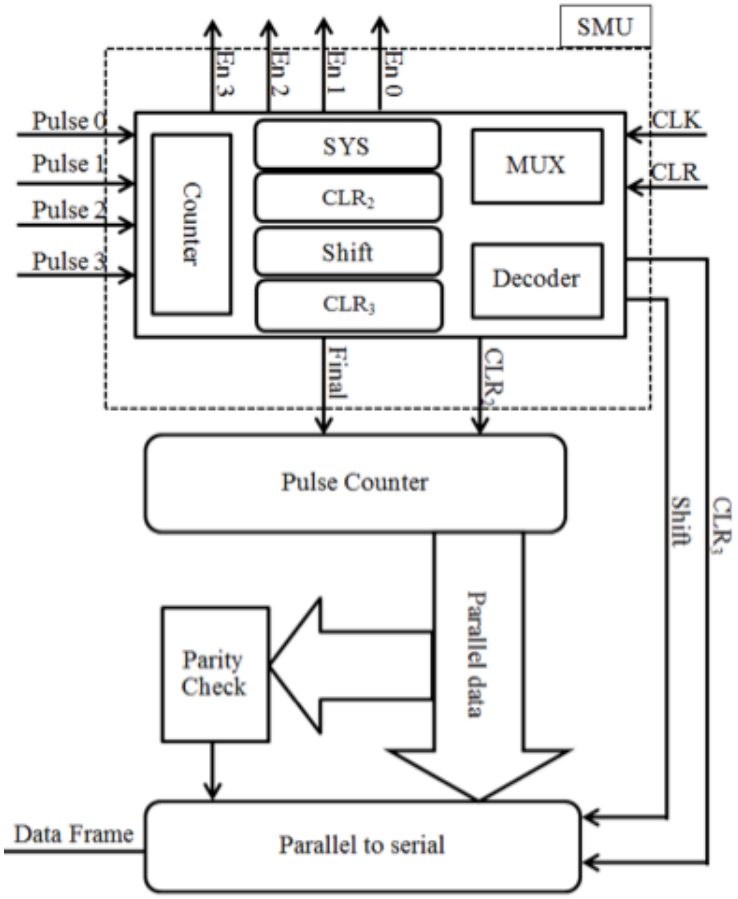

Fig. 2.24. Digital Sub-System Block Diagram

After signals acquisition, the received signals from the sensor in the analog sub-system unit are processed and interfaced to the digital sub-system. In the SMU, the captured signal has been put on at the last stage to transmit for the counter module, which counts the number of obtained pulses for each time period. After each counting process, the counter module should be reset. For this purpose, the SMU generates specific clear signals to control the counter module. After the counting process is

completed, the SMU converts the parallel outputs of counter in serial form via the shift register module. To control the start and stop time bits for the shift register module, the SMU produces two control signals, clear and shift, as a third function of the digital sub-system.

2.2.2 System Management Unit (SMU)

The significant module in the digital sub-system is the SMU because all functions in system are managed and processed with this module. Four internal control signals, system signal (SYS), clear signal (CLR_2), $SHIFT$, and second clear (CLR_3), have been assigned for SMU.

For timing control of the SMU, the SYS and CLR_2 signal provide the different logic levels, one or zero, so that the SMU manages and controls the pre-defined occurrence in the modules of the sub-systems based on logic level changing. Each sixteen-clock period, the changes are observed in SYS and CLR_2 signals. The SMU is sensitive to high level of SYS and low level of CLR_2. The main task of these two signals is to enable the signal for analog sub-system and then encode the generated pulses in the sensor-drivers as output of the SMU.

To generate the enabling signal and process the final signal, the Multiplexer and Decoder sample the CLR_2 and SYS level. The CLR_2 state has been defined one but each sixteen-clock cycle, for one clock cycle, its state is changed to zero. And then the state change in SYS occurs after three clocks cycle. Because the SMU is sensitive to high logic level of SYS, the SYS becomes high three clocks after the CLR_2 signal falling edge. Therefore, the time between CLR_3 falling and SYS rising is 1 clock. During these three clocks, CLR_3 falling, one clock between CLR_3 falling and SYS rising, and SYS rising, the Decoder generates the enable signal and Multiplexer

transmits the obtained pulse signal to the final output. It means that each sensor is monitored for 3 clocks during 64 clocks.

Although sensors are monitored for 2 clocks, the obtained pulses in the last clock are transmitted to the final output. It means that each sensor driver has one clock to reach stability after enabling. The necessity of time interval for stability comes from the topology of the sensor-drivers. The sensor-drivers have been designed based one frequency variation. In order to achieve this purpose the ring oscillator is utilized. Based on the ring oscillator functionality, it needs time to reach stability after applying voltage to generate periodic signal. Therefore, the SMU makes a time interval for reaching stability. After that the obtained pulse signal from analog sub-system is put over the final output.

The other segment of the SMU is the 4-bit counter. The desired cycle for one sensor enabling, reading, counting the pulses, and data packing is 16 clocks. To count the clock, the four-bit counter has been utilized. The counter manages the SMU signal and consequently all orders in the system.

The other defined task for the CLR_3 is resetting the 8-bit counter. After preparing the final signal, the 8-bit counter module counts the pulses, which are carried with the final signal. The final signal as an output of SMU carries the obtained pulses of each sensor. In structure of the final signal, in each sixteen clocks, the final signal includes the obtained pulses for one clock. Therefore, before starting to count the carried pulses, the 8-bit counter has to be reset for a new cycle. According to the method of the system arrangement, after CLR_3 falling then rising, the final signals starts to carry pulses for one clock. The falling and then rising in CLR_3 signal generates zero state for the CLR_3 that it is suitable for counter clearing because this zero state exactly occurs before starting to count the new obtained pulses.

After counting the pulses, the 8-bit counter make eight parallel data output that shows the number of the carried pulses in one clock. The counter keeps the outputs until next zero in CLR_3. The time interval between counting finishing and resetting is 14 clocks. Therefore, during the time interval, the parallel data should be shifted and outputted in serial form. For this purpose, two signals are provided by the SMU to start and end the parallel to serial conversion. So after finishing data counting, the Shift signal is used to generate a zero to start converting parallel to serial data. Based on the number of the transmitted bits, the CLR_3 signal should be generated to reset the shift register module. The desired bit in data package in this work is 11. Therefore, 11 clocks after producing zero state in the $SHIFT$ signal, the CLR_3 signal fall to zero from high logic level.

2.2.3 8-bit Pulse Counter

The final output of the SMU carries the sensor-driver pulses for one clock cycle within 16 clocks. The carried pulses act as clock for the 8-bit counter and counter count pulses number once in each 16 clocks. To start new cycle of counting, the counter should be reset once every 16 clocks. The exact time for resetting is determined from the Controller module. The clear signal is then sent to the counter module from the SMU. The CLR_2 signal determines the time of resetting. When CLR_2 falls to zero state, the counter modules are then reset. The topology of the 8-bit counter is D-flip-flop based circuits. The pulses are assigned as clocks for the first stage counter. The output of each stage is one bit that it can be zero or one. The inverting output of each D-flip-flop feedbacks to the input and is assigned as clock for next step.

2.2.4 Shift Register

The shift register is utilized for converting the parallel data of the 8-bit counter to serial data with serial protocol. After counting the number of pulses, the SMU

provides two signals to control the shift register. The shift register needs a trigger to start transmitting bits into serial format, while the other signal resets the shift register module. Immediately after completing the counter module task, the shift register should start shifting the outputs of the counter module.

To trigger the shift register module, the SMU generates zero for a clock cycle. The shift register module then starts shifting the data in serial configuration and makes a package of the data that includes start bit, 8-bit of counter output, parity check, and stop bit. All data package is eleven bits so the stop signal or reset signal should trigger the eleven clock bits after the start signal, then it waits for the next start signal for the next cycle. The start signal is called $SHIFT$ and stop signal is called CLR_3.

2.2.5 Theory and Design

System Management Unit (SMU)

To determine the trigger time for the assigned signal of the SMU, the 4-bit outputs of the inside counter in the SMU module should be compared together. The trigger signal occurs based on the logic data from the comparator unit. The comparator circuit is shown in Figure 2.25, taken from tanner tool [41], with the logic function given in 2.22. The derivation of the comparison circuit is

$$Y = \overline{A + B + C + D} \tag{2.22}$$

A is first bit of the counter (b_0), B is b_1, C is b_2, and D is b_3. The truth table of the comparison logic for SMU control signals is shown in Table 2.1.

Table 2.1
Control Signal of SMU

Signal	b_0	b_1	b_2	b_3	**Y**
CLR_3	0	1	0	1	1
CLR_2	0	1	1	0	1
SYS	1	0	0	1	1
SHIFT	1	0	1	0	1

The first 10 clocks is the time interval to set the signals trigger order. After signal setting each 16 clocks the control signals are generated sequentially.

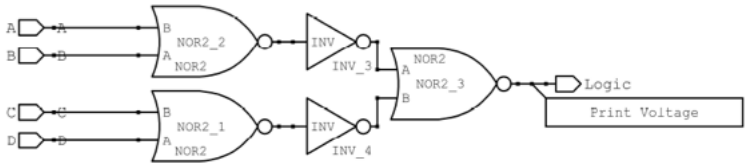

Fig. 2.25. Standard Cell Structure of Signal Delay Calculator Core

Instead of using standard logic gates, the combinational logic is utilized to reduce the hardware involved with devices, and consequently reduce the power consumption. Two approaches were utilized: the first is using NOR structure and second is using NAND structure. Figure 2.26, taken from tanner tool [21], shows the NOR structure. The delay resulted from this structure is more than standard cell arrangement.

Figure 2.27, taken from tanner tool [21], shows the complementary CMOC circuit for the NAND structure design. The NAND structure is faster than other design. The NOR structure with four fan-in is equivalent to the Inverter-NAND4-Inverter. The proposed NAND structure produces delay less than standard cells and NOR structure [42].

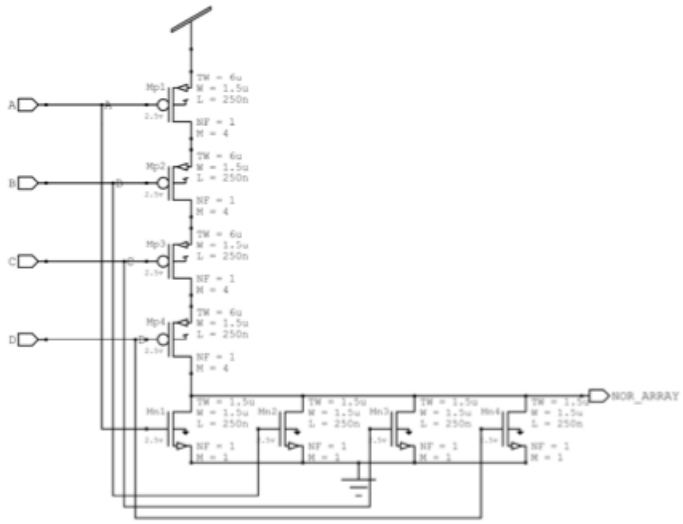

Fig. 2.26. NOR structure of Signal Delay Calculator Core

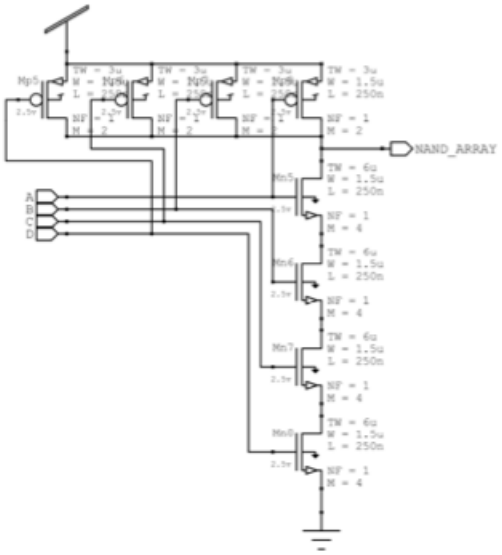

Fig. 2.27. NAND structure of Signal Delay Calculator Core

After generating the control signals, the enabling signal should be formed and the output signal is prepared to transmit to the counter module. The signal enabling and processing are dependent on each other. To enable the sensors, the decoder generates the enabling signal based on the SYS and CLR_2 signals. The decoder is enabled

between the triggering signal of SYS and CLR_2. The enabled logic of the decoder is shown in Figure 2.28, taken from tanner tool [21].

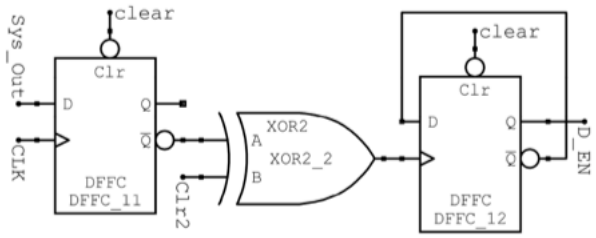

Fig. 2.28. Enable Generator for Decoder

The 2 to 4 decoder decodes two bits that are constructed base on the CLR_2. The outputs of decoder enable the sensors. Simultaneously, the two bit inputs of the decoder are selected for the Multiplexor. The inputs of the Multiplexor are pulses from sensor. Therefore, when the sensor is enabled, its output is chosen by Multiplexer. The logic of the Decoder input and also the selectors of the multiplexer are shown in Figure 2.29, taken from tanner tool [21].

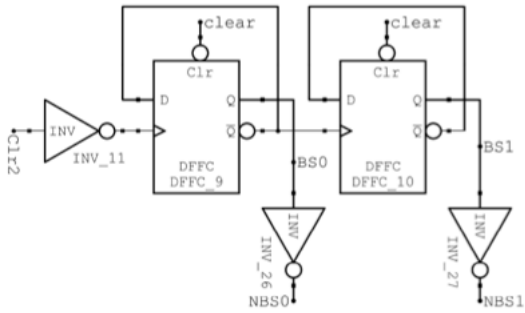

Fig. 2.29. Selector Generator for MUX

The 2 to 4 decoder, which is illustrated in Figure 2.30, taken from tanner tool [21], is utilized to form enable signal. The decoder enable with the signal that is formed based on SYS and CLR_2. Then based on the state of input bits, the 4-bit outputs

are generated. In the output of the decoder, the high logic level moves from first bit to last bit and consequently enable sensors in order. The state of the enable signal is shown in following Table 2.2.

Table 2.2
Decoder Logic

A_0	A_1	EN_0	EN_1	EN_2	$EN3$
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

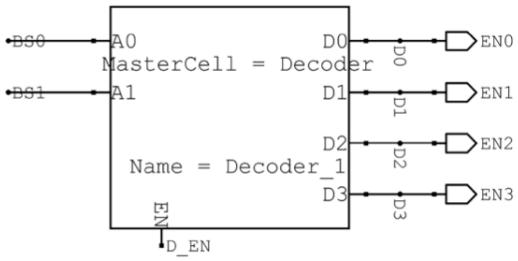

Fig. 2.30. 2 to 4 Decoder

After enabling the sensor, the sensor pulse-output is chosen with Multiplexer. The captured pulses from the Sensor and with SYS signal pulses are then captured for 3 clocks, and based on the defined method, the counter module is assigned just for one clock cycle. The time for counting the pulses is correlated with SYS signal. The utilized logic is illustrated in Figure 2.31, taken from tanner tool [21].

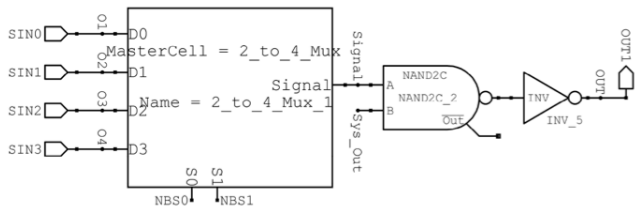

Fig. 2.31. Final Signal Generator

8-bit Pulse Counter

The 4-bit counter is utilized in two modules of the digital sub-system. Figure 2.32, taken from tanner tool [21], shows the structure of the D flip-flop arrangement to count the input of the counter. The clock in the first D flip-flop is fed to the input of the counter.

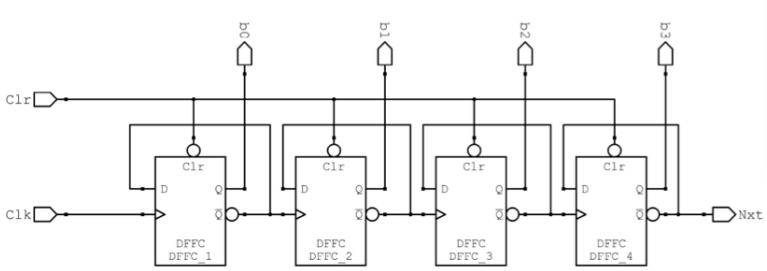

Fig. 2.32. 4-bit Counter

The 8-bit counter was formed from combining two 4-bit counters. The pulses, which are obtained from sensors and processed in the SMU, are the inputs of the 8-bit counter. The clear signal of the counter is provided with the Controller module. The SMU generates the CLR_2 to reset the 8-bit counter once each sixteen clocks.

Shift Register

After counting the number of the pulses, in the shift register module, the parallel 8-bit output of the counter module is converted to serial data arrangement. Figure 2.33, taken from tanner tool [21], shows the logic of the shift register module. The shift register starts with Shift signal triggering that is provided by SMU. With the first clock, the first bit is put on the output. Then with each clock, the previous bit is shifted forward and replaced by the next bit. This process continues for 11 bits. With CLR_3 signal the shift register is then reset and stayed for next data package.

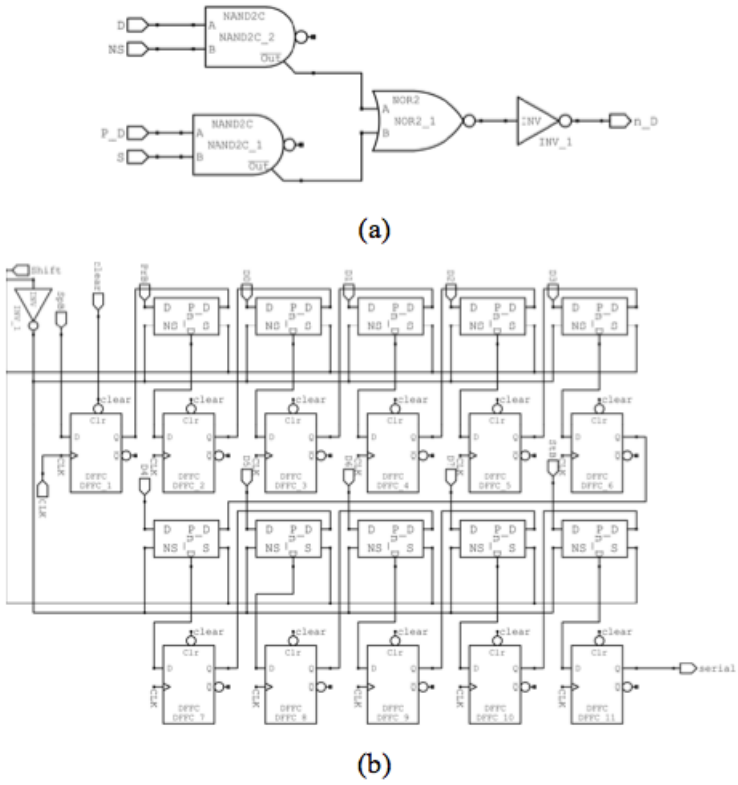

Fig. 2.33. a) Compression Cell in Shift Register b) Schematic of Shift Register

3. SIMULATION RESULTS AND DISCUSSION

The proposed system, consisting of the digital and analog subsystems, has been simulated with Tanner Tools for 250 nm CMOS technology, while using Mentor Graphics Tools for 180nm CMOS technology [21, 22]. The two different technologies were pursued in order to study the effect of the device physics on the frequency of the ring oscillator and its linearity range and performance, power consumption, and power supply voltage level. Furthermore, the two technologies were performed to address the design validity for different technologies.

3.1 Digital Sub-System

This subsystem includes the SMU (System management Unit), Counter, and shift register. Its main function is to read sensor data, convert the analog data sensor to digital form, manage the power usage, enable/disable the sensors sequentially, and construct the output data frame.

3.1.1 The System Management Unit (SMU)

The SMU setup that was designed and tested is given in Figure 3.1, which consists of the 4-bit counter, 2-to-4 decoder, 4-to-1 MUX, the comparator units, selector generator for MUX, and 2-bit input generator for decoder. The comparators were designed with $NAND$, NOR, and standard logic cells architectures, searching for the highest speed performance that may be followed in the system. The $NAND$ architecture was chosen for that purpose.

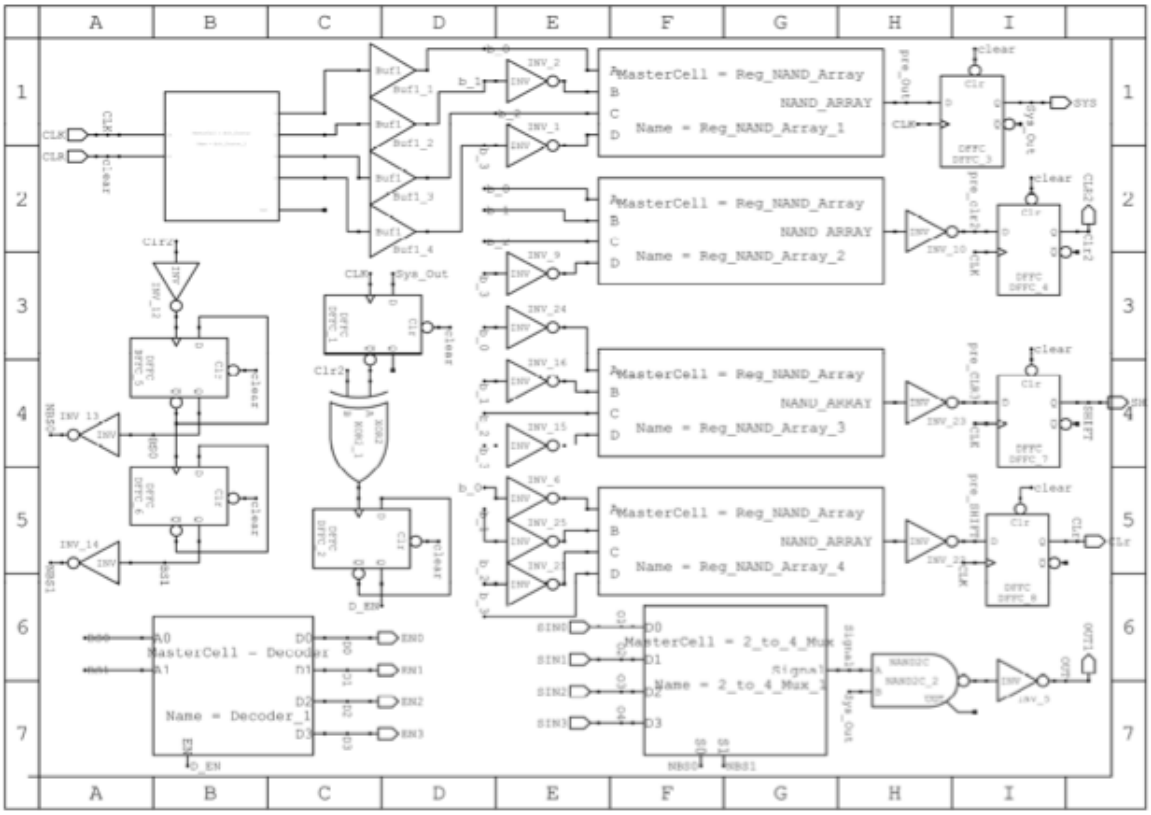

Fig. 3.1. Setup of the SMU Module

Figure 3.2 shows the simulation results of the three rise time performances for the comparator architectures. The comparator circuit was used in four control signals of the SMU as indicated in Table III of chapter 2. There signals are: CLR_3, CLR_2, SYS, and $SHIFT$. These control signals were simulated with Tanner tools, and results were obtained as in Figure 35. With CLR_2 and SYS, the sensors may be enabled sequentially, and then the data may be captured, and then transmitted to the counter. The sys signal within the SMU manages and arranges the other units of the system, including MUX and Decoder.

Figure 3.3 (a) shows the captured signal for SYS, a SMU signal that manages and arranges the other units of the system. From the system starting time (following

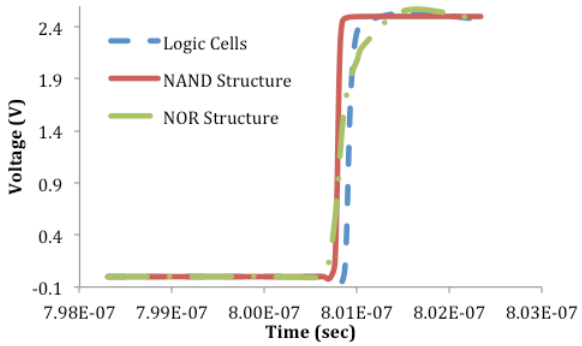

Fig. 3.2. The Comparator Simulation Results

a clear signal), the SYS signal will be triggered for the first time after 10 clock cycles, and then the state of the SYS signal will change from low to high for one clock every 16 clocks.

The second signal of the SMU is CLR_2 that is illustrated in Figure 3.3(b). This signal shows the change of the CLR_2 state from high to low for one clock cycle per 16 clocks. The first time when the CLR_2 is triggered, there were 2 clocks sooner than SYS signal trigger, and this forms the correlation between SYS and CLR_2 within the timing diagram.

Based on the defined strategy, the decoder should be enabled between the two falling edge CLR_2 and SYS signals. With this, as shown in Figure 3.3(c) the decoder is enabled for 3 clocks out of 16 clocks. That relation between the SYS, CLR_2, and the decoder enable is driven within the hardware presented in Chapter 2.

When the decoder is enabled, one of the four outputs of decoder will become high. After the enable signal is reset to zero, all outputs will reset as well. Therefore with this approach, the sensor-enable-signals can be generated. The sensor-enable-signals only have activated the sensor for 3 clocks per 16 clocks. With two-bit input of the decoder are allocated with CLR_2 to enable the sensors. 3.3(d and e) shows the two

inputs of the decoder. The inputs can be generated based on CLR_2 signal. For each rising edge of the CLR_2, the states of the decoder inputs will change. The four state decoder inputs 00, 01, 10, and 11 are generated based on the CLR_2. When the 00 state is applied, the first output will turn high while the others are remained zeros. The 01 input will activate the second output, Likewise, the other two inputs, 10 and 11. Activating the outputs, there are four decoder outputs enabling the sensors sequentially. The output of the decoder is shown in Figure 3.3(f, h, j, and l). Each output is formed with decoder-enable-signal and two-bit inputs of the decoder. For example, when the first enable signal is generated, the first bit of decoder input is turned to high, and the second bit is reset to zero. Therefore, the second output of the decoder will be raised to 1 for 3 clock cycles. During this period, other enable signals are remained zeros. Therefore, each sensor is enabled for 3 clocks in every 64 clocks.

After enabling the sensors, immediately the output of the sensor will be captured and processed in the SMU. For this purpose, the output of the sensor-driver is connected to the multiplexer. When the sensor is enabled by the decoder, the multiplexer will select the enabled sensor. The multiplexer includes two selectors to select one of four inputs. The selector signals of the multiplexer are the same inputs of the decoder. After selecting each sensor, the pulse wave of the sensor has become an output of multiplexer.

Final output of the SMU has been generated based on the MUX output. Each 16 clocks, the MUX transmits the pulse wave of the sensor-drivers into its output in order. Therefore, the output of the MUX pulses is fed by the sensor-drivers. Due to the output stability of the MUX, the third pulse was only counted, while the first two pulses were before reaching the steady state of the MUX outputs. To remove these two pulses, the output of the MUX was compared with SYS signal. The comparator gate between the MUX output and SYS was AND gate. The obtained result of the

comparison is shown in Figure 3.3(n). IN order to count the number of pulses, the final signal has been sent to counter module.

Figure 3.3(o) shows the shift signal. To control the starting time of the shift register, the Shift signal has been provided for shift register module. The shift signal was triggered immediately after SYS falling edge. After 11 clocks from trigger of $SHIFT$ signal, the CLR_3 signal was generated by the SMU to stop the shift register module. As shown in Figure 3.3(p), in order to stop and reset the shift register, the CLR_3 signal has been produced after 11 clocks from the rising edge of the shift signal.

3.1.2 Pulse Counter

After processing the data in the SMU module, the captured pulses from sensor-driver were transmitted to counter module. The counter module counts the received pulses and keeps it for 11 clocks cycle in order to convert it to serial data instead of parallel. So, the timing adjustment in this process is a significant task for the SMU module. For this purpose, the SMU has provided CLR_2 for counter resetting. The MUX output pulses are generated when the SYS is turned high. Therefor, 3 stages have existed for counter module function as shown in Figure 3.4. The first stage when the counter module is reset with the falling edge of the CLR_2. Then with the SYS rising edge, the counter module started counting the pulses. In the last stage, the SYS signal is reset to zero, and the counter stops counting, keeping the output until the next falling edge of the CLR_2.

3.2 Analog Sub-System

This subsystem consists of the sensor-drivers that drive the resistance-based sensors, capacitance-based sensors, and $CMOS$-based temperature sensor. The com-

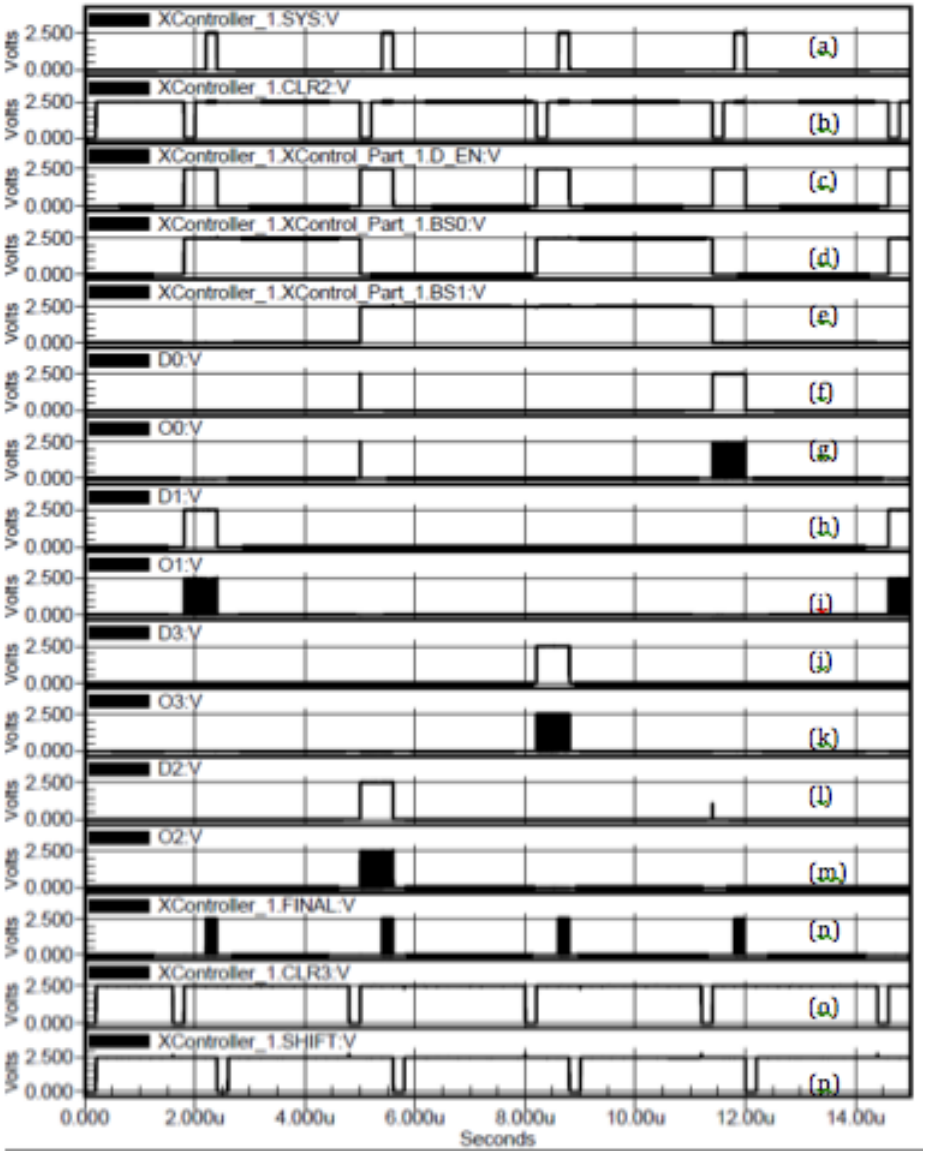

Fig. 3.3. a) SYS Signal Trigger b) Obtained Signal for CLR_2 c) Decoder Enable Signal d and e) 2-Bit Input of the Decoder f, h, j, and l) Four Parallel Output of the Decoder, the Enable Signal of Sensors g, i, k, and m) MUX output n) Final Output of the SMU that Carries the Captured Pulses from Sensor-Driver o) Shift Signal p) CLR_3 Signal

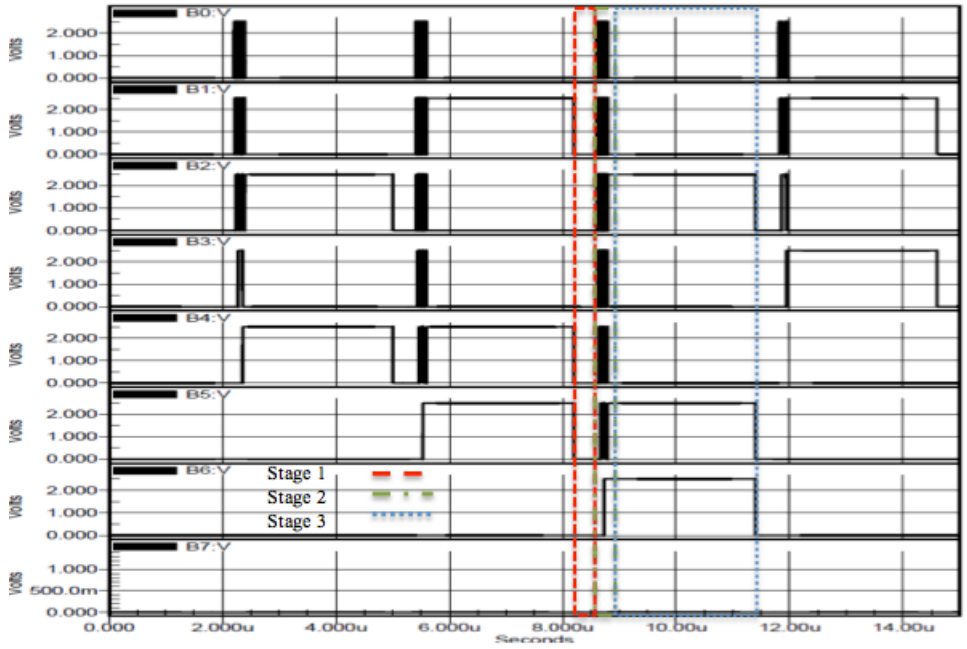

Fig. 3.4. 8-Bit Parallel Output of the Counter Module

ponents of the sensor-drivers includes temperature sensitive VCO that detect the temperature variation, and another insensitive VCO that translate capacitive and resistive quantities into frequencies. The analog subsystem also includes the controllable current source that bias the sensor circuitries, 8-bit voltage source that control the current source, threshold voltage source that feed the temperature sensor, and pulse generator that translate the VCO frequency into pulses. These components were designed and simulated with 180 nm and 250 nm technologies.

3.2.1 Voltage Controlled Oscillator (VCO)

The simulated VCO, which consists of bias unit, delay elements, and enabling unit, is shown in Figure 3.5. The ratio of the w/l for the $NMOS$s and $PMOS$s of the bias unit is listed in Table3.1.

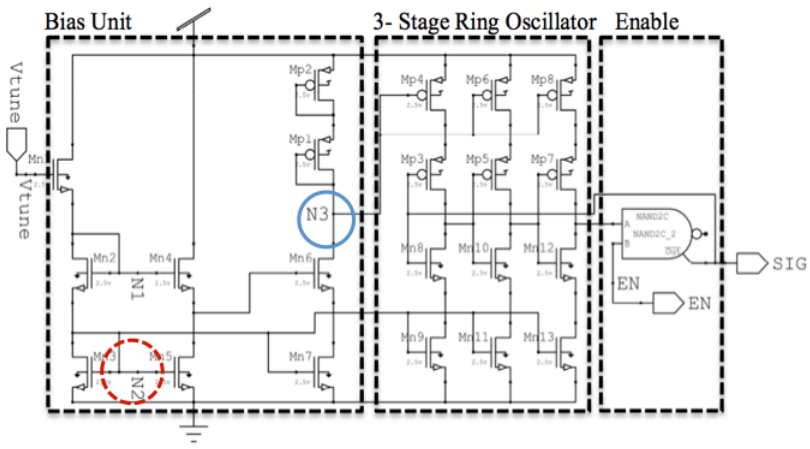

Fig. 3.5. Simulated Circuit of Ring Oscillator

Table 3.1
w/l Ratio of the Transistor in the Bias Unit

	$w(\mu m)$	$l(\mu m)$
Mn_1	0.5	0.5
Mn_2	0.5	2
$Mn_3, Mn_4, Mn_5, Mn_6, Mn_7$	0.5	0.5
Mp_1, Mp_2	0.5	0.5

The bias unit provides two high swing levels of the voltages at node N_2 and N_3, for upper side transistors and lower side transistors for controlling the current of the delay stages. In Figure 3.6, the voltage swings for $PMOS$ and $NMOS$ transistors were shown while the tune voltage sweeps from 0 to 2.5 V. The solid line shows the control voltage of upper side and the dash line illustrated the lower side voltage of the delay stage. To achieve a range of frequencies, the delay stage is controlled from the bias unit. The relation between the upper and lower biasing voltages as function of the tune voltage is given in Figure 3.6. Following this relationship, one can design for wide range of tuning voltage by selecting the bias voltages of both devices.

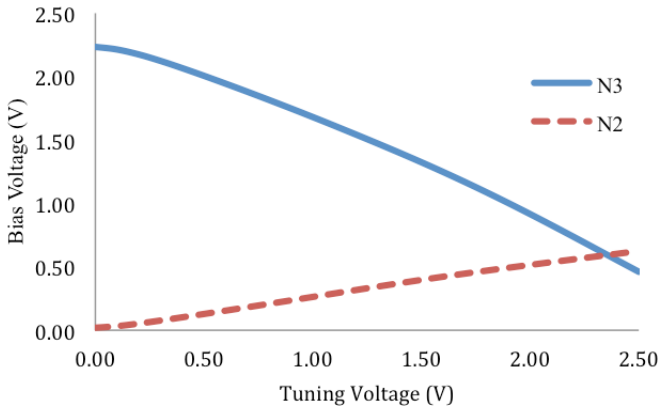

Fig. 3.6. Control Voltage Swings Providing by Bias Unit, for Upper Side and Lower Side of Delay Elements

Figure 3.9 shows the effect of sweeping tune voltage from 0 V to 2.5 V on current with the impact on current enhancement. Before tune voltage reaching 1 V, the current of stages are zero because the upper and lower sides transistors are in triode region. With passing 1 V, the current is enhanced by increasing its lower side voltage, and simultaneously decreasing the upper side as shown in Figure 3.6.

The output of the ring oscillator is dependent on the current of the delay units. This shows that the frequency of the ring oscillator is function of the input voltage and the upper and lower side voltages of delay stage. As shown in Figure 3.7, the generated output is periodical signal at 2 V. The dash line shows that the obtained signal serves as inputs to the AND gate. The voltage level of the signal has not reached the maximum and minimum voltage. The AND gate makes up the voltage level of the signal. The output of the AND gate is the output of the ring oscillator that is shown in solid line.

With control voltage sweeping from 0 to 2.5 V, the output frequency of the ring oscillator is increasing. The obtained result from Tanner tools, which are illustrated in Figure 3.9, shows the two operating regions where the frequency changes smooth

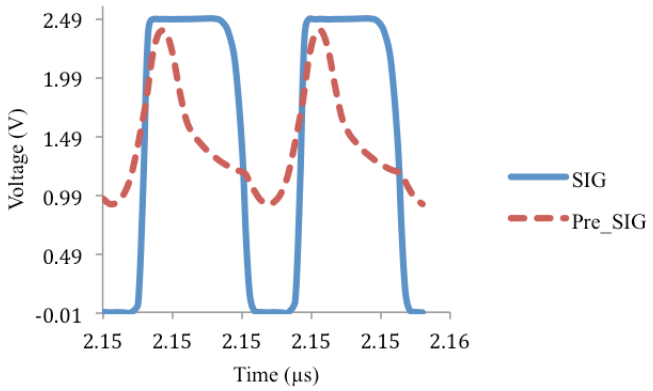

Fig. 3.7. Obtained Result at 2 V for Voltage Control for 250 nm CMOS Technology

or being constant, and the frequency changes linearly with tune voltage variation. When input voltage was less than 1 V, the transistors were in triode region, and the voltage variation has not been effected with the output frequency and it remains constant. With increasing the tune voltage, the output frequencies are varied linearly for the rest of voltage range. When the voltage is higher than 1 V, the transistors have operated at the active region, indicating that the best tuning range for the ring oscillator was between 1 and 2.5 V. In this range, the frequency has varied linearly from 20 MHZ to 207 MHz.

The results of the 180 nm technology were obtained using Mentor Graphics tools while the system is derived with 1.8 V. The obtained waveforms are shown in Figure 3.8 for 1 V input voltage. The dash line shows the obtain signal as an input of the AND gate. The voltage level of the signal has not reach the maximum and minimum voltages. The AND gate makes up the voltage level of the signal. The output of the AND gate is the output of the ring oscillator that is shown in solid line.

In 180 nm $CMOS$ technology, with control voltage sweeping from 0 to 1.8 V, the output frequency of the ring oscillator is increasing. The obtained results as illustrated in Figure 3.9 show that there are two operating regions, one when the

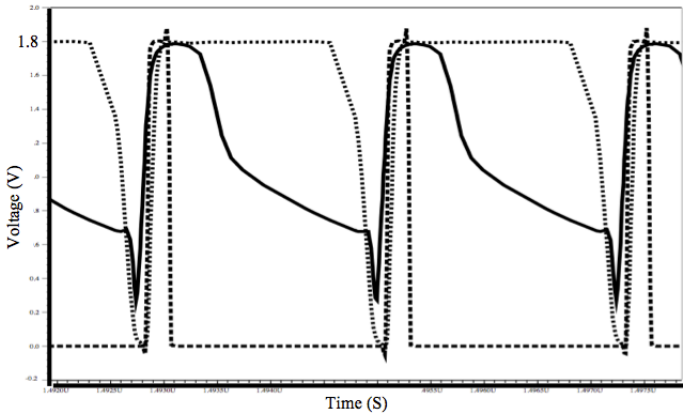

Fig. 3.8. Obtained Result at 1 V for Voltage Control for 180 nm CMOS Technology

frequency changes linearly, while the other being constant. When the input voltage was less than 0.4 V, the transistors were in triode region, and the voltage variation has no effect on the output frequency and, therefore, it is constant. With increasing the tune voltage, the frequency starts increasing linearly by increasing the tuning voltage. The output frequency of VCO linearly changes from 0 to 446 MHz.

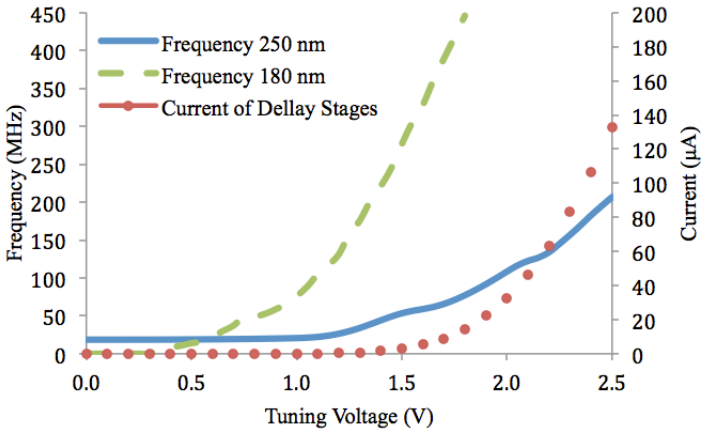

Fig. 3.9. Tuning Range of the Ring Oscillator and Current of Delay Stages

Figure 3.9 show similar patterns for the frequency of the ring oscillator and current of delay stages in the ring oscillator. Since the frequency is function of the current,

the frequency will be generated following the tune voltage delay. The difference in the frequency range is attributed to the device capacitance from the 250 nm and 180 nm technologies. The equivalent capacitance of a following delay stage in the ring oscillator is inversely proportional with the frequency equation 2.3. The capacitance surface area is determined by width and length of the $CMOS$ transistors and physical layout technology. Because features are smaller in the 180 nm $CMOS$ technology, the capacitance may reach smaller values as compared with the 250 nm $CMOS$ technology. Therefore, in 180 nm $CMOS$ technology, the ring oscillator can produce a wider frequency range than the case in 250 nm $CMOS$ technology.

The other key factor in VCO is the temperature sensitivity. To achieve accurate results in of a wide temperature operation region, the VCO should be less sensitive to temperature. At room temperature (25°C), when the tune voltage is 1.8V, the obtained frequency is 77 MHz. As shown in Figure 3.10, when temperature changes between 0°C and 50°C, the output frequency produces 1.9% error in worth case, while for basic type of the 3-stage ring oscillator, the frequency is changed up to 10% [39]. Because the ring oscillator frequency depends on the tuning voltage, the bias unit was designed to overcome the temperature variation effect.

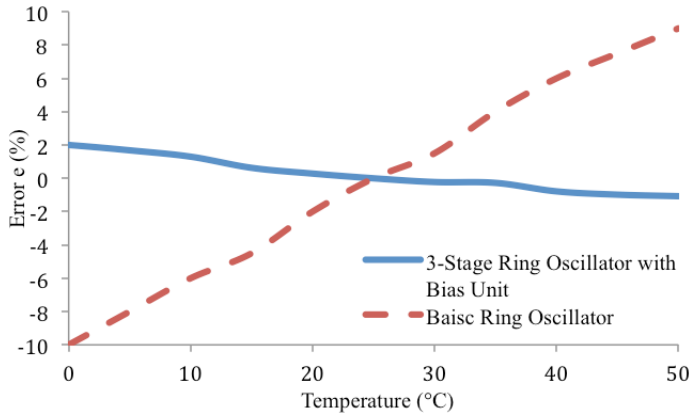

Fig. 3.10. Frequency Error with Temperature Variation at 1.8 V

3.2.2 The Current Source Biasing Circuit

To drive the resistance-based sensors, the controllable self-biasing current source, which is shown in Figure 3.11, was presented to drive the sensors for various applications. The voltage, which is built by current source and sensor resistivity, feed the ring oscillator for voltage conversion to pulses wave frequency and determining the sensors state. The simulated self-biasing current source results show that the current passed through the node $'OUT'$ is dependent on the resistors resistivity. In those schematics, the resistor is derived with the threshold voltage of the Mn_3 device, resulting in an output current $'OUT'$ that is independent on the input current $'IN'$ and the power-supply voltage. The current source is utilized to drive sensors and form the input voltage for VCO. The ratio of the w/l used in simulation for the various devices are given in Table 3.2.

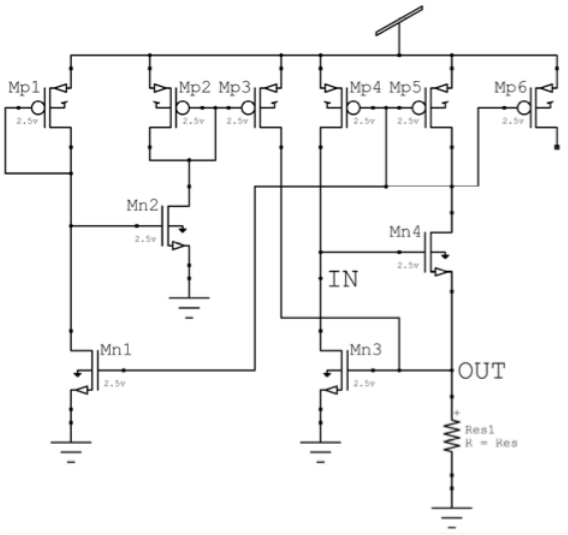

Fig. 3.11. Self-Biasing Current Source

Figure 3.13(a) shows the dependency of the current output versus increasing resistance. The obtained results show that the output current falls with increasing in the resistance.

Table 3.2
Size of Width and Length of Transistors in Current Source

	$w(\mu m)$	$l(\mu m)$
$Mn_1, Mn_3, and Mn_4$	3	0.25
Mn_2	0.5	0.25
Mp_1, Mp_2, Mp_3	0.5	0.25
Mp_4, Mp_5, Mp_6	3	0.5

The resistor in Figure 3.11 is replaced with $NMOS$ transistor, which its resistivity is controllable with the input voltage. Figure 3.12 shows the new configuration of the current source. The voltage in node $'OUT'$ is 750 mV, so the drain voltage of the added transistor is derived with 750 mV. With this design, both the drain current of the Mn_5 and the $'OUT'$ current of the current source are function of V_{in}, resulting in a $'bias - current'$ that is dependent on V_{in}.

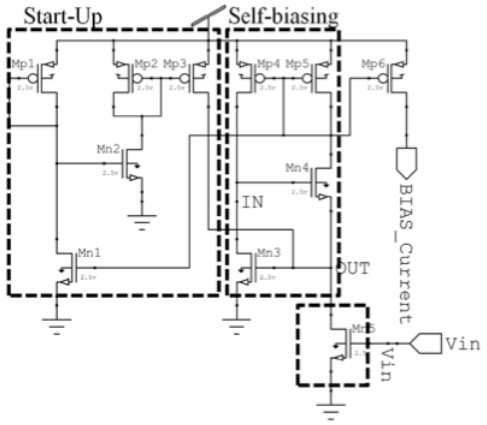

Fig. 3.12. the Controllable Current Source

According to functionality of the added transistor, the resistance of the transistor falls with increasing V_{in}. Based on the captured result for current source, with de-

creasing the resistance, the current output is increasing. Therefore, with increasing V_{in}, the output current increases. The obtained result, which is illustrated in Figure 3.13, has confirmed the above conclusions.

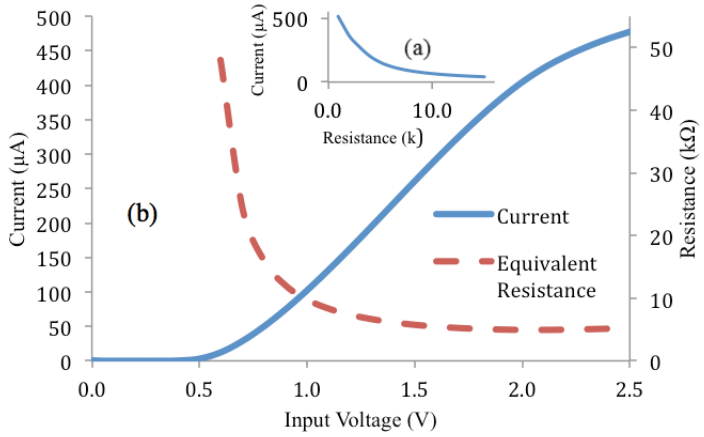

Fig. 3.13. Bias Currents of Input Voltage Controlled Current Source. a) Bias Current vs. Bias Resistance. b) Equivalent Resistivity of NMOS Transistor vs. Input Voltage (Dotted Line) and Current Vs. Input Voltage (Solid Line)

3.2.3 Voltage Shift Level Circuit

The schematic of the level shift circuit is presented in Figure 3.14, which consists of chain of the transmission gates. The output of the voltage level shift circuit feeds the input voltage for controllable current source. The output voltage level is shifted to next or previous state by 8-bit digital input, and consequently, the biasing current is determined by level of the voltage output. The level of the output voltage is built based on the number of the gates involving in circuit and their ratio of the w/l. The number of the gates is figuring out from the digital input. And also the w/l ratios are listed in Table 3.3.

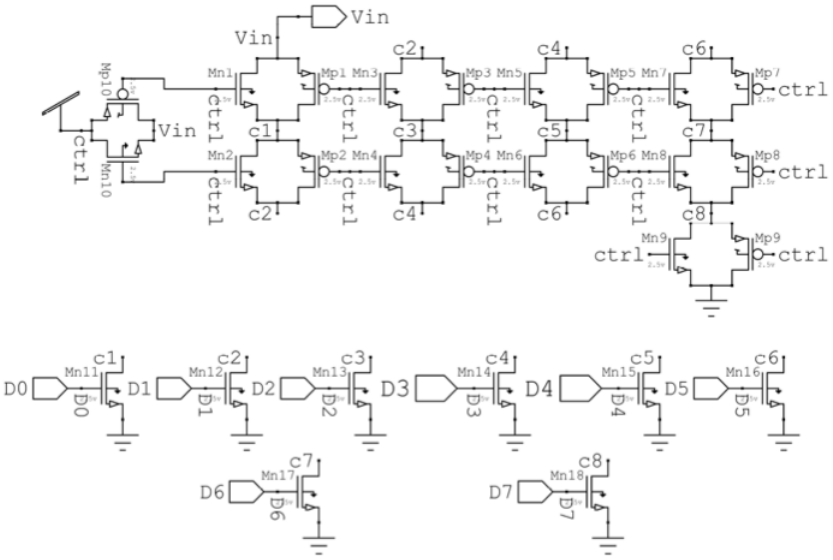

Fig. 3.14. Schematic of Voltage Level Shift Circuit

Table 3.3
w/l Ratio for the Transmission Gates

	$w(\mu m)$	$l(\mu m)$
$Mn_1, Mp_1, Mn_2, and Mp_2$	4	0.25
$Mn_3, Mp_3, Mn_4, and Mp_4$	3	0.25
$Mn_5 and Mp_5$	2	0.25
$Mn_6 and Mp_6$	1.5	0.25
$Mn_7, Mp_7, Mn_8, and Mp_8$	1	0.25
$Mn_9 and Mp_9$	0.5	0.25
$Mn_{10} and Mp_{10}$	2	0.25

The obtained result of voltage level shift circuit is shown in Table VIII. When the digital input was 00000001, the output voltage of the voltage source was at its lower level. With moving 1 from first bit to next bits, the output voltage level is shifted to a higher level. When the 1 moves to the most significant bit position, the output

voltage will reach the highest voltage level. The voltage source produces 8 levels of voltage ranging between 0.76 V and 1.36 V. After integrated shift level voltage with current source, Table 3.4 shows the relationship between place of 1 in digital input and the input voltage level and current bias. The plot shows the linear relationship. It means that with moving 1 forward, the voltage level and consequently bias current will increase linearly.

Table 3.4
Voltage Level Shifting with Moving 1 from First Bit to Eighth Bit and Bias Current

Bit Place of '1'	**Input Voltage 'V'**	**Bias Current (μA)**
0000 0001	0.76	12.5
0000 0010	0.86	28.8
0000 0100	0.96	50.0
0000 1000	1.06	74.8
0001 0000	1.14	102.3
0010 0000	1.24	132.0
0100 0000	1.3	163.1
1000 0000	1.36	195.3

3.2.4 Threshold Voltage Source

The $CMOS$ transistors threshold voltages are dependent on temperature. In the proposed threshold voltage supply, which is shown in Figure 3.15, the dependency on the temperature is made maximum. The output voltage of the voltage source feeds the ring oscillator in the $CMOS$-based temperature sensor. The output voltage of the presented voltage source is a coefficient of the threshold voltage (V_t). The output

voltage of the following schematic is $3V_t$. Therefore; the voltage source produces the voltage output with more temperature dependency.

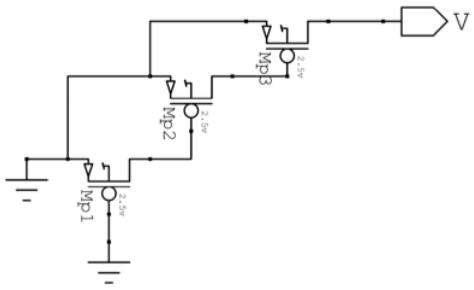

Fig. 3.15. Temperature Sensitive Voltage Source

The simulation results in Figure 3.16 shows that the output voltage of the voltage source falls with increasing the temperature. Within a temperature range between -50 and 100°C, the output voltage linear varies 0.4 V.

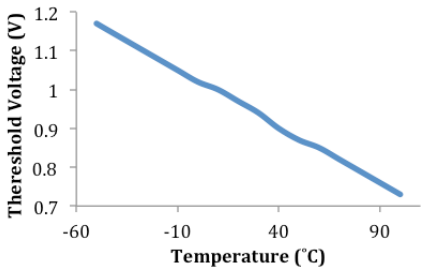

Fig. 3.16. Temperature Dependency of Voltage Source Output

3.2.5 Pulse Generator

The input of the pulse generated, which is shown in Figure 3.17, is fed by the ring oscillator output. Two functionality is defined for the pulse generator, there are decreasing rising time and decreasing the ratio of high-level to low-level voltage of

pulses. The lower rising time creates a higher speed for the system. The average of the voltage level is dependent to the ratio of high-level to low-level. Higher ratio makes the higher average of voltage level and consequently system using more power consumption. Therefore, to achieve the lower power consumption, the ratio of the high-level and low-level of the pulses is kept smaller with presented pulse generator.

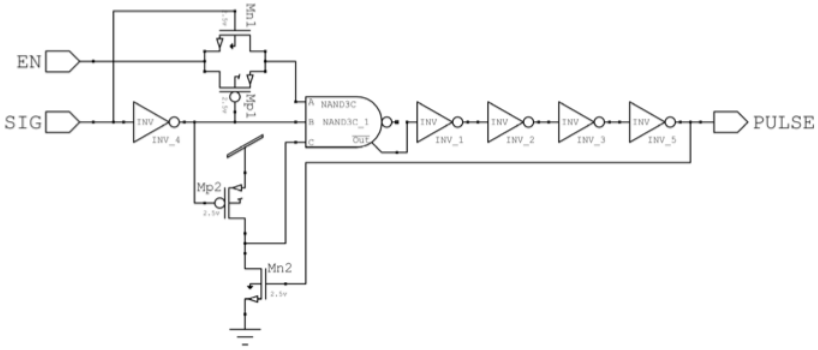

Fig. 3.17. Pulses Generator Schematic

Figure 3.18 shows the obtained pulse wave from the pulse generator. As shown in the figure, the high level voltage of the pulse wave had a suitable width rather than low-level voltage. The pulse wave has completely reached its the maximum and minimum voltage levels. The pulse generator has formed a periodic signal pulse wave.

With comparison between input and output of the pulse generator, the difference is clearly detectable. The solid line in Figure 3.18 shows the pulse wave, and the dash line shows the output of the ring oscillator. The ring oscillator output has not reached its high level voltage. The rising time of signal was higher than the pulse generator output. These results show that the ring oscillator output has been converted to pulse wave.

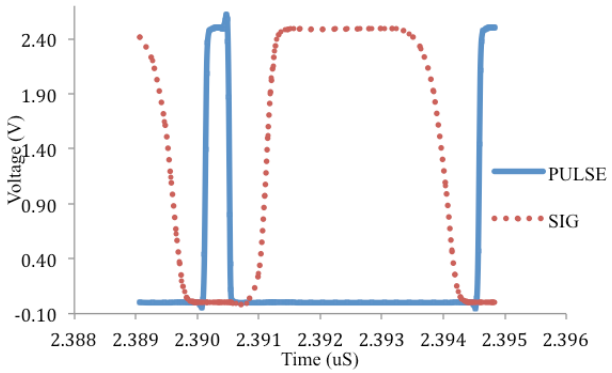

Fig. 3.18. Comparison between Output and Input of the Pulse Generator (Pulse Generator Output at 2 V Input Voltage)

3.2.6 *CMOS*-Based Temperature Sensor

The circuit was simulated for temperature sensor is illustrated in Figure 3.19. Based on the method for sensing the temperature variation, two main circuits are utilized in the *CMOS*-based temperature sensor. The first circuit is ring oscillator, which is sensitive to temperature variation. And other main circuit is threshold voltage generator. This source voltage is sensitive to temperature changes. The simulation shows that increasing in temperature reduces output voltage of the voltage-supply.

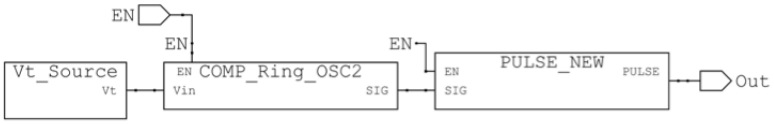

Fig. 3.19. Components of the CMOS-Based Temperature Sensor

The schematic of the temperature sensitive ring oscillator circuit is shown in Figure 3.20, which consists of three stages, bias unit, 5 delay stages, and enable unit. The bias unit provides the control voltages for upper and lower side. As shown in Figure 3.20, the control voltages swing is dependent to threshold voltage. In other

hand, the threshold voltage is dependent to temperature variation. Therefore, the control voltages are varied based on the temperature variation. When the temperature is enhanced, the lower side voltage falls and the upper side voltage increases. And also the presented arrangement of the 5 delay stages ring oscillator is designed dependent on temperature.

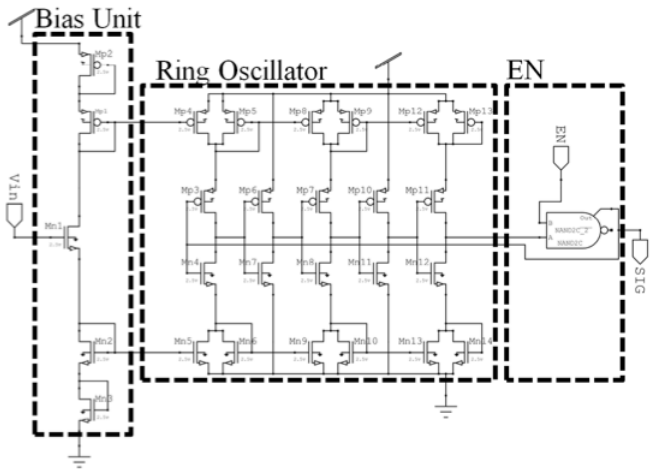

Fig. 3.20. Temperature Sensitive Ring Oscillator

With temperature variation from -50 to 100°C, the pulses wave frequency changes 1.12 GHz to 617 MHz for 250 nm technology. The result (Figure 3.21) shows that increasing temperature reduces output frequency of CMOS-Based temperature sensor. The obtained result shows the linear change with temperature variation.

With same ratio for feature size in 180 nm technology, the temperature sensors generates a range of frequency between 2.6 GHz and 1.8 GHz by temperature increasing from -50 to 100C as shown in Figure 3.22. The reason for difference in range of the frequency is result of the parasitic capacitance in each technology. In 180 nm technology, the smaller channel length for $CMOS$ transistor can be achieved and consequently, the pulses can reach to higher frequency in same temperature with comparison by 250 nm technology. Obviously the power consumption for 180 nm is less

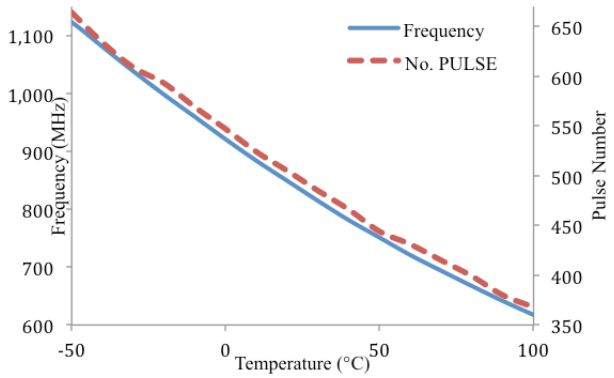

Fig. 3.21. Produced Frequency and Number Pulses by Temperature Sensor When Temperature Variation in Range of -50 to 100°C for 250 nm Technology

than 250 nm for same design. The obtained results show that the consumed power for 180 nm in worst case (temperature is 100°C) is 16 nW.As shown in Table 3.5, the simulation results for presented design show a significantly lower power consumption compared to previously reported sensors, however it should be noted that the presented results are derived from simulation models where as compared results are experimental from fabricated devices. It is expected that the overall experimental power consumption for the design presented in this thesis will go up due to a number of parasitic effects present in a practical devices which were not considered in the ideal simulation model.

3.3 Power Performance

In this work, the system is controlled with SMU, which was designed to perform specific tasks, instead of using a generic controller (MCU) that consumes significant portion of power at digital sub-system [1, 8]. The designed SMU defines the duty cycle of the proposed system, as 12/64. The assigned period for the each sensor is 3 of 64 clocks and the time interval between each clock enabling is 13 clocks cycle.

Table 3.5
Power Consumption Comparison of the Presented Designed Temperature Sensor with Previously Reported Sensors

	This Work	**Souri, et al.** [13]	**Hwang, et al.** [14]	**Lee, et al.** [15]	**Wu, et al.** [16]	**Law, et al.** [17]	**Souri, et al.** [18]	Aita, et al. [19]	Woo, et al. [20]
Sensor Type	Ring Oscillator	BJT	Ring Oscillator	MOSFET	Resistor	MOSFET	BJT	MOSFET	Ring Oscillator
CMOS Technology (nm)	180	160	65	180	180	180	160	700	130
Supply Voltage (V)	1.8	1.5–2	1	N/A	1.2–2	0.9–1.1	1.6–2	3.3	0.8
Temperature Range (°C) (V)	-50 to 100	-55 to 125	0 to 110	-65 to 165	0 to 100	0 to 100	-30 to 125	-70 to 130	5 to100
Accuracy (°C)	±0.1	±0.15	±0.15	±1.9	±0.5	-0.8/+1	±0.2	±0.25	N/A
Power Consumption (μW)	0.016	6.12	500	53.4	36	405	7.4	100	0.03

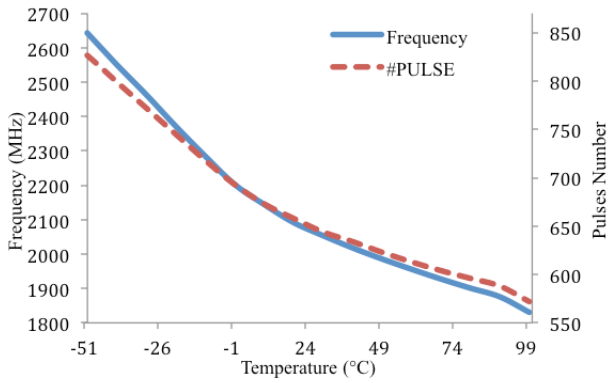

Fig. 3.22. Produced Frequency and Number Pulses by Temperature Sensor When Temperature Variation in Range of -50 to 100°C for 180 nm Technology

Therefore, in the duty cycle, sensors are enabled for data acquisition each 16 clocks consequently. As a result, one sensor-driver is at 'on-state' for 3 of 16 clocks cycle and other sensor-drivers are inactivated. This techniques result in significant reduction in power consumption.

The core of the sensor driver is ring oscillator, which drives the sensor and translates the sensor analyte concentration to frequency. After enabling a sensor, the oscillator start oscillation but the output is unstable as shown in Figure 3.23. To pass the transient time, the oscillator need time to reach a steady state and generate a periodic signal with stable frequency. As shown in Figure 3.23, the transient time for different input voltage of ring oscillator is variable. To make confidence margin, two first clock cycles are allocated to achieve oscillator stability. Thus, three clocks cycle are considered in this work.

The root mean square (RMS) value of the voltage (V_{rms}) and current (I_{rms}) can determine the average power consumption (P_{avg}) of a periodic signal which is given by

$$P_{avg} = V_{rms} \times I_{rms} \tag{3.1}$$

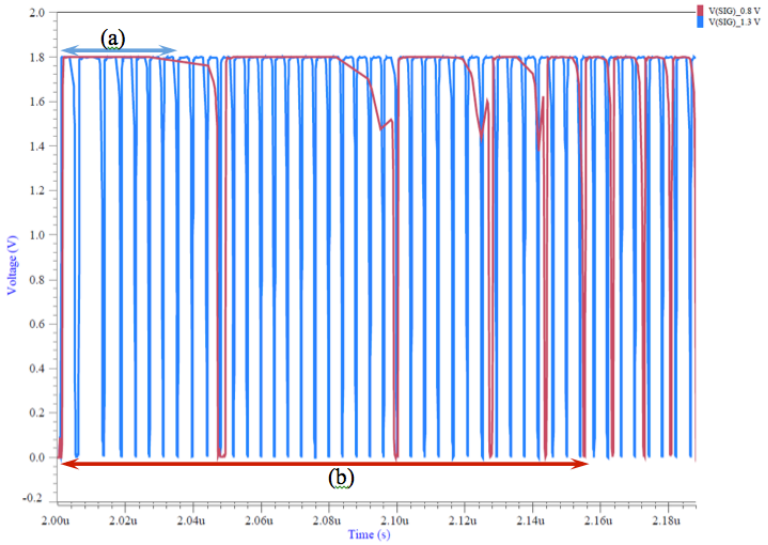

Fig. 3.23. a) The Transient Period for 1.3 V Tuning Voltage and b) The Transient Period for 0.8 V Tuning Voltage

Assume the RMS value of $u(t)$, U_{rms}, can be calculated by

$$U_{rms} = \sqrt{\frac{1}{T}\int_0^T u(t)^2\,dt} \tag{3.2}$$

Where $u(t)$ is periodic function with time period T. The power-supply voltage of the sensor-driver is a pulse function which its peak voltage is V_{DD}. When the power pulse is in the peak, the bias current for one delay stage of the ring oscillator can be calculated by [36]

$$I_{BIAS} = 2N f_{osc} V_{osc} C_G \tag{3.3}$$

Where V_{osc} and f_{osc} are oscillation voltage and frequency and also I_{BIAS} is bias current of the delay element in ring oscillator with parasitic delay capacitance (C_G) when the number of the delay elements is N. In the rest of the cycle, when the power supply is zero, the current should be zero. Therefore, the current is pulse function which its peak is determined by 3.3.

A completed period of the system is 64 clocks cycle that consists of the 12 clocks cycle in high level and the rest of the period in zero. To calculate the V_{rms}, which

waveform is shown in Figure 3.24, 16 clocks cycle are investigated instead of 64 clocks cycle because the complete period of the system can be divide into 4 regions with same pattern. If the sensor is on 'a' of 16 clocks cycle, the V_{rms} is given by

$$V_{rms} = \sqrt{\frac{1}{16t_c}\int_0^{at_c} V_{DD}^2\, dt} = V_{DD}\sqrt{\frac{at_c}{16t_c}} \tag{3.4}$$

Where thet_c is period of a clock cycle. And the duty cycle of the power-supply can be determined by

$$D = \frac{a}{16} \quad and \quad a = integer \tag{3.5}$$

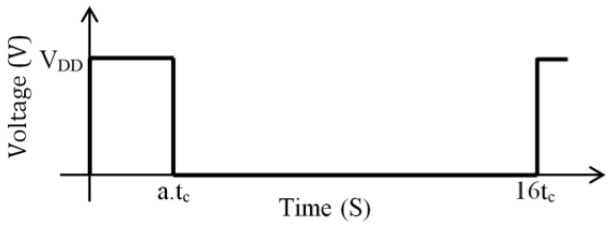

Fig. 3.24. Power-Supply Voltage Waveform for Sensor-Driver

In same way, the RMS value for Current is calculated by

$$I_{BIAS} = \sqrt{\frac{1}{16t_c}\int_0^{at_c} I_{BIAS}^2\, dt} = I_{BIAS}\sqrt{\frac{at_c}{16t_c}} \tag{3.6}$$

Therefore, the average power consumption is determined by

$$P_{avg} = I_{BIAS}V_{DD}\frac{a}{16} \tag{3.7}$$

Two factors, duty cycle and current bias level, is variable in determining the power consumption. The duty cycle id calculated by the number of clock cycle which the sensor driver is activated by SMU. Obviously, with increasing 'a' in the 3.4, the average of the power is increasing. Therefore, to achieve minimum power consumption, the 'a' should be in minimum but it cannot be less than 3. Also the current is dependent to output frequency which is enhanced by input voltage of the ring oscillator.

According to 3.3, the current is increasing with frequency enhancement and consequently, the power consumption reach to higher value for higher frequency. Based on the 3.4, with increasing 1 clock cycle, the power consumption in ring oscillator is enhanced by 6%.

Although reducing the duty cycle of the sensor driver can make condition to reduce power consumption, increasing the 'on-state' of sensor-driver can improve sensitivity of the system. During the 'on-state' clock cycle, the sensors are monitored based on the number of the pulses, which is generated by sensor driver. The 'on-state' period is divided into two periods, (i) transient period and (ii) monitoring period. Based on the defined method, two clock cycles are allocated that sensor-deliver reaches stability in transient state and one clock cycle is for monitoring period. Therefore, the senor-driver is activated for three clock cycles. For three 'on-state' clock cycles, assuming the minimum frequency change between f_1 and f_2 is δf, the system can detect one more pulse. Therefor if the sensor-driver generates f_1 in state one and the system counts the 'n' pulses, the system counts $'n+1'$ pulses for f_2 at state two. If the monitoring period is doubled (four clock cycles 'on-state'), the number of counted pulses will become '$2n$' for state one and '$2n+2$' for state two. Therefore, a state is created between state one and state two. It means that the system can detect more state and sequentially increasing sensitivity of the system. If the monitoring period is increased by factor three (five clock cycles 'on-state'), the system can read two more states between state one and state two. This increases the number of monitoring period enhancing probability of counting more number of pulses between two states of the sensor. It results in the increase in the number of the monitoring state of the sensor and consequently increasing sensitivity of the system.

Unlike the other proposed BSN system-on-chip, this system does not include the analog to digital convertor (ADC) [1, 6–10]. The substitute method in analog conversion to digital is based on the number of the pulses so other method to reduce

the power in this work is transmitting pulses to digital sub-system with lower V_{rms}. The average power can be calculated by

$$P_{avg} = \frac{V_{rms}^2}{R_{load}} \tag{3.8}$$

The R_{load} is provided by digital sub-system when the analog part is enabled. To this purpose, the duty cycle of the pulses should be reduced. The period of the pulse generator output is related to frequency, and consequently, the denominator of the duty cycle is changed with frequency variation. To achieve minimum duty cycle in each frequency, the output frequency is formed by zero voltage level variation and the high level width is fixed for all frequencies with utilized pulse generator, as shown in Figure 3.25. When the driver-sensor is enabled, the V_{rms} for output pulse generator calculated by

$$V_{rms} = \sqrt{f_{osc} \int_0^{t_w} V_{DD}^2 \, dt} = V_{DD}\sqrt{f_{osc} t_w} \tag{3.9}$$

Where t_w is width of the high level voltage. The V_{rms} is related to frequency directly so the average power is dependent to frequency of the sensor-driver output. The V_{rms} in entire period is calculated by

$$V_{rms} = \sqrt{\frac{1}{16t_c} \int_0^{3t_c} V_{DD}\sqrt{f_{osc} t_w} \, dt} = V_{DD}\sqrt{\frac{3 f_{osc} t_w}{16 t_c}} \tag{3.10}$$

With utilized methods to reduce power consumption, the simulation shows the 100 nW for the presented system in worst case. Table 3.6 shows the comparison between presented system-on-chip and other reported work. The presented system does not include memory unit, thus, the captured sensor data has to be instantaneously transmitted to a remote station, e.g. end user interface. This may result in a loss of sensor data in an event of loss of communication link with the remote station. In addition, the presented design does not include transmitter and receiver modules, and thus necessitates the use of separate modules for the transfer of the data. According the Table 3.6, the major proportion of the power is consumed by transmission unit.

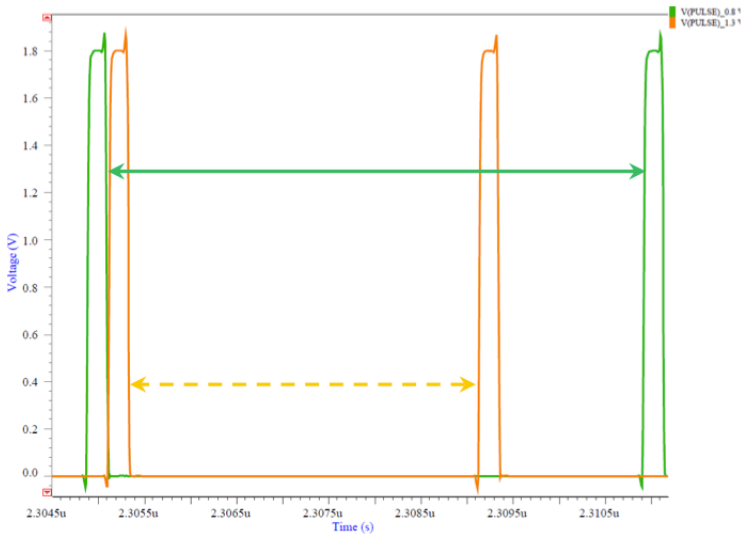

Fig. 3.25. Zero Voltage Level Variation in Pulse Generator

To reduce the power consumption, Zhang et al. utilized the method, which applies the transmission unit for a portion of time. The presented system can use Zhangs method because the system cannot store the captured data in the memory and data should be transmitted immediately. The implementation of transmission unit can increase the power consumption of the system.

3.4 Applications

Advances in wireless sensors and miniature electronics have garnered much attention in the rapidly advancing healthcare industry [43–45]. The main goal of this project is design ASIC chip with that can integrate multiple sensors for continuous monitoring of vital parameters in the human body or surrounding environment. Elderly people, children, pregnant women, and those with disabilities can all make use of lifesaving assistance from the system proposed by the research group. In addition, for Smart house application, the designed chip can be integrated with multiple sensors will provide more information from the surrounding environment. The goal of

Table 3.6
Power Consumption Comparison of the Presented Design with Previously Reported Systems

	This Work	**Zhang et al.** [1]	**Kim et al.** [6]	**Verma et al.** [7]	**Chen et al.** [8]	**Rai et al.** [9]	**Yan et al.** [10]
Sensors	Res, Cap-Based, and Temp	EEG, EMG ECG	ECG	ECG	Temp Pressure	Neural, ECG EMG, EEG	ECG TIV
Supply Voltage	1.8 V	30 mV, -10 dBm	1.2 V	1 V	0.4 V/0.5 V	1 V	1.2 V
Energy Harvesting	N/A	Thermal, RF	N/A	N/A	Solar	N/A	N/A
Power Management	N/A	yes	N/A	N/A	yes	yes	yes
Supply regulator	N/A	yes	N/A	N/A	yes	yes	yes
GPP MCU	N/A	yes	N/A	N/A	yes	yes	yes
ADC	yes	yes	yes	yes	yes	yes	yes
Memory	N/A	yes	yes	N/A	yes	N/A	yes
$T_x P_{DC}(100\% on)$	N/A	160 μW	N/A	N/A	N/A	400 μW	2.8 mW
Digital Power	60 nW	2.1μW	12μW	2.1μW	2.1μW	N/A	500 μW
Total Chip Power	100 nW	19 μW	31.1 μW	77.1 μW	7.7 μW	500 μW	2.4 mW
Technology	180 nm	130 nm	180 nm	180 nm	180 nm	130 nm	180 nm

the proposed project is to develop a low power miniaturized device equipped with multiple sensors for monitoring vital parameters, and delivering the information thus gathered to a gateway device for healthcare, smart house, environment monitoring. In the following some applications for the presented chip is proposed.

The presented system-on-chip can be integrated with *RF* module to communicate with end user interfaces as shown in Figure 3.26, such as cellphones. By integrating biosensors, the system-on-chip can detect and monitor vital parameters of the human body and transmits the detected data to an end user interface (e.g. smartphone). The following combination of biosensors can be utilized for monitoring human body, and can be monitored with a smartphone [43–49]:

- Heart rate, Blood Pressur, *ECG* [43]
- Heart rate, oxygen saturation, location [45]
- *ECG*, acceleration, breathing [47]
- *ECG*, Heart Rate, *EEG*, Temperature [48]

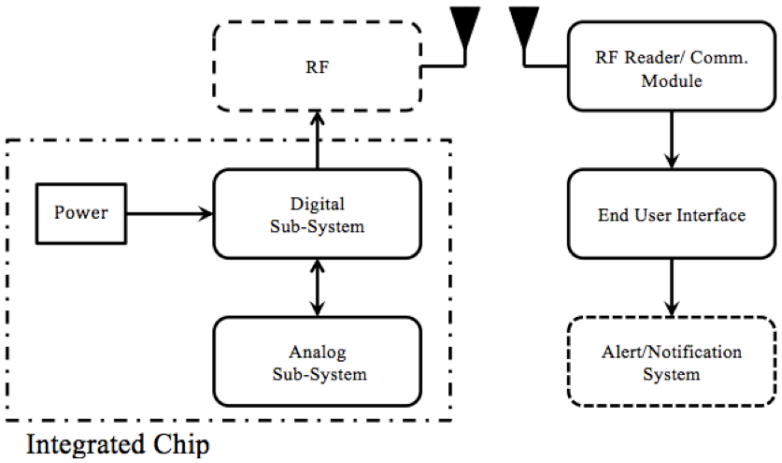

Fig. 3.26. Block Diagram of RF Integrated with System-on-Chip

The accelerometer can be integrated to developed system-on-chip to detect fall detection and (or) body gesture [50]. Fall detection is very important for the elderly,

children or people who have Parkinsons. And also accelerometer can be utilized to predict the subject‘s behavioral information such as walking, standing or climbing the stairs [51].

In another setup, data provided by body sensors in accordance with the environmental information provided by a gas sensor, a temperature sensor and a humidity sensor helps the elderly not to forget their daily activities by reminding them of unfinished jobs [52]. Using intelligent algorithms like HMM and a Genetic algorithm, data provided by wearable sensors and embedded sensors can predict and recognize the users activity [53].

Diabetes threatens the lives of millions of people in the US and around the world [54, 55]. A non-invasive method for accurately detecting elevated blood glucose levels could provide lifesaving information for a person suffering from a diabetic attack. Blood glucose level variation can manifest itself in multitudinous ways in the Human body. Studies have shown that it causes a measurable change in temperatures in the extremities of the foot [56–58]. Glucose alters the ability of hydrogen to bond this leads to a weakening of the intermolecular forces within water, and is evidenced by an earlobe that becomes less dense temporarily [59]. This in turn leads to a variation in the frequency a sound makes while resonating in the earlobe [59] Electrical impedance of the earlobe is also affected by this change [59]. A tremendous amount of research has shown a correlation between Volatile Organic Compounds in exhaled breath, and the level of glucose in the blood [60–67]. The proposed chip can provide the interface for multiple sensors to measure the different symptoms of the high blood glucose sugar in the human body.

Multiple parameters on human body can be monitored via a multi sensor chip. If the outputs of the sensors are above threshold, an alarm signal can alert the family member or a health care team. The data can also be sent via a getaway device to the

hospital and be recorded on the patient medical history. The following information can be provided for a health care center via such systems: Blood pressure, heart rate, oxygen saturation, body temperature, *ECG*, weight, breathing rate, and body activity can be monitored continuously and a low power, miniaturized interface that can provide accurate readings can provide lifesaving information for health care team.

Researchers are looking for the noninvasive methods to do a Complete Blood Count, Noninvasive monitoring of body dehydration, Measuring electrolyte in blood (Sodium, Potassium, Chloride, Bicarbonate) and etc [44, 68]. It may not be possible to have a good estimate with a single sensor. The proposed project provides the interface for a multiple sensors to collect the data for an accurate estimate of the mentioned applications.

To monitor the surrounding parameters of the houses, the sensor can be utilized such as temperature sensor, light sensor, humidity sensor, gas sensor, and etc. The environment parameters can be adjusted after sensors detect the quantity of parameters. With controlling the surrounding parameters, the life quality in house can be improved to better state. With analyzing house environment parameters, the house power consumption can be optimized. Therefore, household power consumption can be regulated intelligently according to detected parameters.

4. CONCLUSIONS AND FUTURE RECOMMENDATIONS

4.1 Conclusions

The goal of this research was the realization of low-power $ASIC$ design with integrated multiple sensor system. Specifically the objectives of this research were to drive the integrated sensor system, manage and optimize power consumption, digitize sensor analog output, and send output data to a transmission module. Design and simulation results on application specific integrated circuits ($ASIC$s) consisting of analog and digital sub-systems forming a system-on-chip have been presented and discussed. Complementary metal-oxide-semiconductor ($CMOS$) technology in integrated circuit (IC) was utilized in the presented system design. A novel method of power management and sequential monitoring of several sensors has been presented and discussed.

Both analog and digital sub-systems utilized several components to achieve the system-on-chip functions. The major components of the digital sub-system consisted of SMU, counter module, and shift register. The SMU activates the sensors only 3/16th fraction (18%) of the time, thereby significantly reducing the power consumption. The SMU then processes the collected signal to counter modules. The data is then packaged in a digital data frame with the help of the shift register module.

In analog sub-system, the sensor-driver includes ring oscillator to convert input voltage to frequency. The ring oscillators that drive capacitance and resistance-based sensors use an arrangement of delay elements with two levels of control voltages. The ring oscillator consists of a bias unit which provides these two levels of control volt-

ages with maximize voltage swing. The control voltage level swings give the oscillator wider tuning range and lower temperature induced variations. The output of the ring oscillator is reformed with pulse generator. And then, by counting the number of pulses of a sensor-driver in one clock cycle, a sensor input parameter is converted to digital. The digital sub-system constructs a 16-bit frame consisting of 8-bit sensor data, start and stop bits, and a parity bit. The output result of the system-on-chip is a serial data that represents the last state of each sensor sequentially.

$CMOS$-based temperature sensor has been presented and discussed. The temperature sensor was designed using changes in the frequency within the ring oscillator with temperature variation. The presented ring oscillator design has wider range of variations with temperature changes. The ring oscillator has been designed with symmetrical load for better temperature sensing. The ring oscillator is controlled by a power supply that is designed to be sensitive with sensing the temperature.

The presented design integrates multiple sensors while consumes low-power and is applicable in a wide range of continuous monitoring requiring small form factor and longer battery life, specifically, in monitoring vital parameters of body or e-health. Low-power consumption is also a key for application with energy harvesting and passive systems. The presented system can be integrated with a transmitter module to send the sensor information to an end user interface, such as cellphone.

4.2 Future Recommendations

The presented system has been utilized to drive the sensors and prepare the serial data that consists of the last state of sensors. The presented SMU manages the system power usage whit activating and inactivating the sensors sequentially for low power application. The proposed system can be modified to use clock-switching

scheme to better optimize the power consumption. This technique is reserved for future consideration. In first step, the system needs the complement module for data transmission. The end stage of the presented system-on-chip produces the data frame in serial form. The generated data can be transmitted with RF module or other transmission technique such as Bluetooth. In future, the RF module can be implemented to incorporate with the system for sending and receiving data. According the literature survey, the significant amount of power is consumed in transmission unit. To achieve better power performance, the duty cycle can be defined for transmitting the data. Therefore, the system needs to be completed with memory to store the captured data during the period that the transmission module is off.

Other recommendation to improve system is related to analog sub-system. The analog sub-system performance depends on the ring oscillator operation. In the future, the architecture of the ring oscillator has to be improved to achieve linear functionality in a wider operation voltage range. And also, the ring oscillator should be designed with better temperature and power-supply voltage insensitivity. The single-end ring oscillator can be replaced by dual or quad output ring oscillator for achieving better stability against temperature and power-supply voltage variation.

The presented system-on-chip has been designed based on optimum power consumption. In future, the unit may features energy harvesting and storing capability. This improvement may convert the active presented system to passive system. Accordingly, it will be utilized for low power chip applications. The energy may be harvested in various sources such as body heat source, vibration source, and electromagnetic wave source. The harvested energy may be stored in the capacitor and the output voltage of the capacitor is adjusted with regulator. The components in the system-on-chip will be fed with regulated voltage.

The presented digital sub-system works in one direction. The digital sub-system prepares the data to transmit. In future, the digital sub-system can be modified to bidirectional data path, send and receive. This improvement can create the ability to control the process of the system from external sources. In digital sub-system, the structure of logic gate can be modified to achieve minimum power consumption. Furthermore, instead of using standard logic cell, the presented logic path may be replaced by logic configuration that feature low power consumption, to further enhances the power reduction.

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