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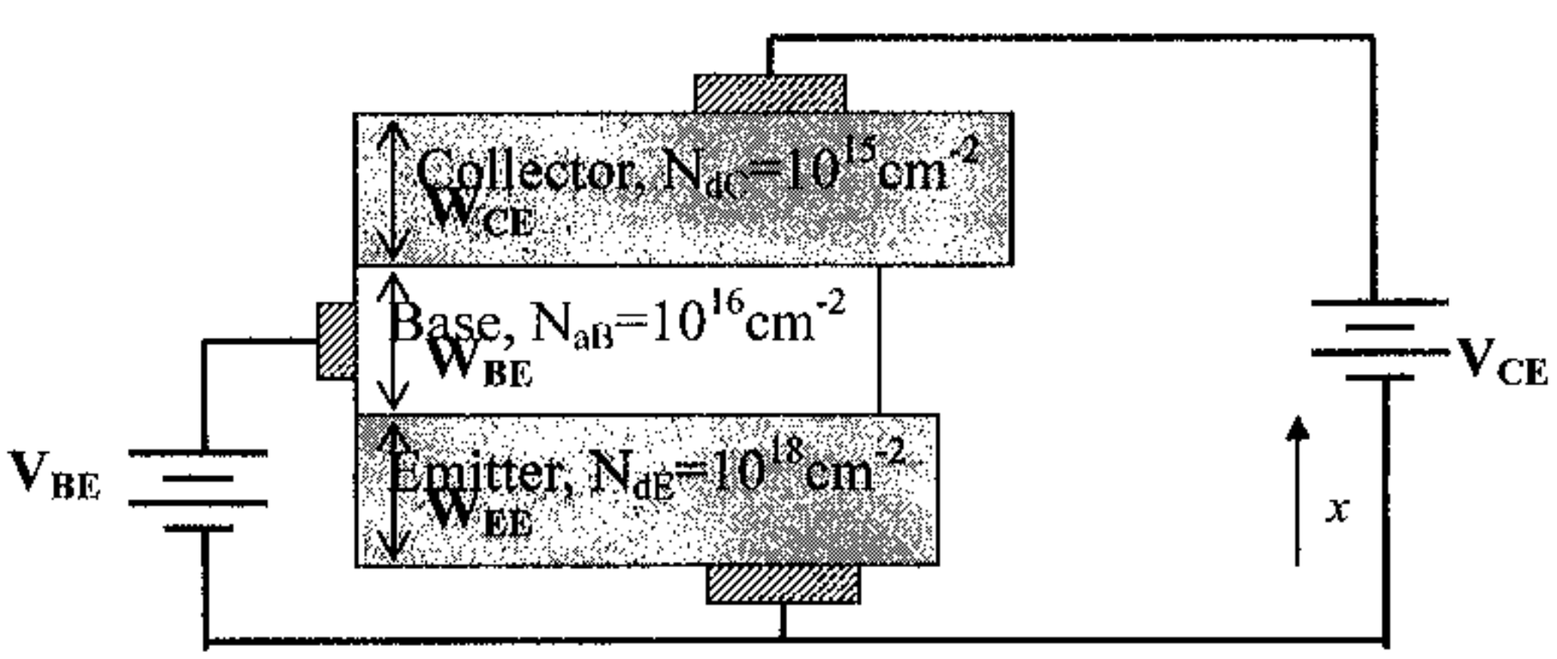
九十二學年度 電子工程研判所 系（所） 組碩士班研究生招生考試

科目 固態電子元件 科號 2605 共 2 頁第 1 頁 *請在試卷【答案卷】內作答

1. For a MOS capacitor fabricated on p-type silicon substrate and with a SiO_2 thickness of d, draw the schematic diagrams of the following items under the condition of strong inversion: (1) energy band diagram of the three materials (metal, SiO_2, and Si) and mark the conduction band edge E_C, valence band edge E_V, intrinsic Fermi level E_i, and Fermi level E_F of the semiconductor, (2) schematic diagram of the charge distribution, (3) schematic diagram of the electric field distribution, (4) schematic diagram of the electrostatic potential distribution. Use x as the horizontal axis for all the four diagrams. (20%)

2. The threshold voltage of a metal-oxide-semiconductor field effect transistor (MOSFET) is usually expressed as the sum of four terms. (1) Write down the expression of the threshold voltage of a MOSFET. Explain the meaning of each term. (2) For typical n-channel and p-channel MOSFETs, what is the polarity of each term (i.e., whether they are positive or negative)? (15%)

3. A npn BJT with doping level label in the Figure shown below . Let $n_i=1x10^{10}cm^{-3}$, $V_T\ln 10=60mV$, $W_E=0.1\mu m$, $W_B=0.2\mu m$, $W_C=0.5\mu m$. Assume ohmic contact at the metal/semiconductor interface. (a) Plot the energy-band diagram, minority carrier densities, *n(x)* and *p(x)* and electric field, *E(x)*, at thermal equilibrium when $V_{BE}=V_{CE}=0$. Label the position of the fermi level and values of *n(x)*, *p(x)* at the boundaries. (10%) (b) Plot the energy-band diagram, minority carrier densities, *n(x)* and *p(x)* and electric field *E(x)* at thermal equilibrium when $V_{BE}=0.6V$, $V_{CE}=1.5V$. Label the position of the fermi level and values of *n(x)*, *p(x)*at the boundaries. (10%) (c) Discuss respectively how the current gain, β, of this device changes when N_{dE} increases/ W_E increases? (5%)



4. **JFET**

(a) Plot the cross-section of a JFET device that can be realized in CMOS single-well technology on p-type substrate. (5%)

(b) How will the substrate bias affect the pinch-off voltage, V_P? (5%)

5. Plot (5%) and explain briefly (10%) the temperature dependence of carrier mobility in semiconductor materials.

6. What is a (a) one-sided junction (5%); (b) linear graded junction (5%): and (c) hyper-abrupt junction (5%)?