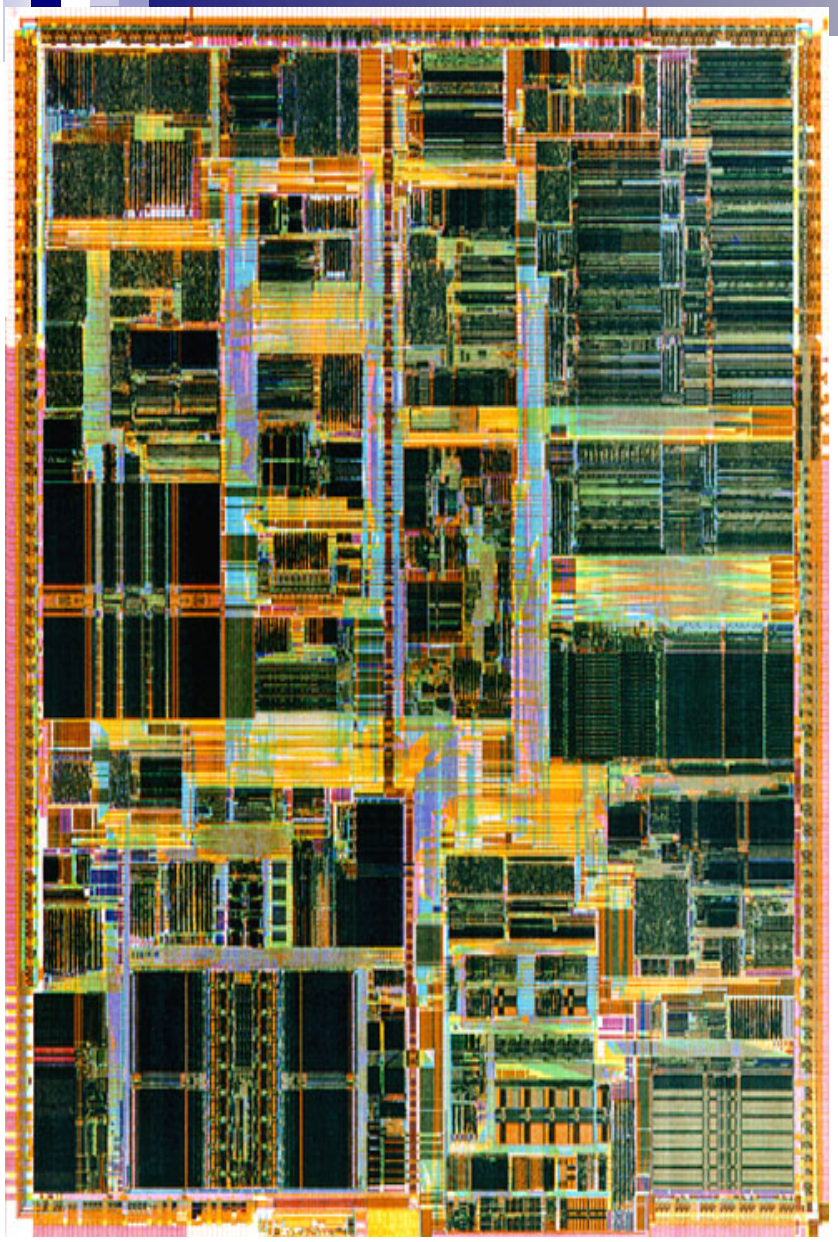


半导体集成电路

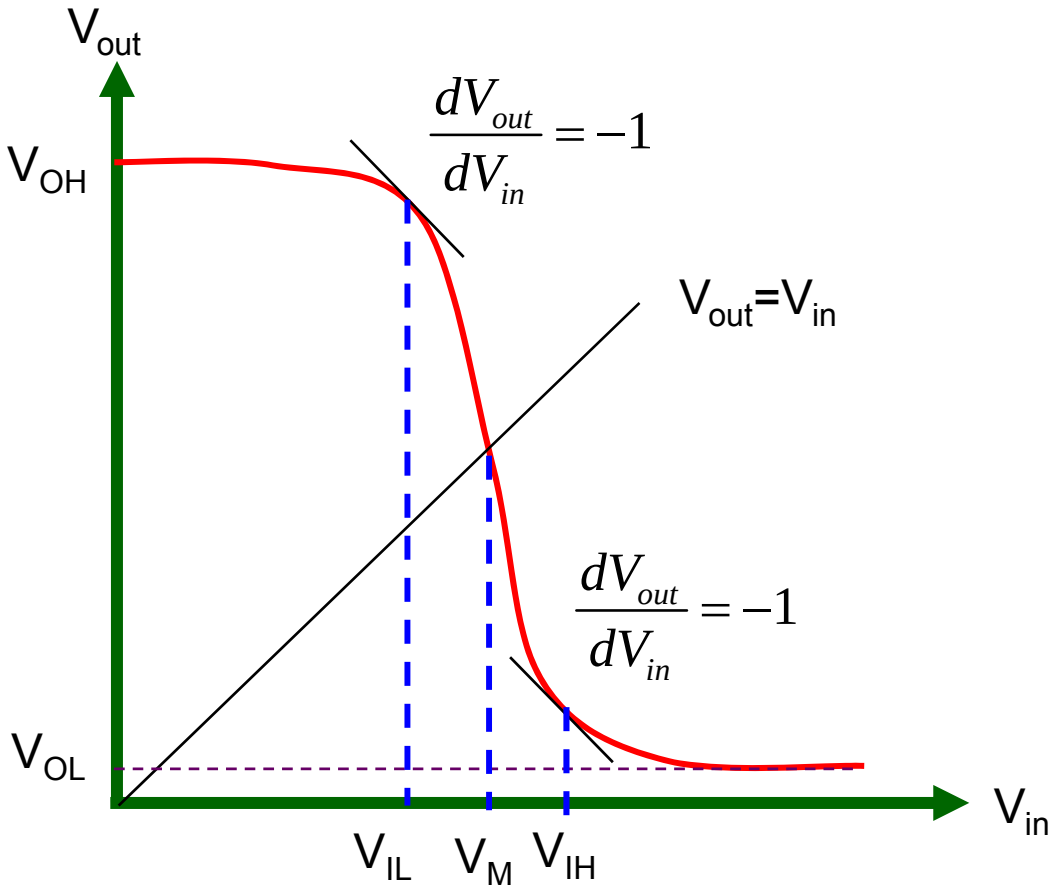
学校：西安理工大学
院系：自动化学院电子工程系
专业：电子、微电
时间：秋季学期

上节课主要内容

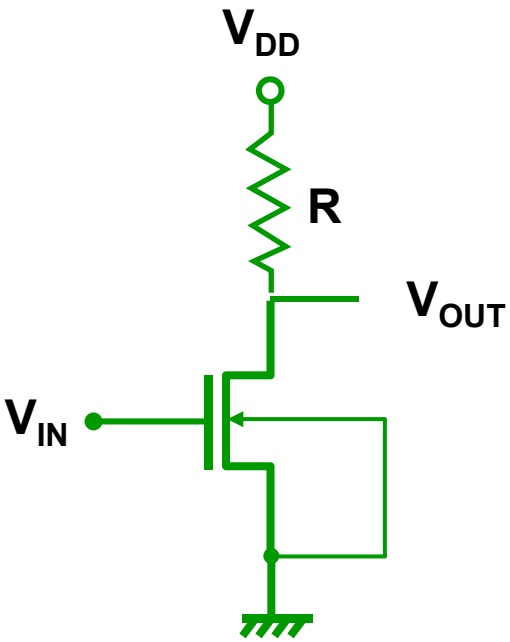
MOS反相器的静态特性

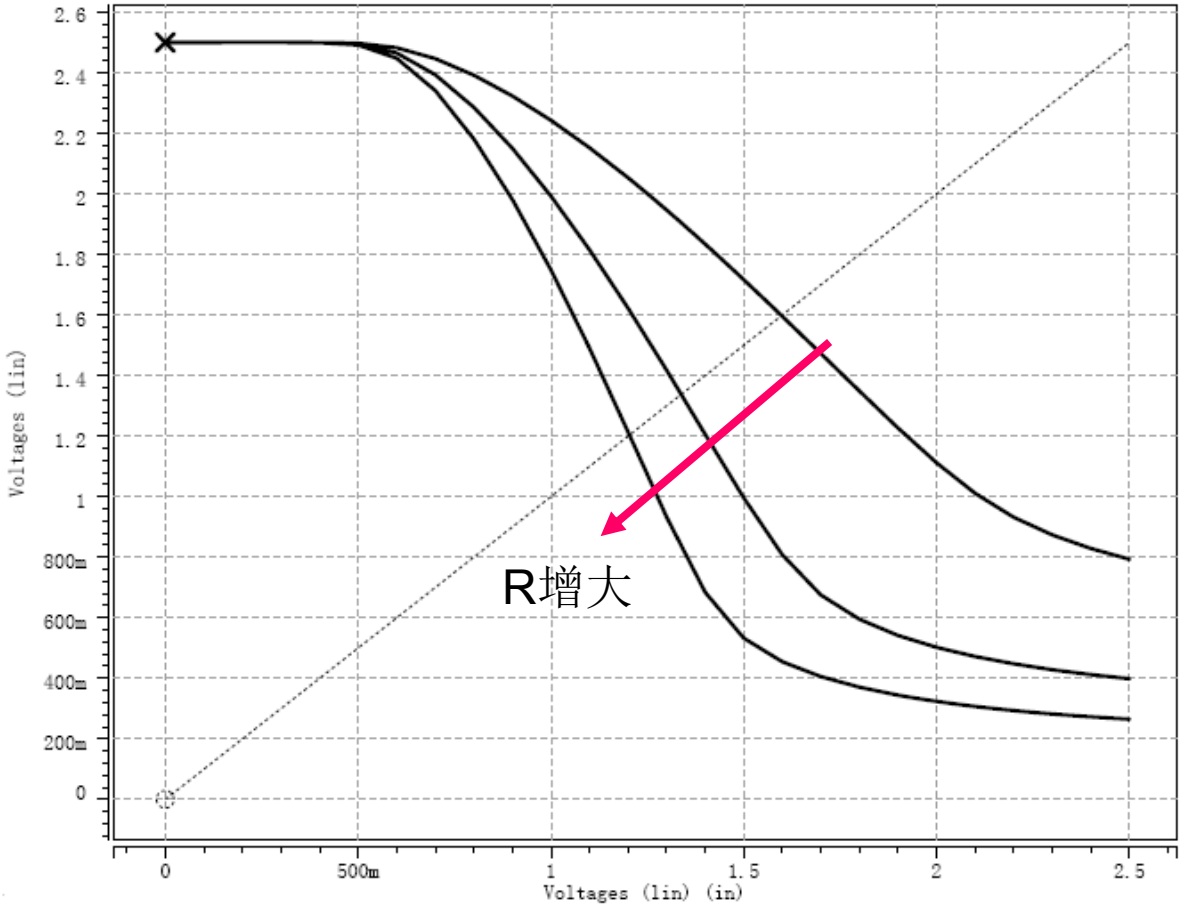
- MOS反相器的构成
- MOS反相器的逻辑阈值
- MOS反相器的噪声容限

反相器的输入输出传输特性

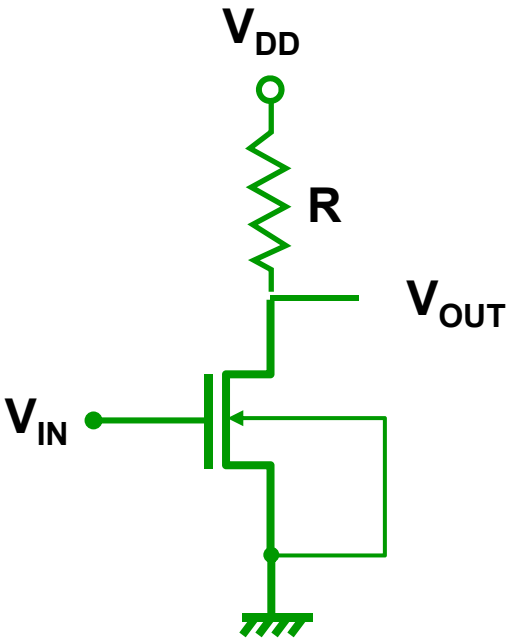


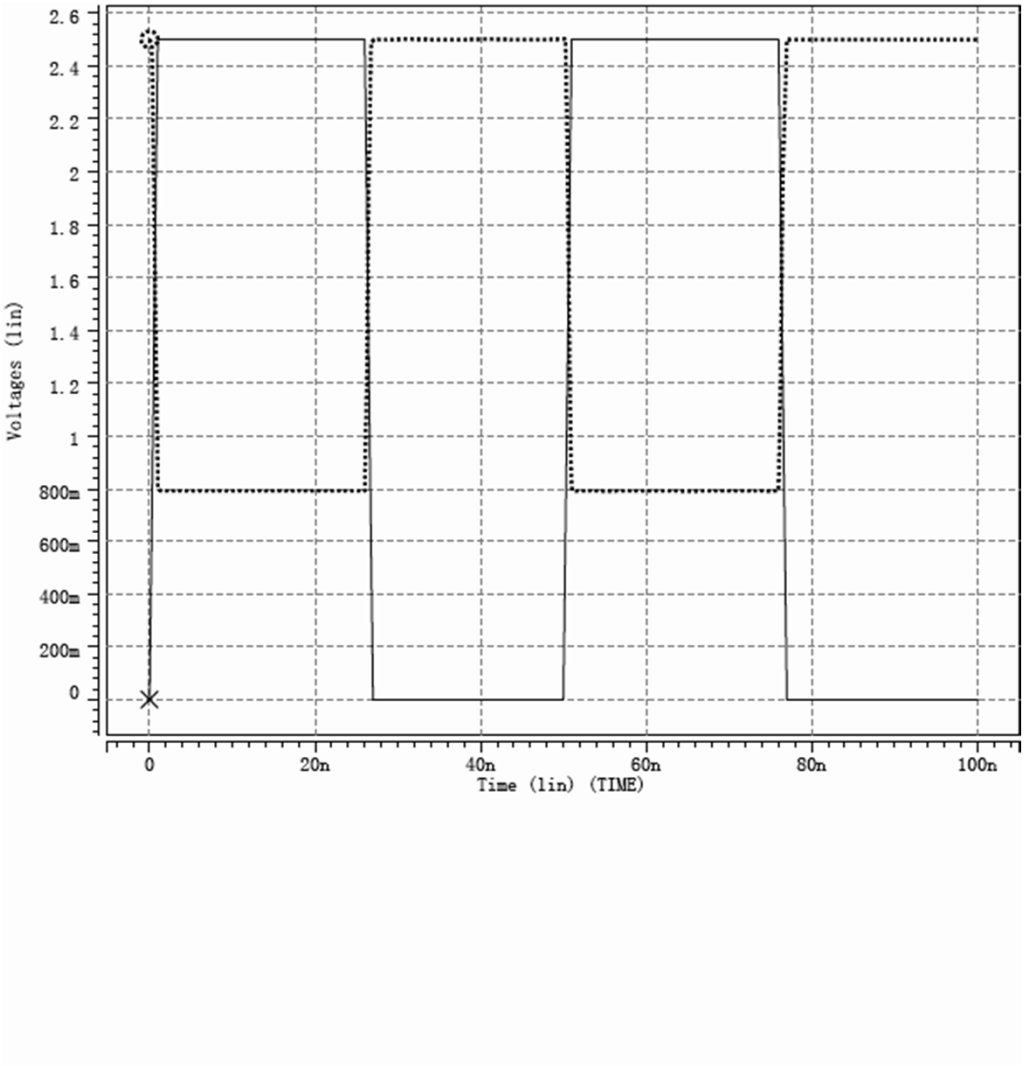
❖ 电阻负载型反相器


V_{DD}
R
V_{OUT}
V_{IN}

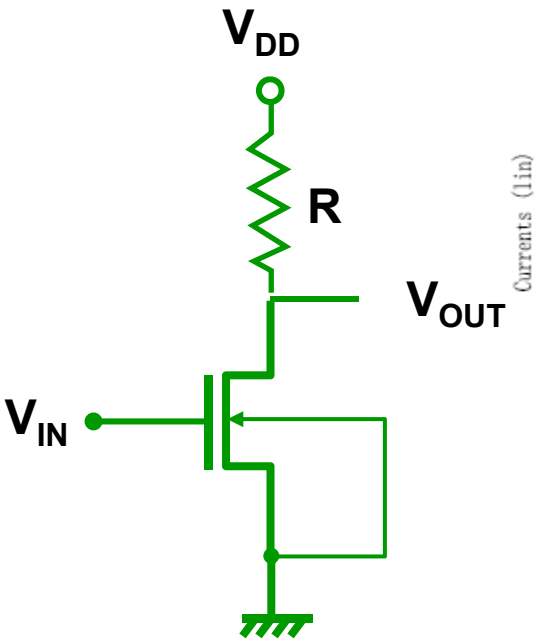

2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
Voltages (lin)
0
500m
1
1.5
2
2.5
Voltages (lin) (in)
R增大

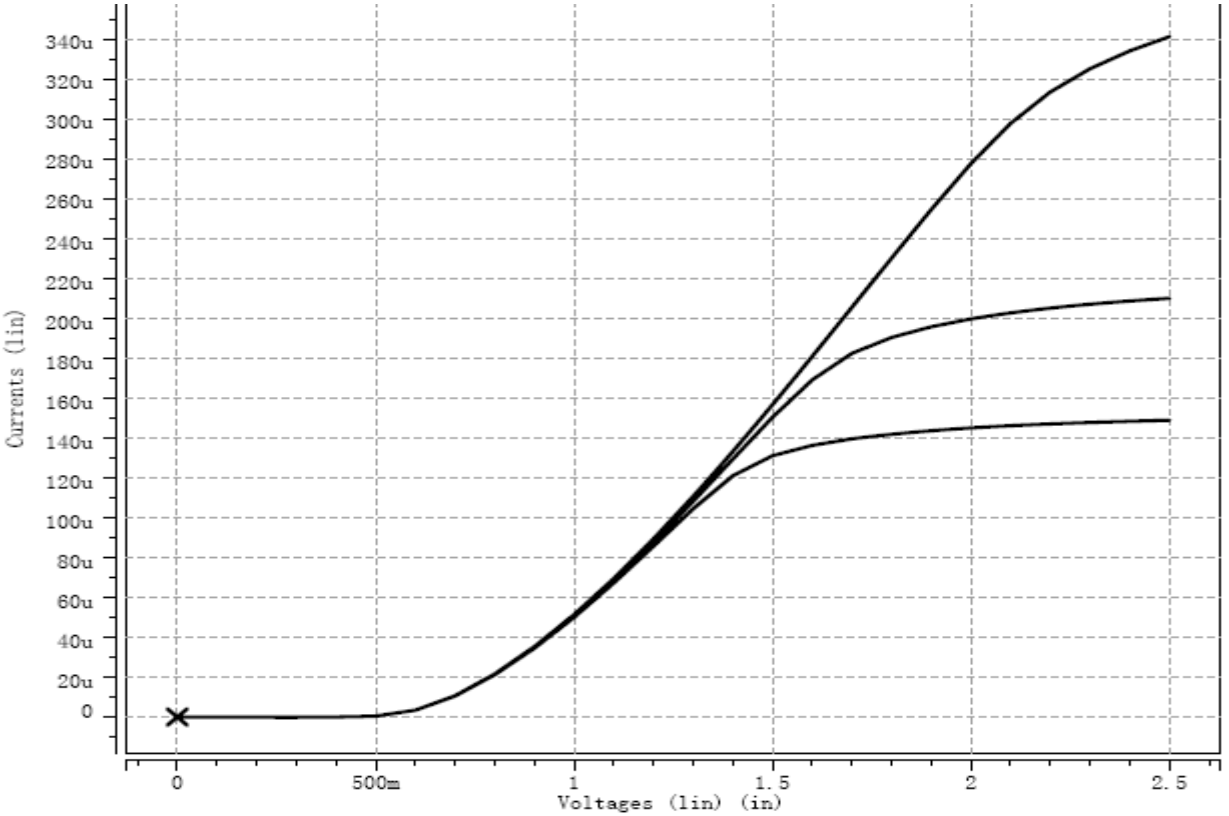
❖ 电阻负载型反相器


V_{DD}
R
V_{OUT}
V_{IN}

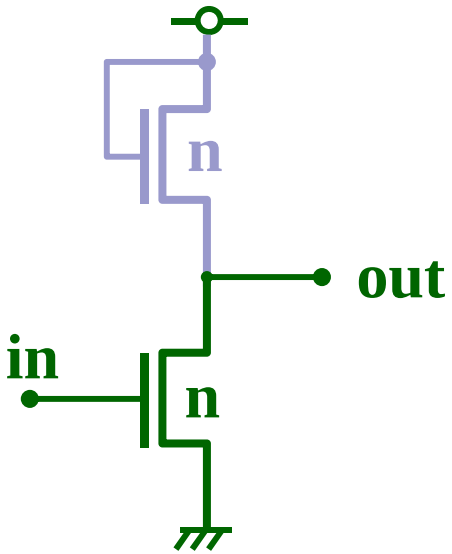

2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
Voltages (lin)
0
20n
40n
60n
80n
100n
Time (lin) (TIME)

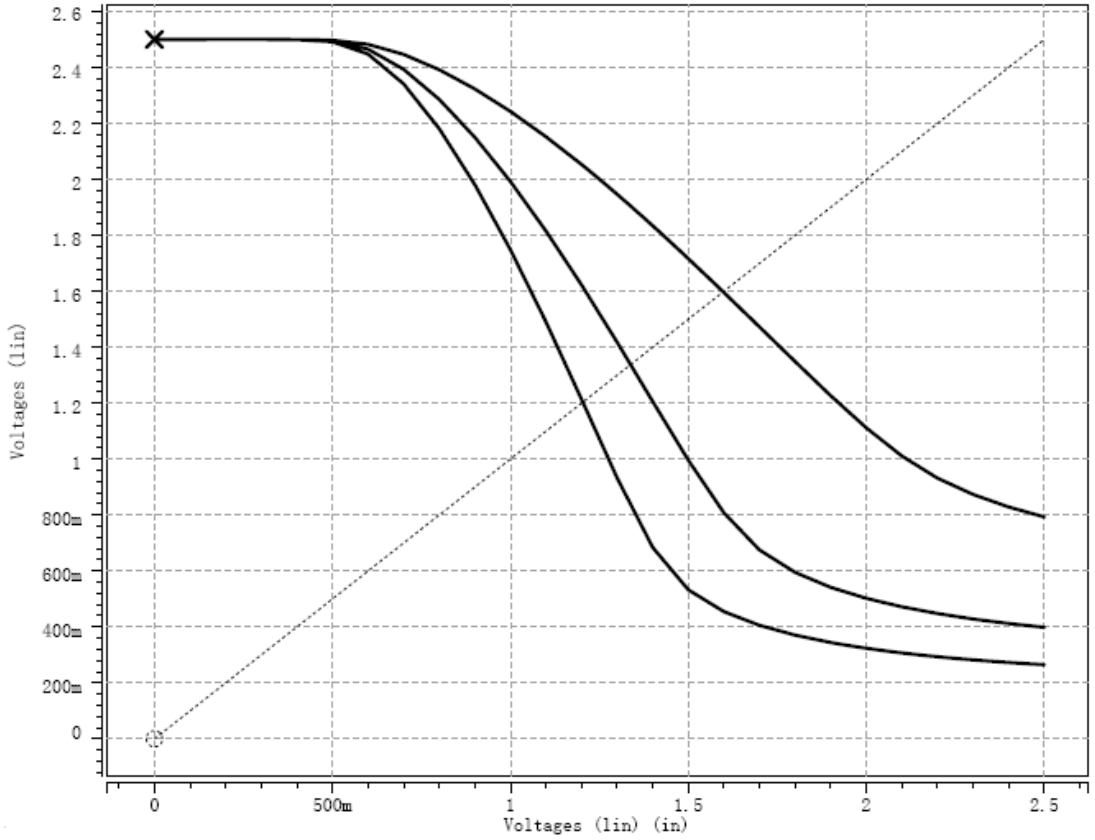
❖ 电阻负载型反相器


V_{DD}
R
V_{OUT}
V_{IN}

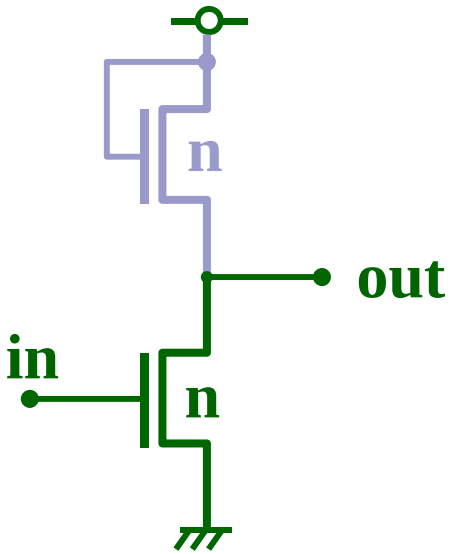

340u
320u
300u
280u
260u
240u
220u
200u
180u
160u
140u
120u
100u
80u
60u
40u
20u
0
Currents (lin)
0
500m
1
1.5
2
2.5
Voltages (lin) (in)

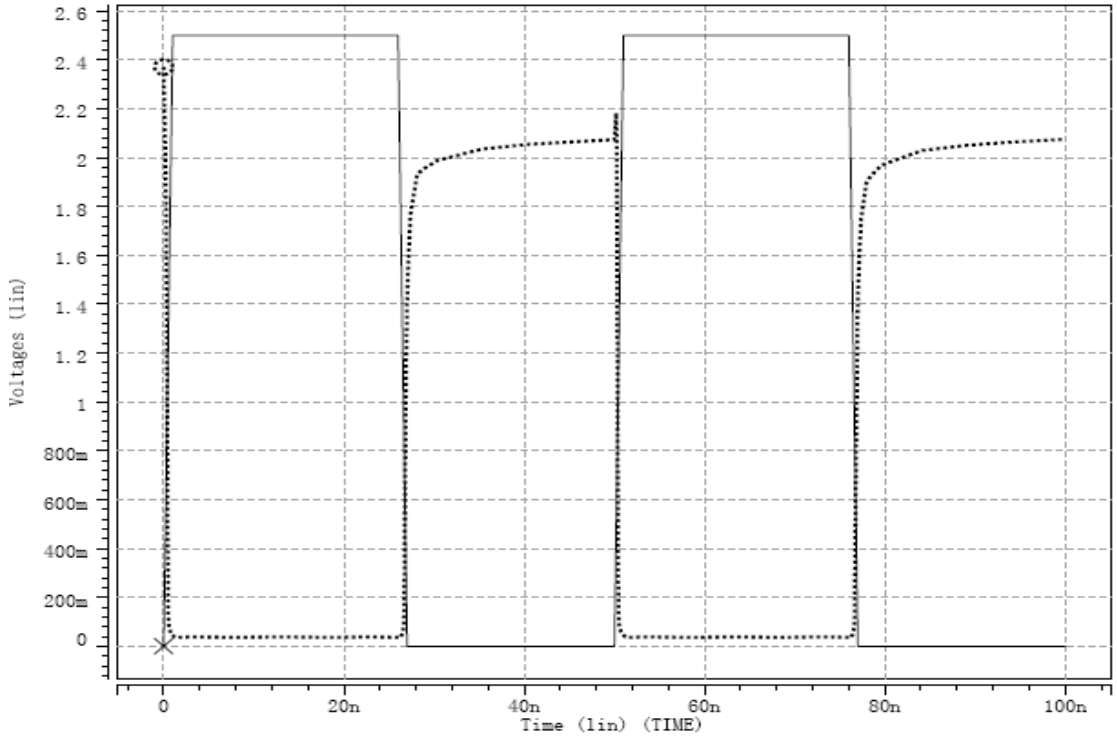
❖ nMOS E/E 反相器


n
out
in
n

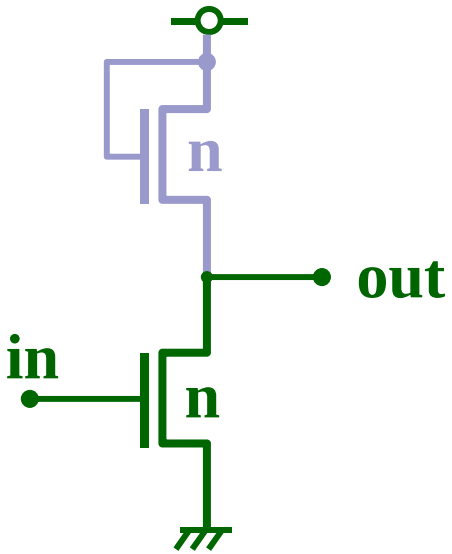

Voltages (lin)
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
500m
1
1.5
2
2.5
Voltages (lin) (in)

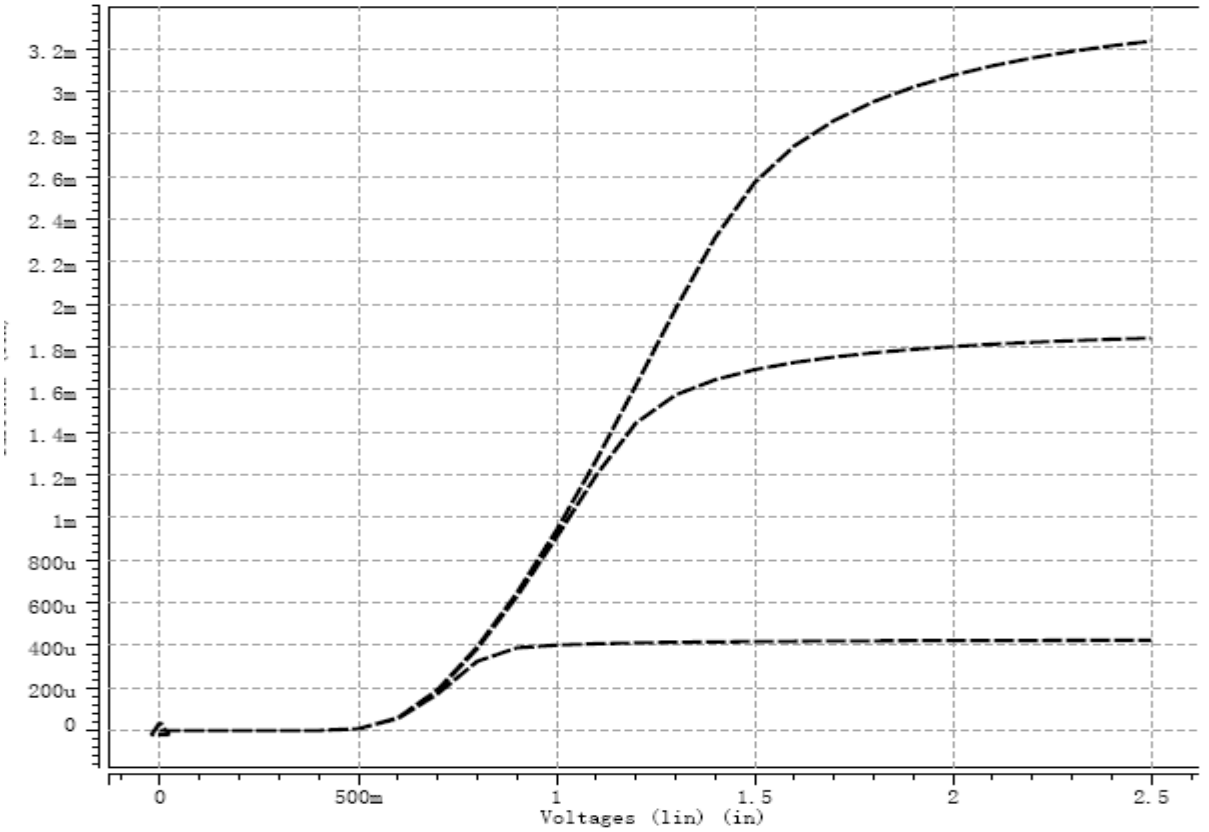
❖ nMOS E/E 反相器


n
out
in
n

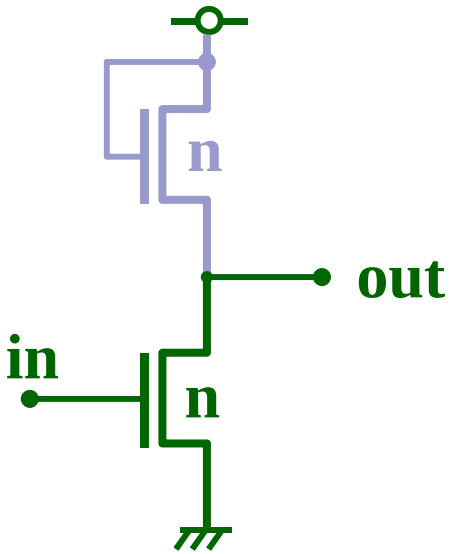

2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
Voltages (lin)
0
20n
40n
60n
80n
100n
Time (lin) (TIME)

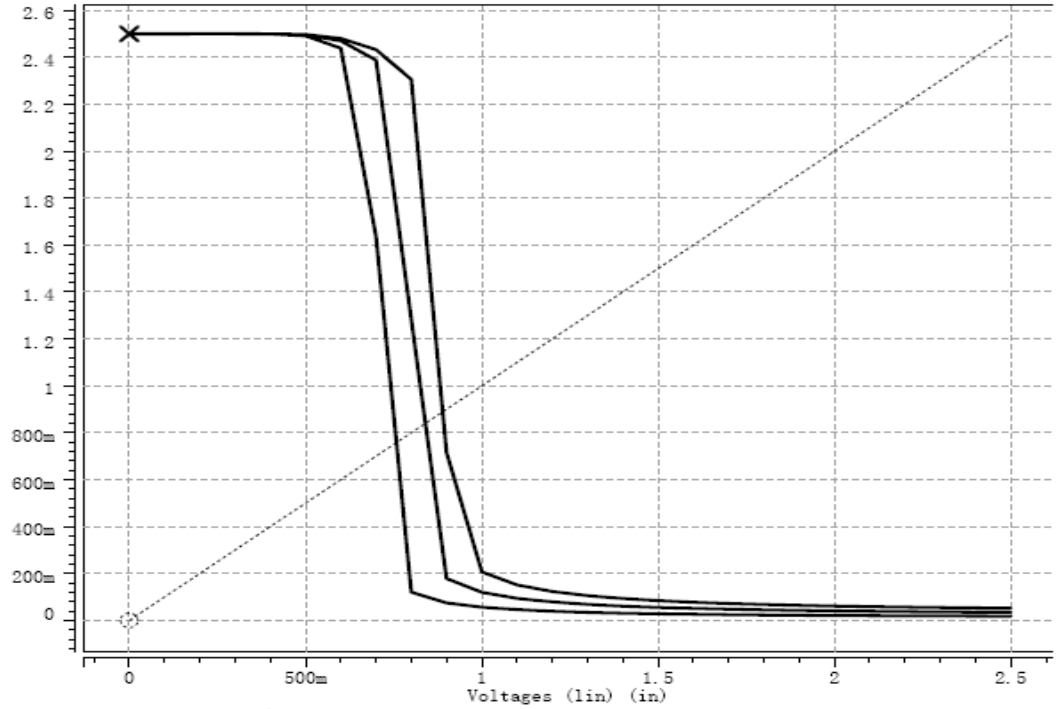
❖ nMOS E/E 反相器


n
out
in
n

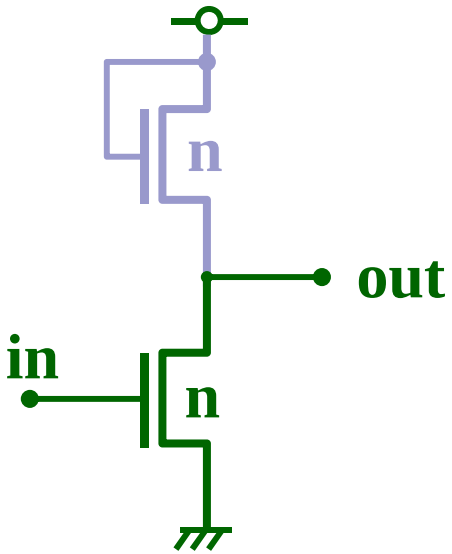

3.2m
3m
2.8m
2.6m
2.4m
2.2m
2m
1.8m
1.6m
1.4m
1.2m
1m
800u
600u
400u
200u
0
0
500m
1
1.5
2
2.5
Voltages (lin) (in)

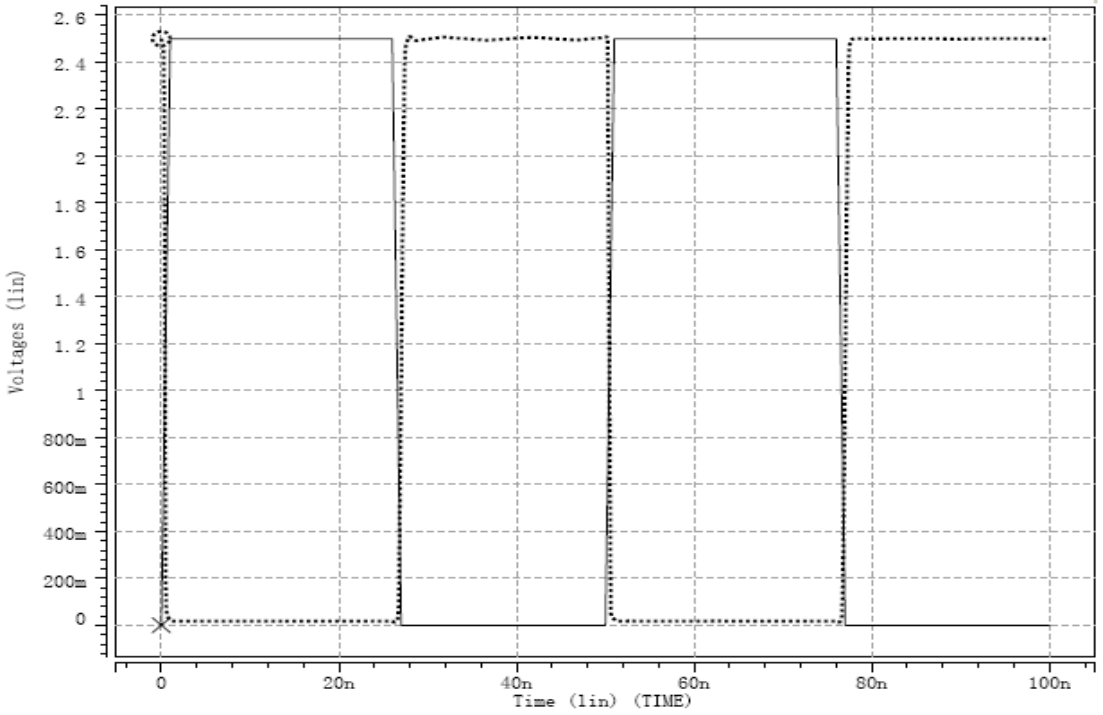
❖ nMOS E/D 反相器


n
out
in
n

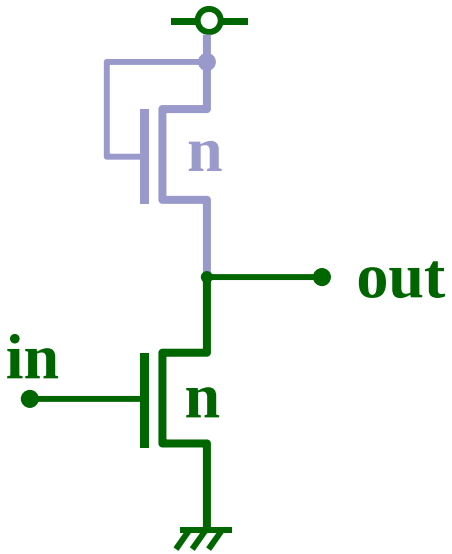

2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
500m
1
1.5
2
2.5
Voltages (lin) (in)

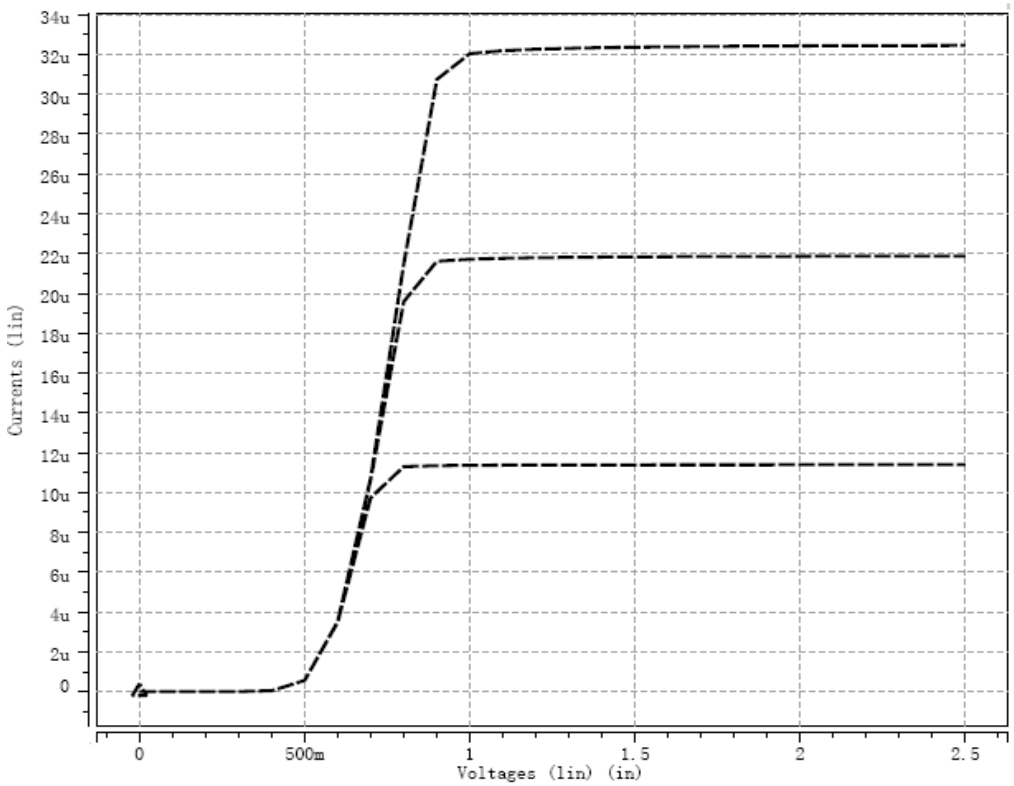
❖ nMOS E/D 反相器


n
out
in
n

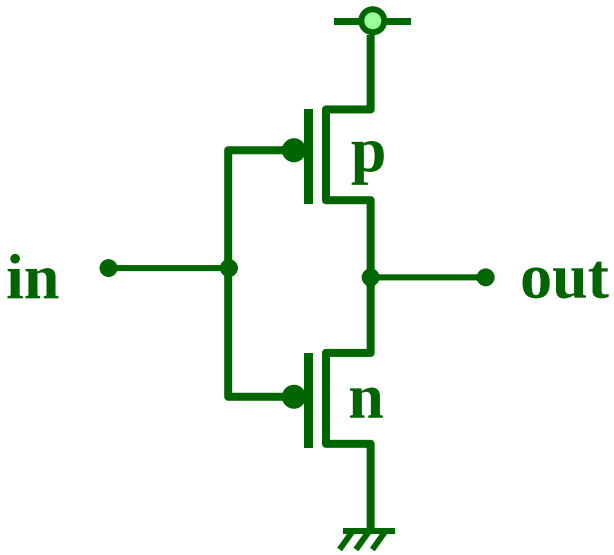

Voltages (lin)
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
0
20n
40n
60n
80n
100n
Time (lin) (TIME)

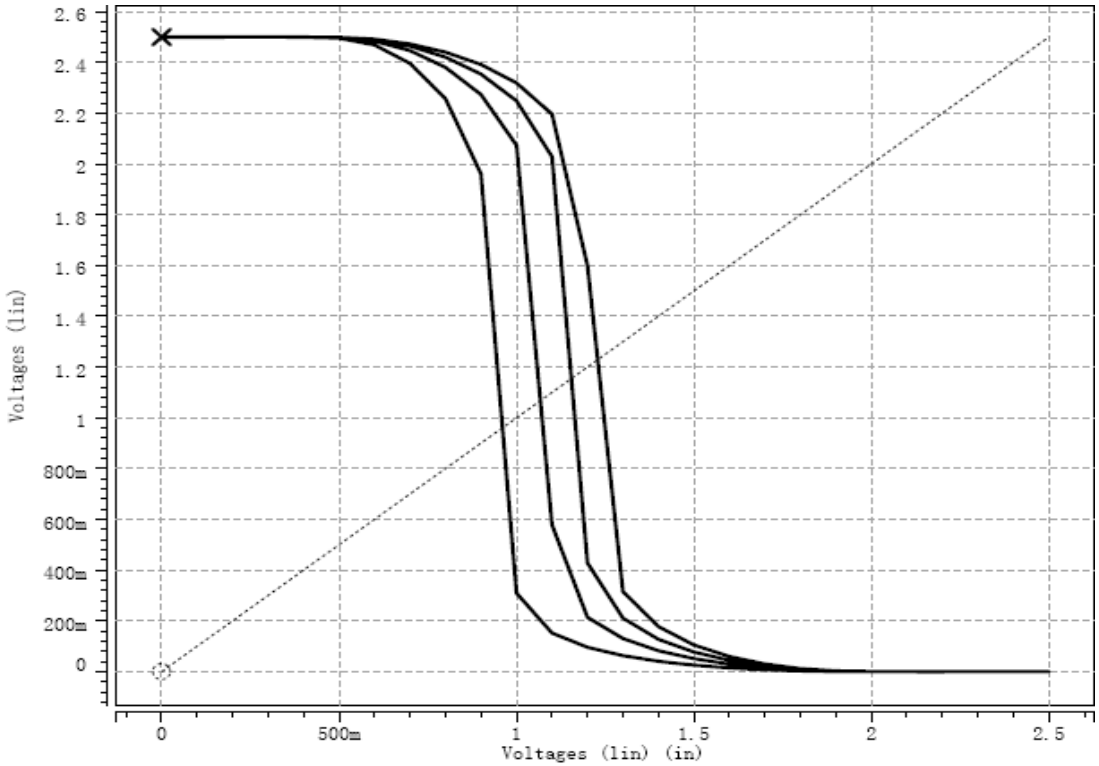
❖ nMOS E/D 反相器


n
out
in
n

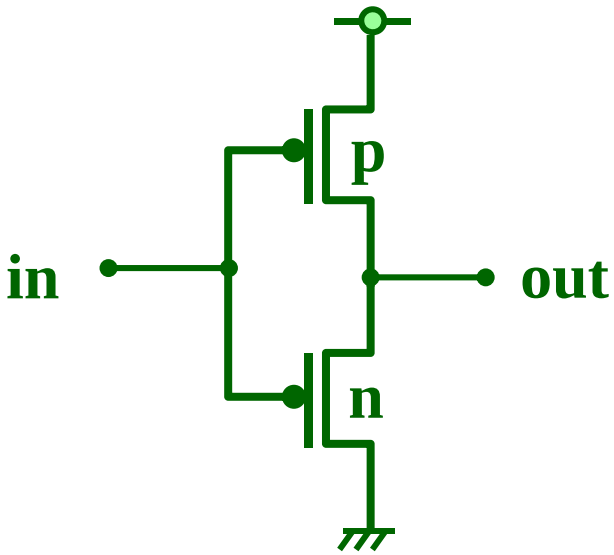

34u
32u
30u
28u
26u
24u
22u
20u
18u
16u
14u
12u
10u
8u
6u
4u
2u
0
Currents (lin)
0
500m
1
1.5
2
2.5
Voltages (lin) (in)

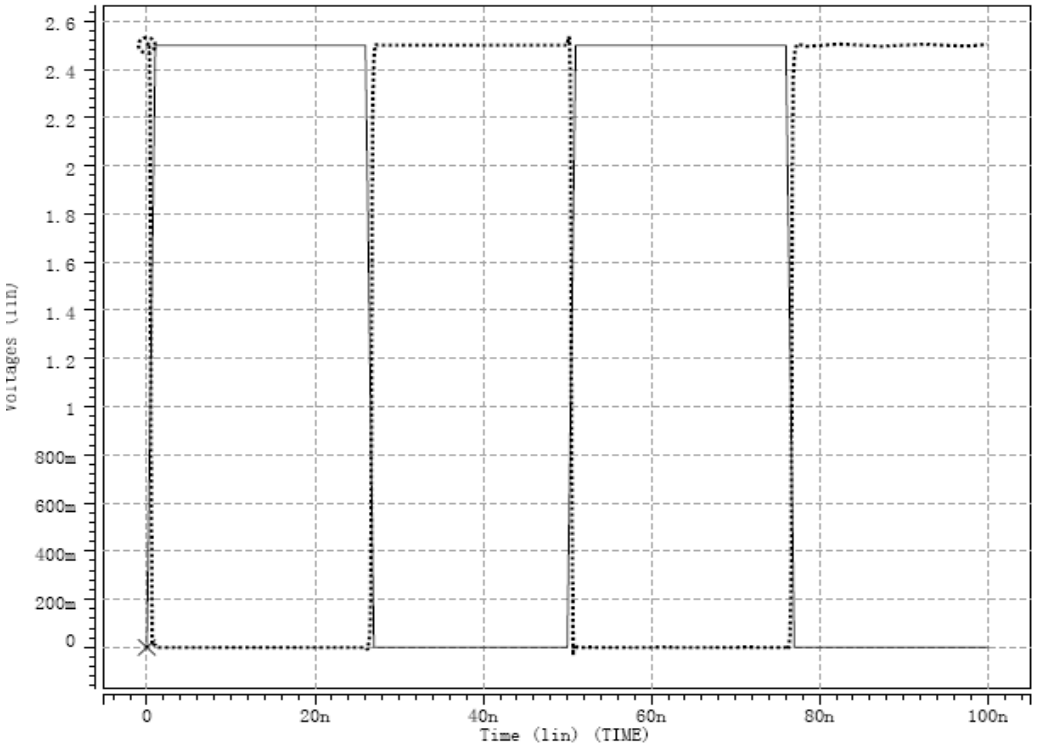
❖ CMOS反相器


in
p
n
out

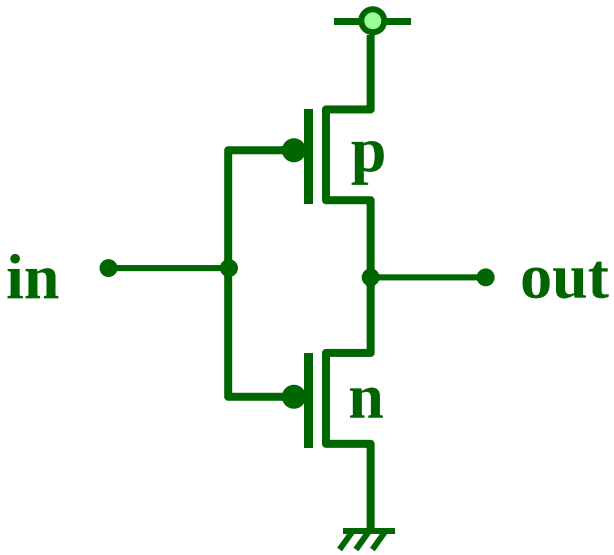

2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
Voltages (lin)
0
500m
1
1.5
2
2.5
Voltages (lin) (in)

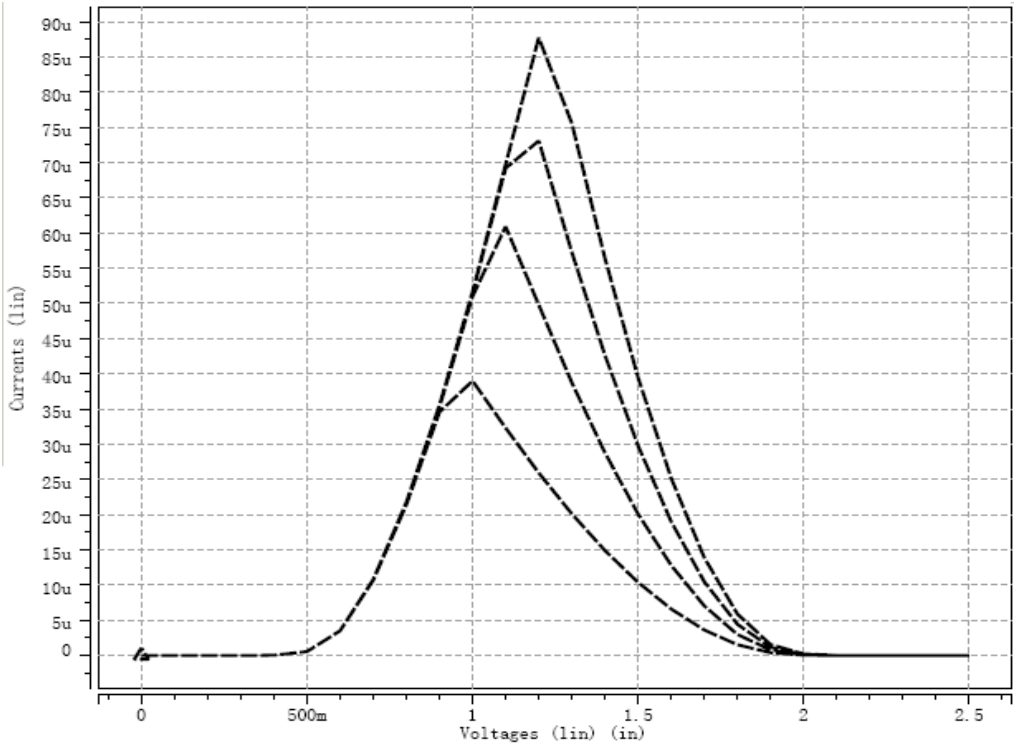
❖ CMOS反相器


in
p
n
out

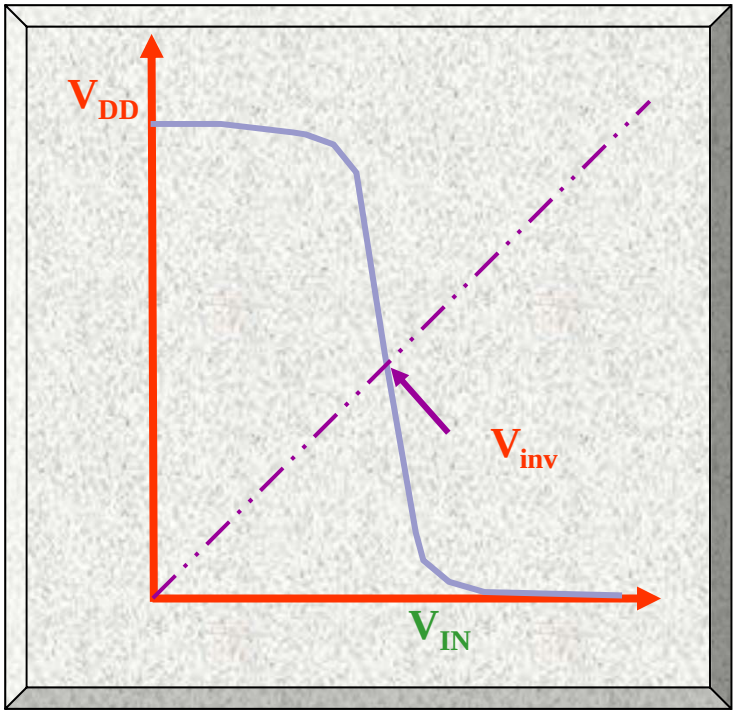

2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
Voltages (lin)
0
20n
40n
60n
80n
100n
Time (lin) (TIME)

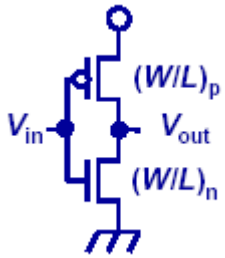
❖ CMOS反相器

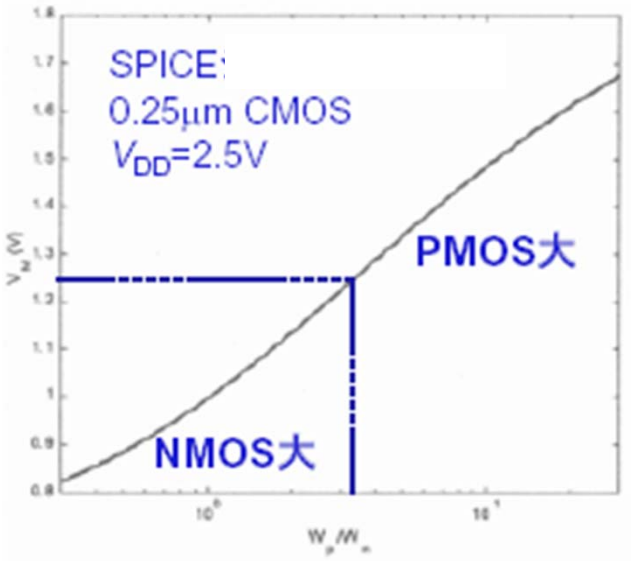

in
p
n
out


90u
85u
80u
75u
70u
65u
60u
55u
50u
45u
40u
35u
30u
25u
20u
15u
10u
5u
0
Currents (lin)
0
500m
1
1.5
2
2.5
Voltages (lin) (in)

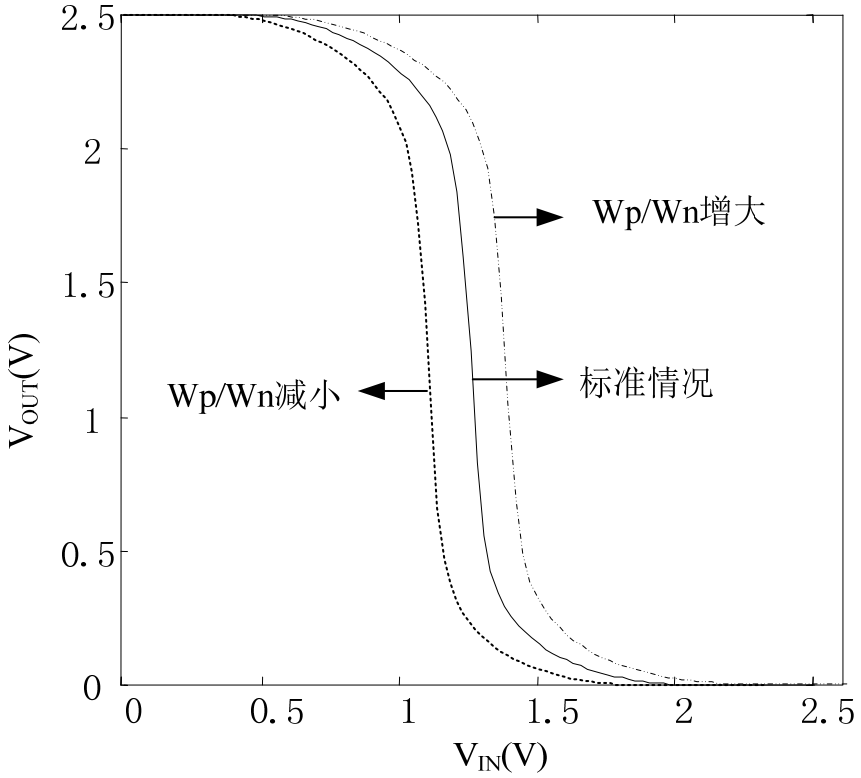
CMOS反向器的逻辑阈值



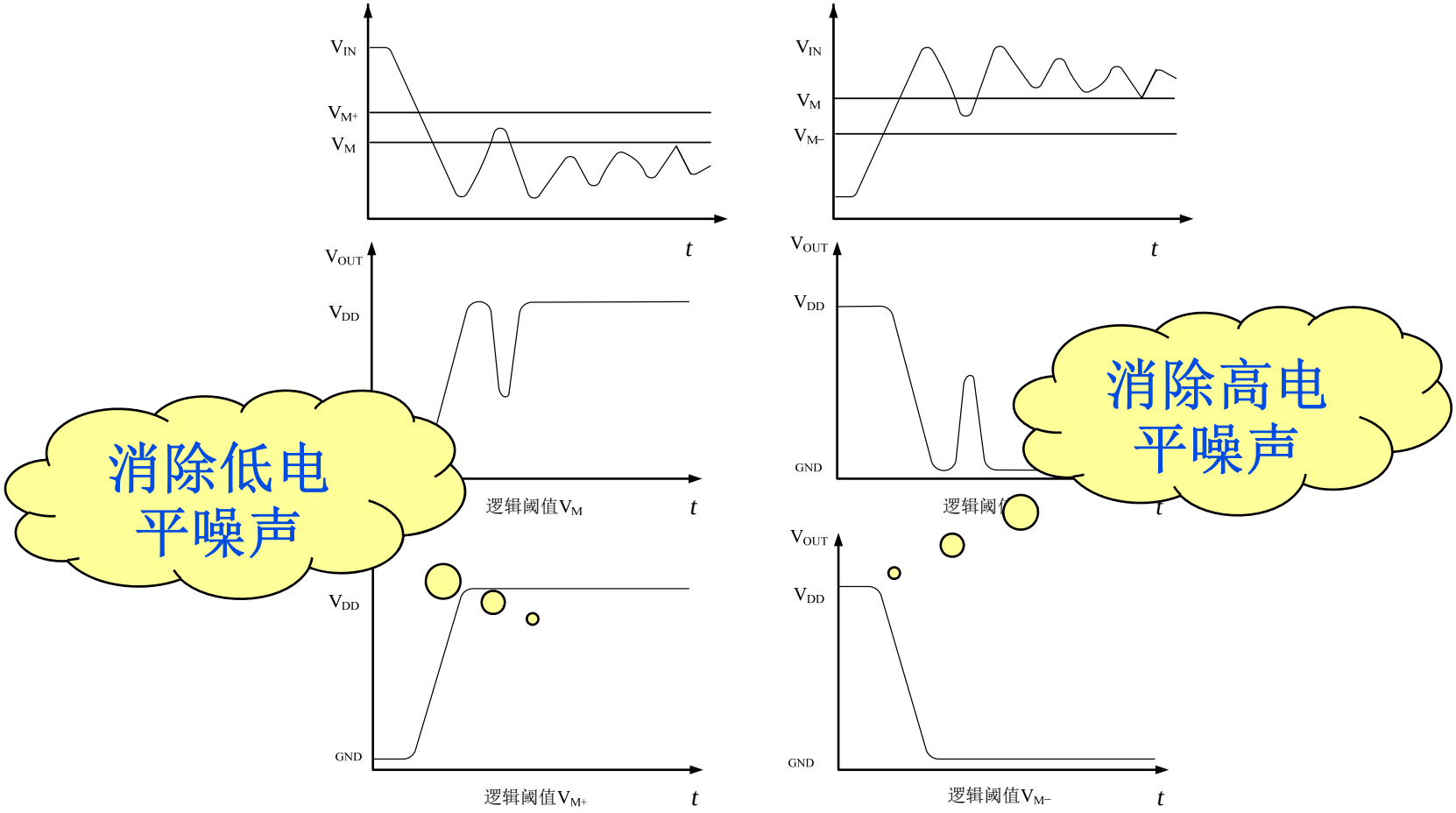




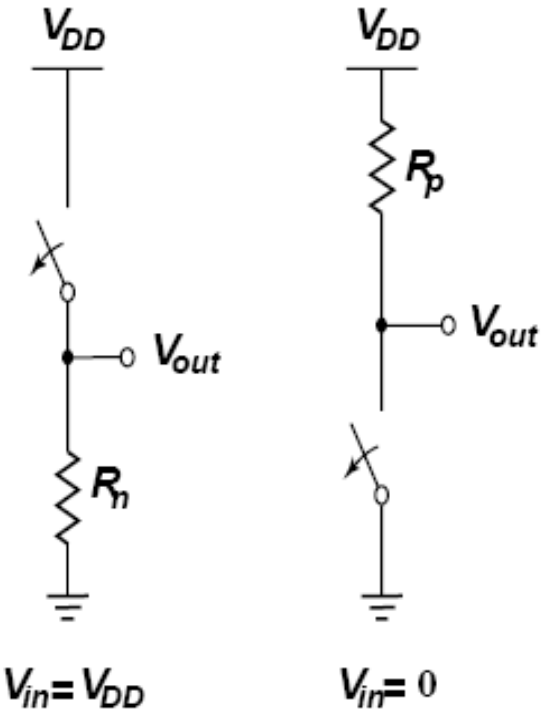
CMOS反向器的逻辑阈值



逻辑阈值的实际应用

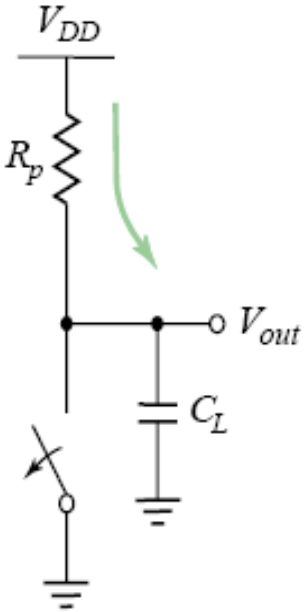

V_{IN}
V_{M+}
V_M
t
V_{OUT}
V_{DD}
GND
逻辑阈值V_M
逻辑阈值V_{M+}
V_{IN}
V_M
V_{M-}
t
V_{OUT}
V_{DD}
GND
逻辑阈值V_{M-}
消除低电平噪声
消除高电平噪声

CMOS反相器的瞬态特性

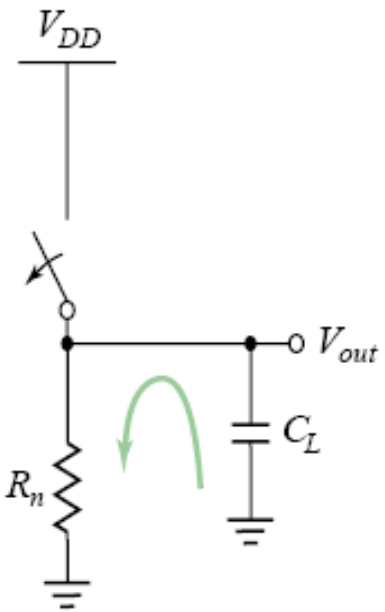


直流分析

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$



(a) 低至高过渡

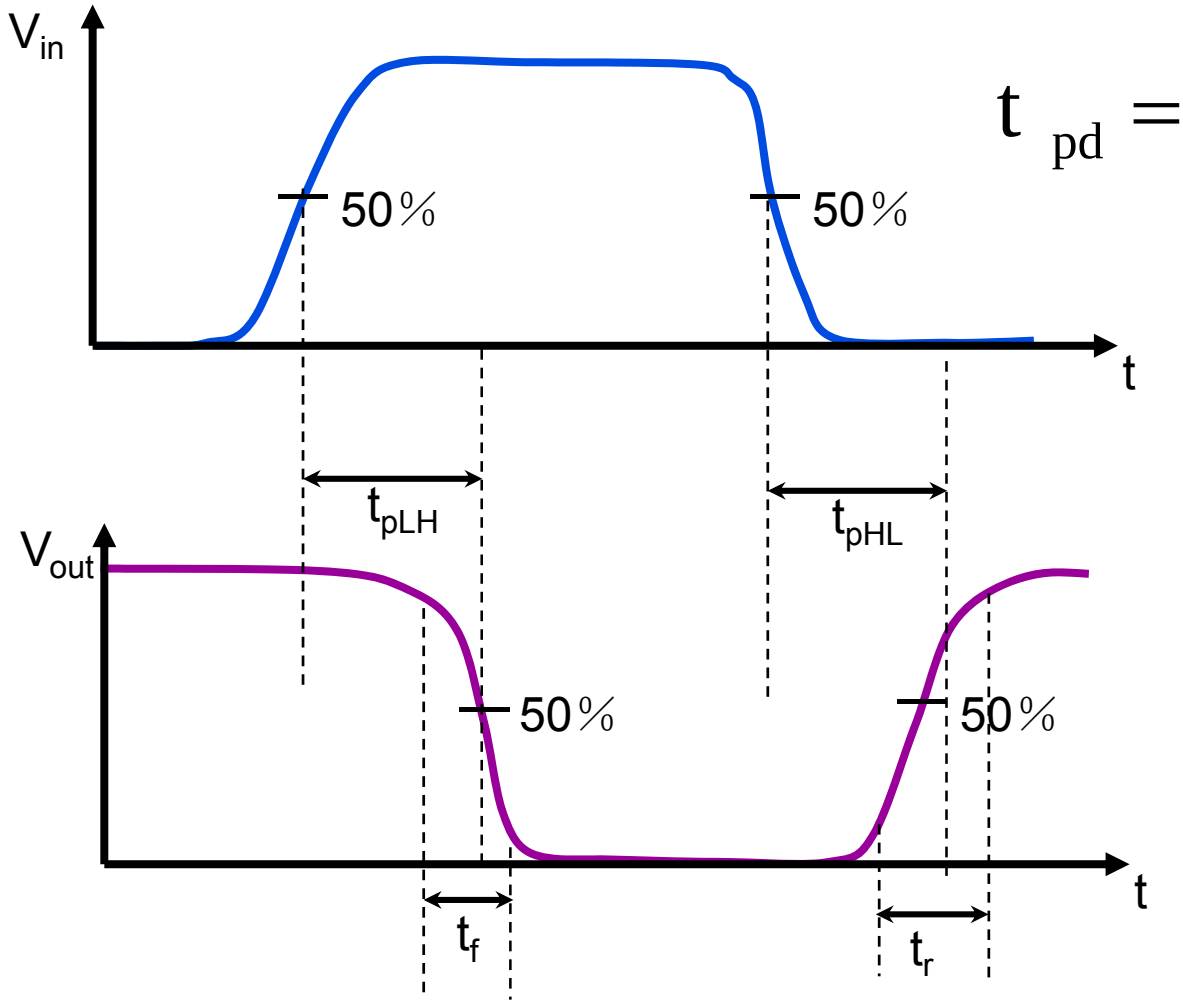


(b) 高至低过渡

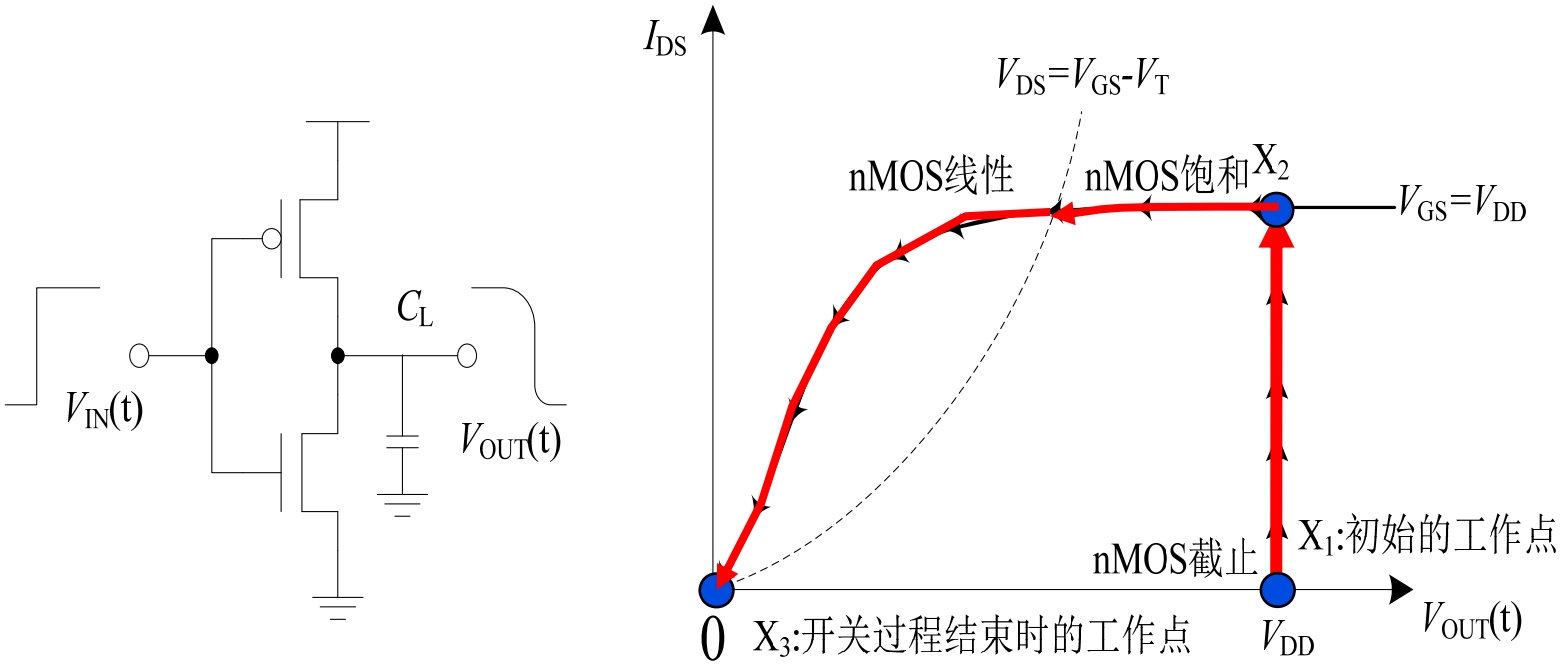
瞬态特性决定了电路的开关时间和工作速度

CMOS反相器的瞬态特性

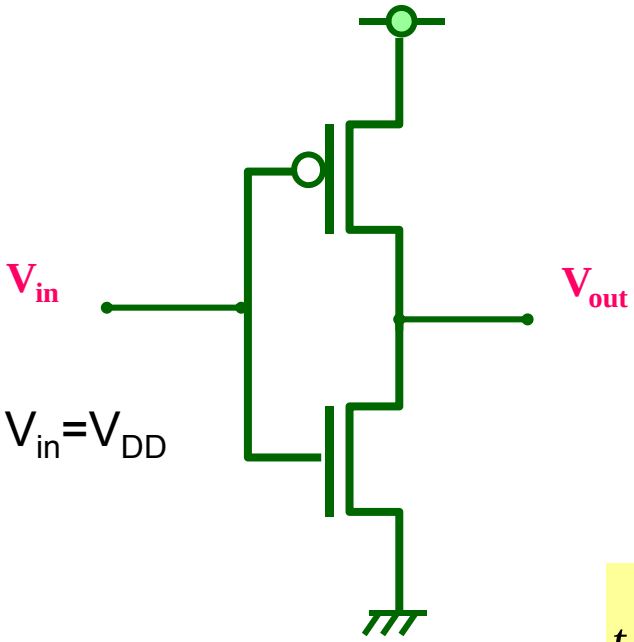
1. 延迟时间t_{pd}(传播时间)　　2.上升时间 t_r　　3.下降时间t_f



$$t_{pd} = \frac{t_{PLH} + t_{PHL}}{2}$$


C_L
$V_{IN}(t)$
$V_{OUT}(t)$
I_{DS}
$V_{DS}=V_{GS}-V_T$
nMOS线性
nMOS饱和
X_2
$V_{GS}=V_{DD}$
nMOS截止
X_1:初始的工作点
0
X_3:开关过程结束时的工作点
V_{DD}
$V_{OUT}(t)$

CMOS反相器的下降时间t_f



1. V_{OUT} 从$90\%V_{DD}$ 下降到 $V_{DD}-V_{TH}$

N管的$V_{DS}>V_{GS}-V_{TH}$，工作在饱和区

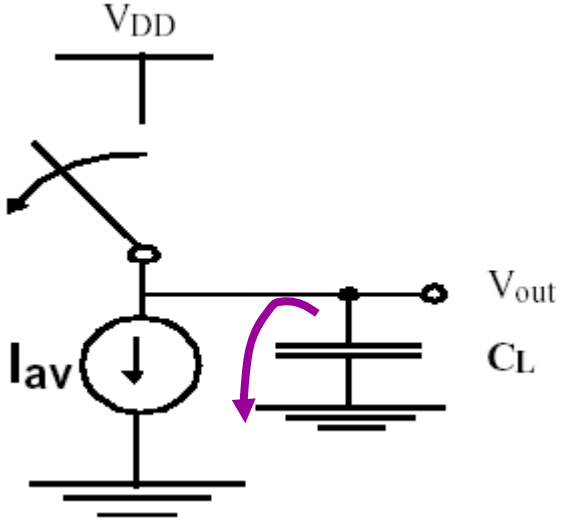
$$C_L\frac{dV_O}{dt}+K_N(V_{DD}-V_{TN})^2=0$$

$$dt=-\frac{C_L}{K_N(V_{DD}-V_{TN})^2}dV_O$$

$$t_{f1}=\int_{0.9V_{DD}}^{V_{DD}-V_{TN}}-\frac{C_L}{K_N(V_{DD}-V_{TN})^2}dV_O$$

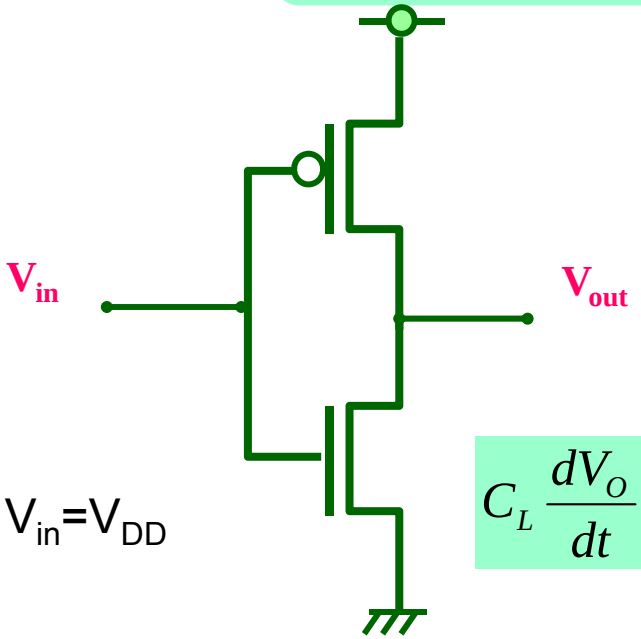
$$=-\frac{C_L}{K_N(V_{DD}-V_{TN})^2}\int_{0.9V_{DD}}^{V_{DD}-V_{TN}}dV_O$$

$$=\frac{C_L(V_{TN}-0.1V_{DD})}{K_N(V_{DD}-V_{TN})^2}$$



饱和区

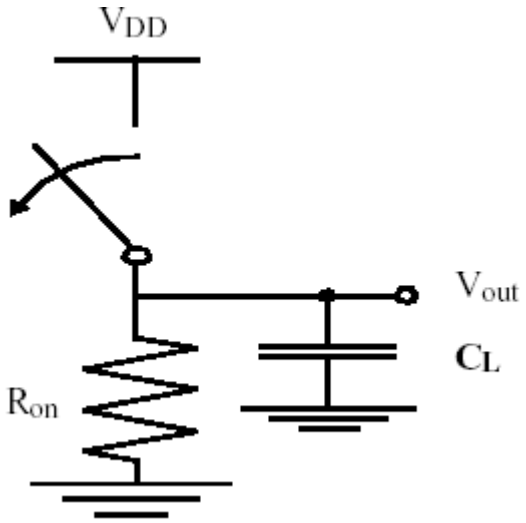
CMOS反相器的下降时间t_f



2. V_{OUT} 从V_{DD}-V_{TH} 下降到 10%V_{DD}

N管的V_{DS}<V_{GS}-V_{TH}，工作在线性区

$$C_L\frac{dV_O}{dt}+K_N[2(V_{DD}-V_{TN})V_O-V_O^{\,2}]=0$$

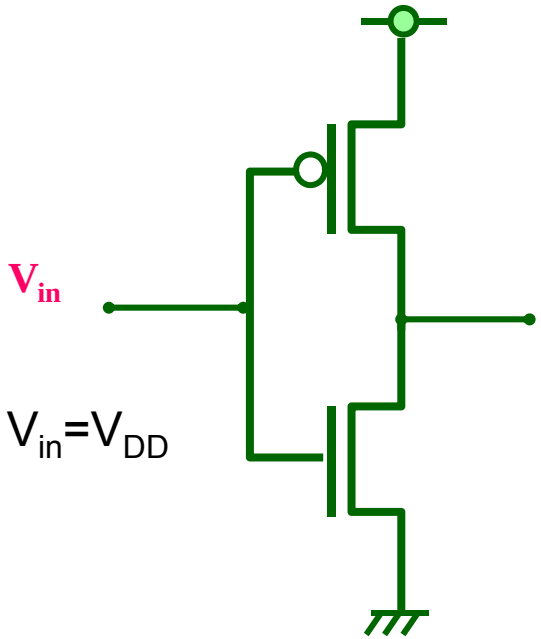


线性区

$$t_{f2}=-\frac{C_L}{2K_N(V_{DD}-V_{TN})}\int_{V_{DD}-V_{TN}}^{0.1V_{DD}}\frac{dV_O}{V_O^{\,2}/2(V_{DD}-V_{TN})}$$

$$=\frac{C_L}{2K_N(V_{DD}-V_{TN})}ln(\frac{19V_{DD}-20V_{TN}}{V_{DD}})$$

CMOS反相器的下降时间t_f



$$t_f = t_{f1} + t_{f2}$$

$$t_f = \frac{C_L(V_{TN} - 0.1V_{DD})}{K_N(V_{DD} - V_{TN})^2} + \frac{C_L}{2K_N(V_{DD} - V_{TN})} ln(\frac{19V_{DD} - 20V_{TN}}{V_{DD}})$$

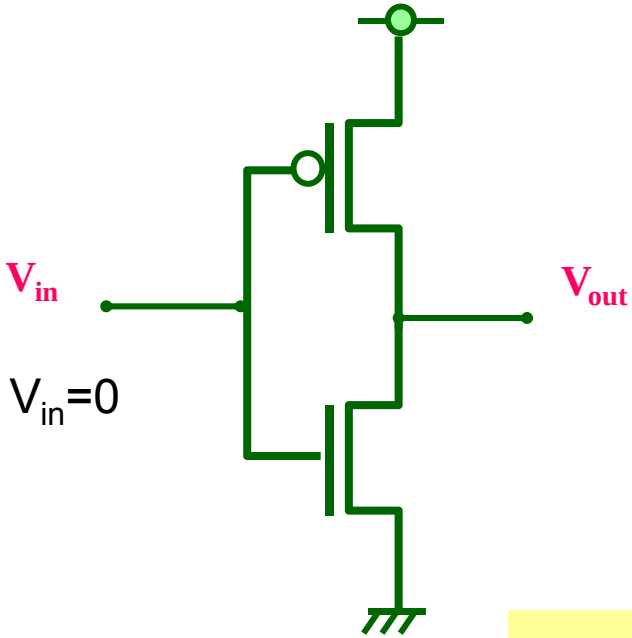
$$= \frac{C_L}{K_N(V_{DD} - V_{TN})} [\frac{(V_{TN} - 0.1V_{DD})}{(V_{DD} - V_{TN})} + \frac{1}{2} ln(\frac{19V_{DD} - 20V_{TN}}{V_{DD}})]$$

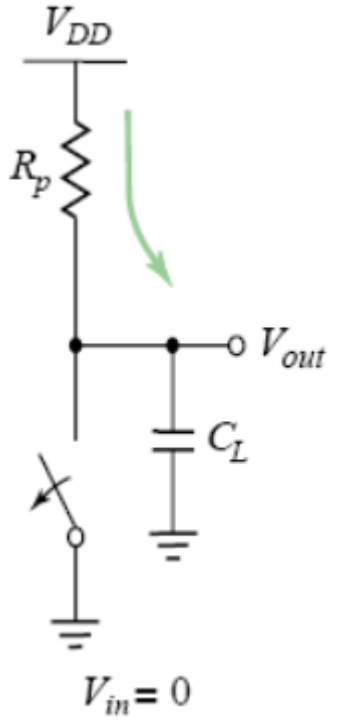
设$V_{TN} \approx 0.2V_{DD}$，则

$$t_f \approx 2\frac{C_L}{k_N V_{DD}}$$

下降时间由N管的尺寸决定

CMOS反相器的上升时间t_r

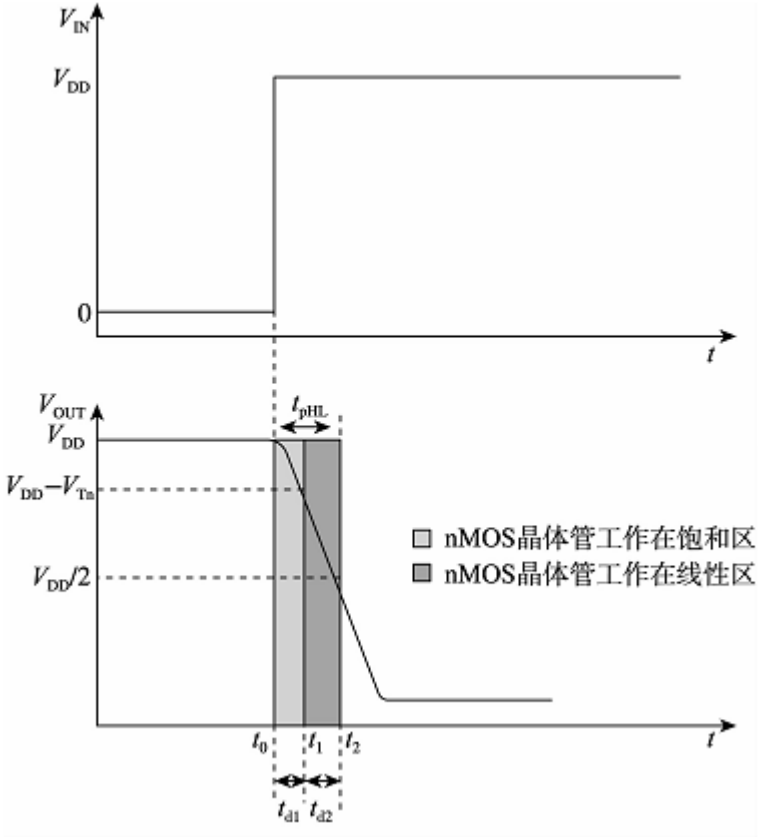




设$|V_{TP}| \approx 0.2V_{DD}$，则 $t_r \approx 2\dfrac{C_L}{k_P V_{DD}}$ 上升时间由P管的尺寸决定

如果N管和P管尺寸相等，$K_P \approx 0.5K_N(\mu_p \approx 0.5\ \mu_n)$,则$t_r \approx 2t_f$，因此，若希望$t_r = t_f$，则$W_P \approx 2W_N$

CMOS反相器的延迟时间t_{pd}



$$C_L\frac{dV_{OUT}}{dt}+k_n(V_{DD}-V_{Tn})^2=0$$

$$t_{d1}=-\frac{C_L}{k_n(V_{DD}-V_{Tn})^2}\int_{V_{DD}}^{V_{DD}-V_{Tn}}dV_{OUT}=-\frac{2C_LV_{Tn}}{k_n(V_{DD}-V_{Tn})^2}$$

$$t_{d2}=\frac{-C_L}{2k_n(V_{DD}-V_{Tn})^2}\int_{0.5V_{DD}}^{V_{DD}-V_{Tn}}\frac{dV_{OUT}}{V_{OUT}^2/2(V_{DD}-V_{Tn})-V_{OUT}}$$

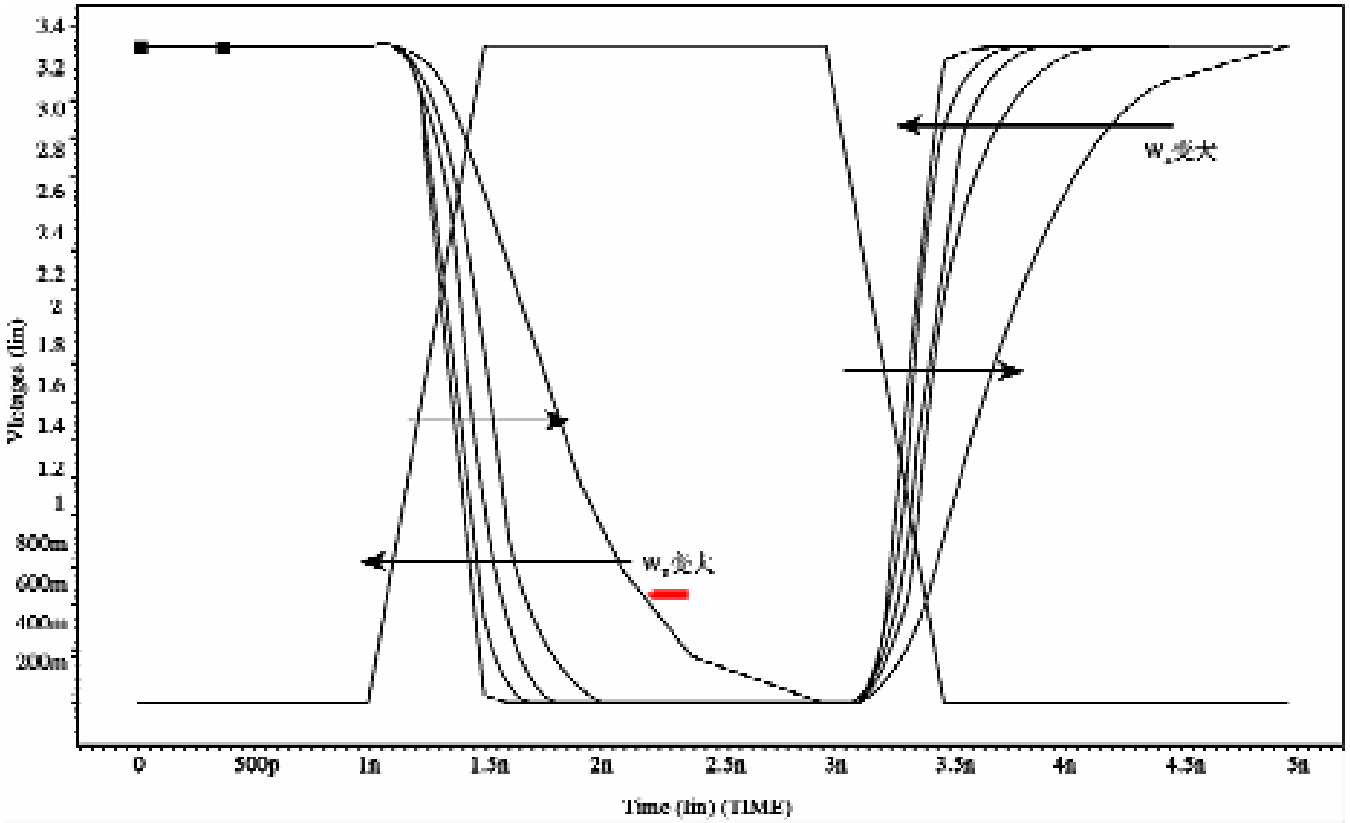
$$=\frac{C_L}{k_n(V_{DD}-V_{Tn})}\ln\left(\frac{3V_{DD}-4V_{Tn}}{V_{DD}}\right)$$

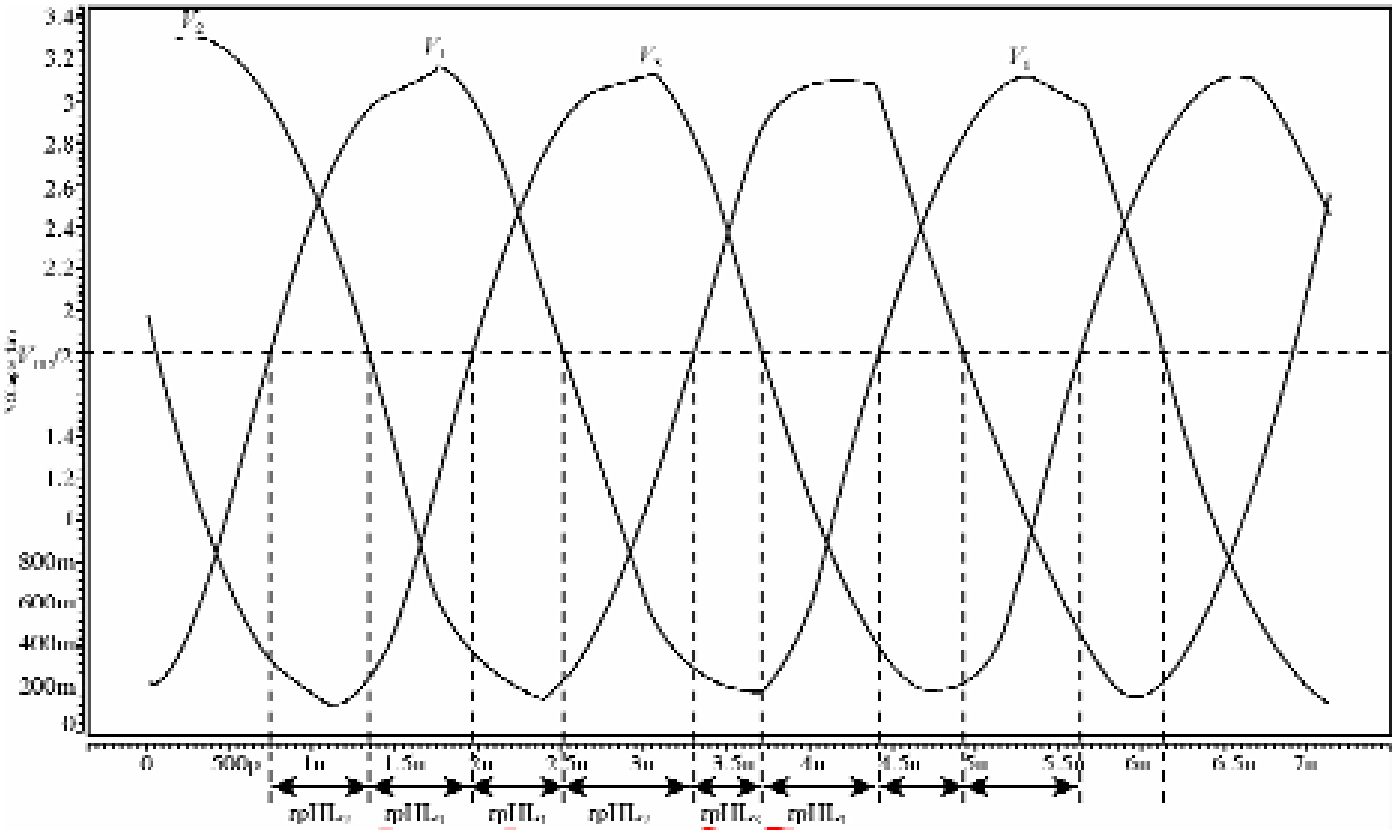
$$t_{pHL}=t_{d1}+t_{d2}$$

$$=\frac{C_L}{k_n(V_{DD}-V_{Tn})}\left[\frac{2V_{Tn}}{V_{DD}-V_{Tn}}+\ln\left(\frac{3V_{DD}-4V_{Tn}}{V_{DD}}\right)\right]$$

$$t_{pHL}\approx\frac{6C_L}{5k_nV_{DD}}$$

$$t_{pLH}\approx\frac{6C_L}{5k_pV_{DD}}$$


Voltages (lin)
3.4
3.2
3.0
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
500p
1n
1.5n
2n
2.5n
3n
3.5n
4n
4.5n
5n
Time (lin) (TIME)
W2变大
W1变大



CMOS反相器的设计

反相器的设计主要是确定MOS管的宽度

对有比反相器：

根据V_{OL}确定两管尺寸

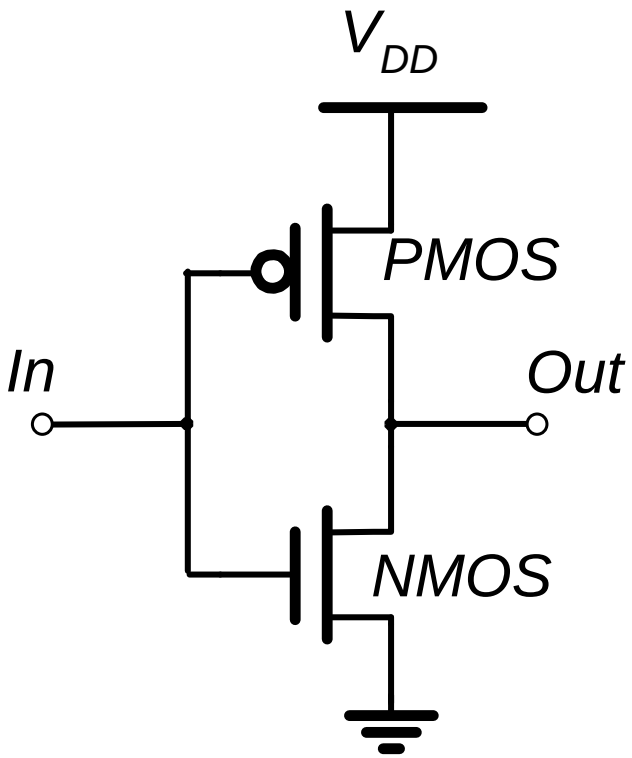
对CMOS反相器:

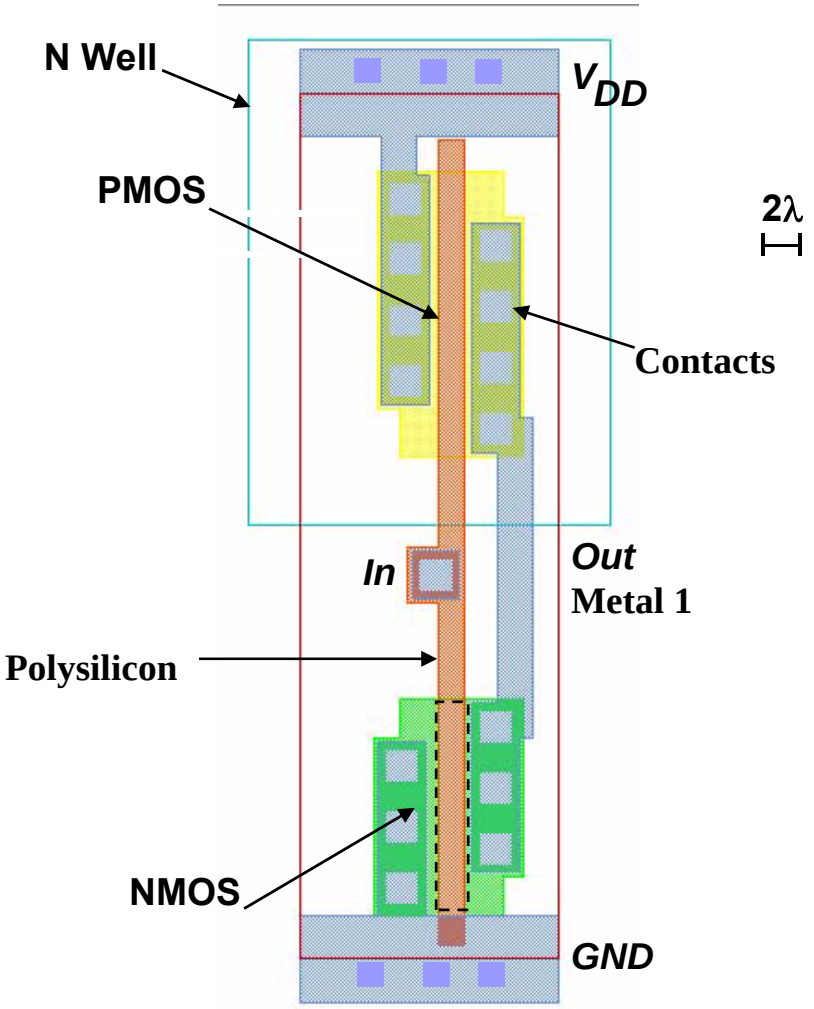
1.根据V_M确定尺寸

$$V_M = \frac{V_{DD} + V_{TP} + V_{TN}\sqrt{K_R}}{1+\sqrt{K_R}}$$

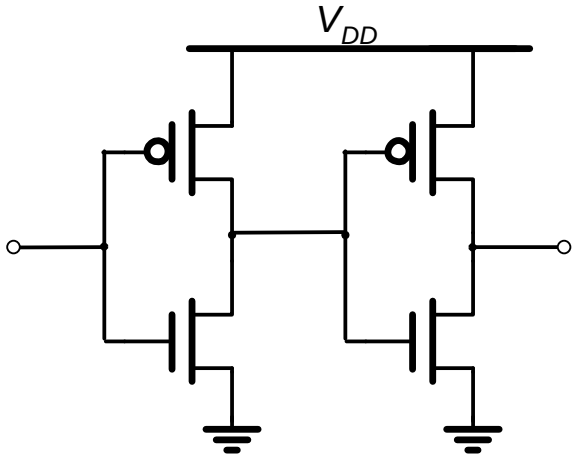
2.根据上升下降时间相等原则设计（$W_P/W_N \approx 2:1$)

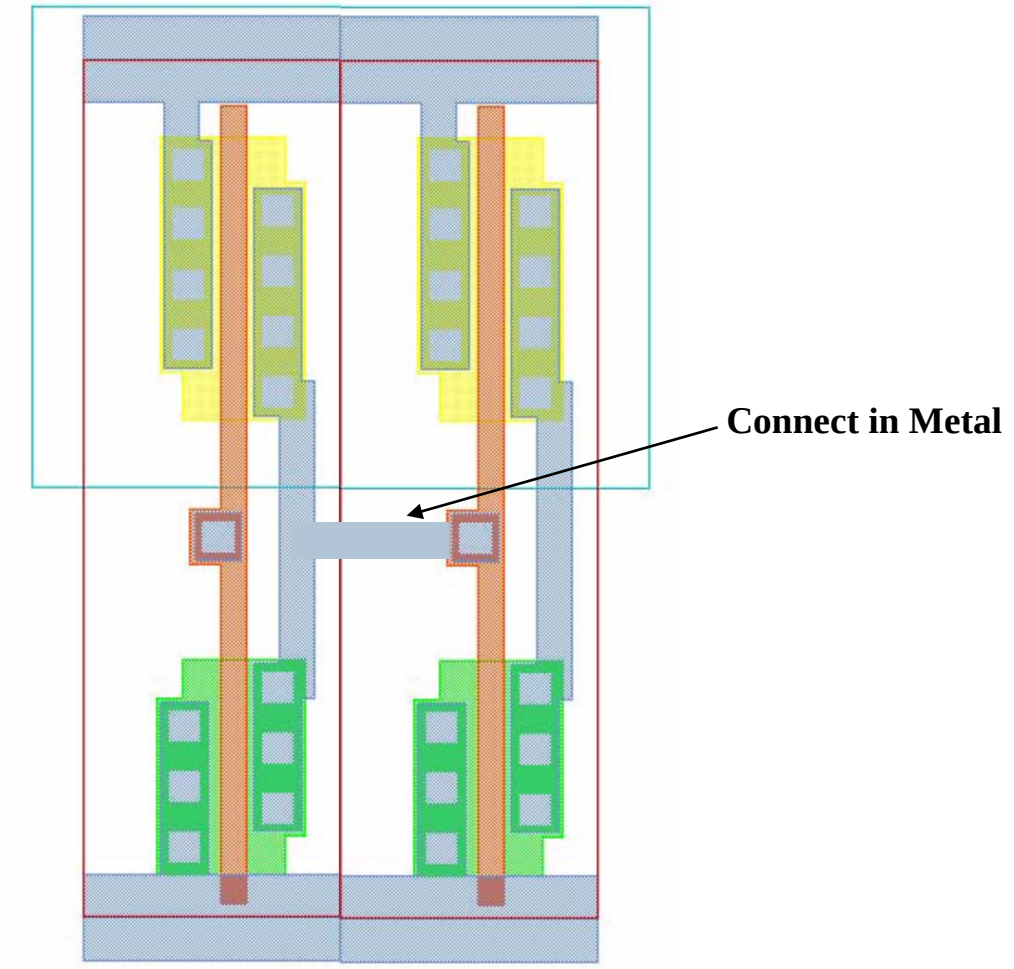
CMOS 反相器版图


V_{DD}
PMOS
In
Out
NMOS


N Well
V_{DD}
PMOS
2λ
Contacts
In
Out
Metal 1
Polysilicon
NMOS
GND

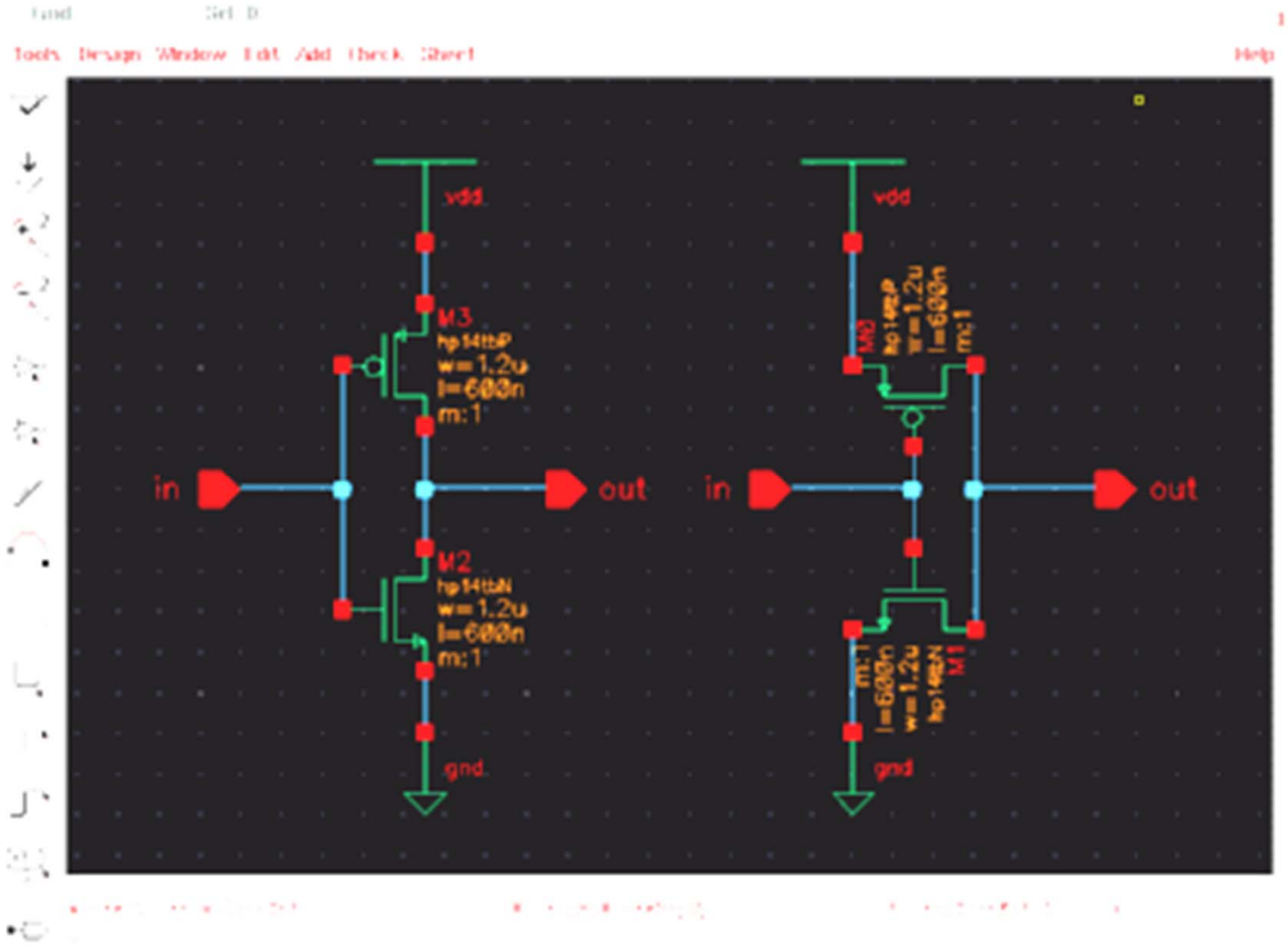
Two Inverters



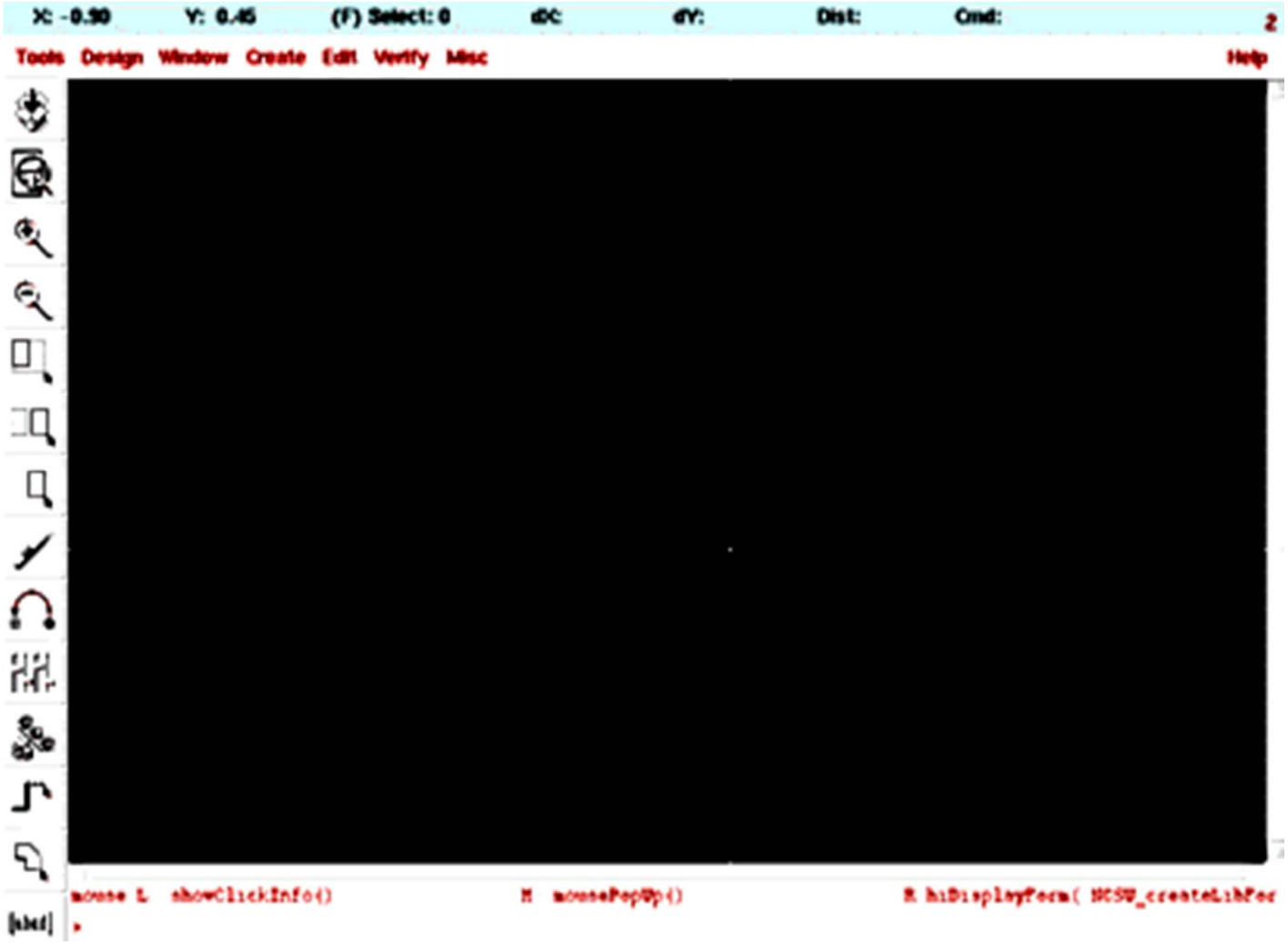


Example: CMOS Inverter Layout

Design Idea

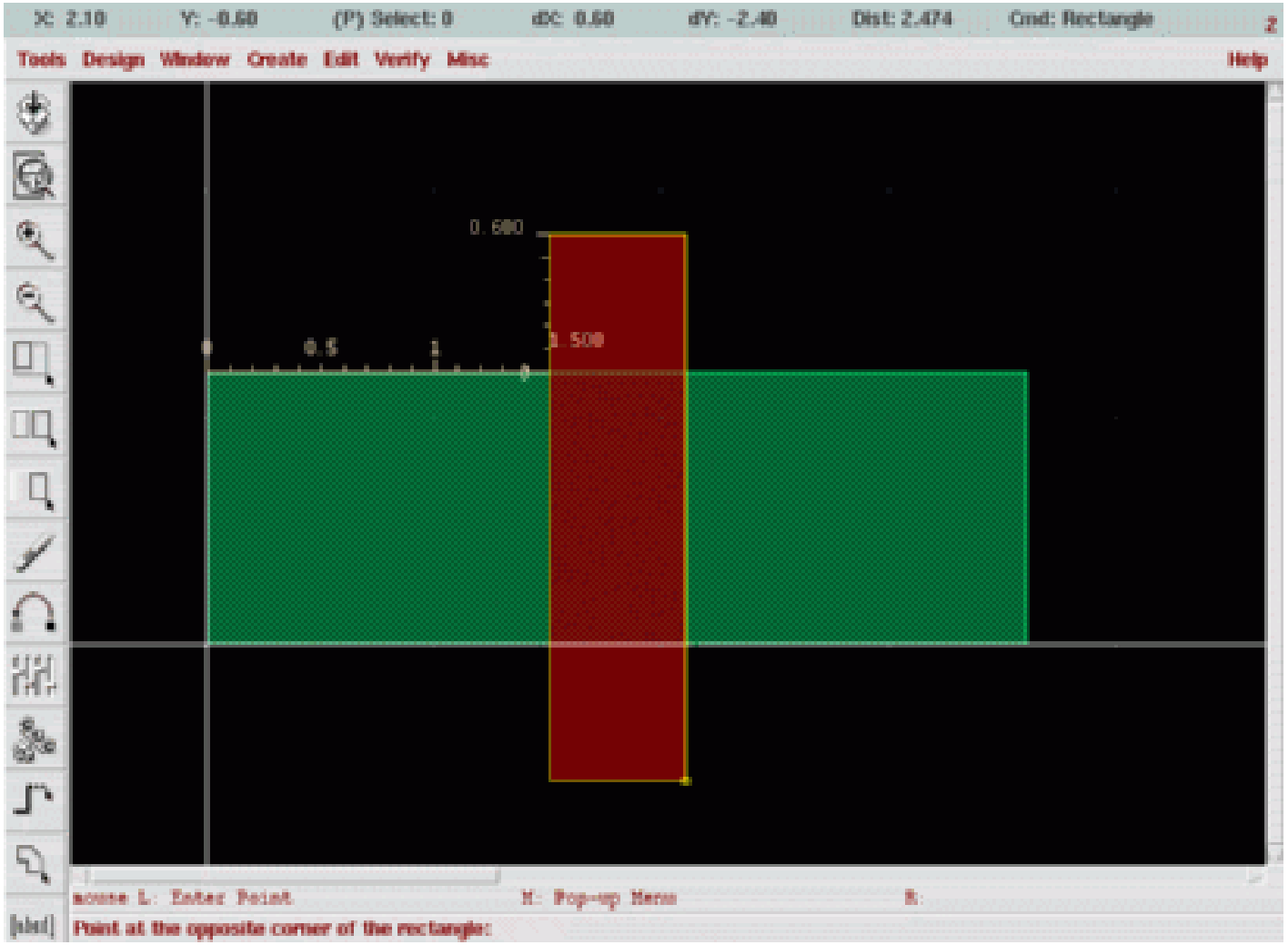


Virtuoso and LSW

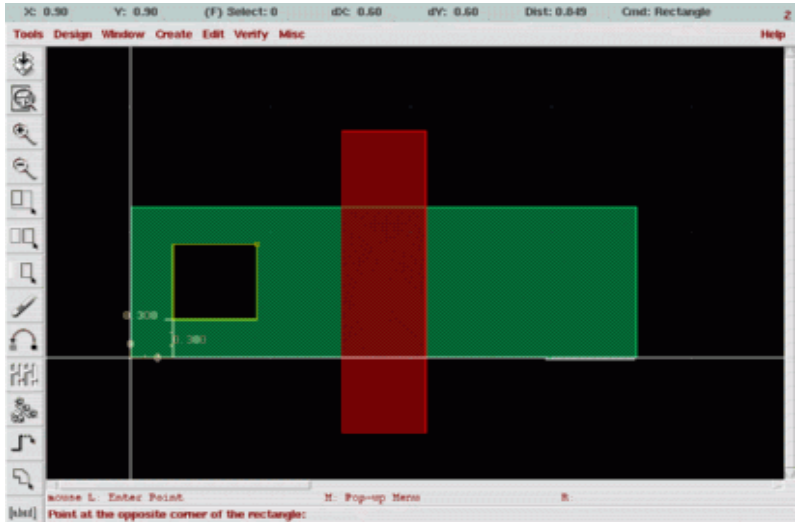


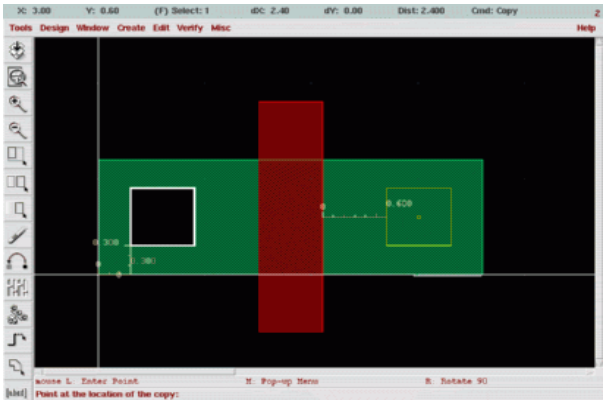
Drawing the N-Diffusion (Active)

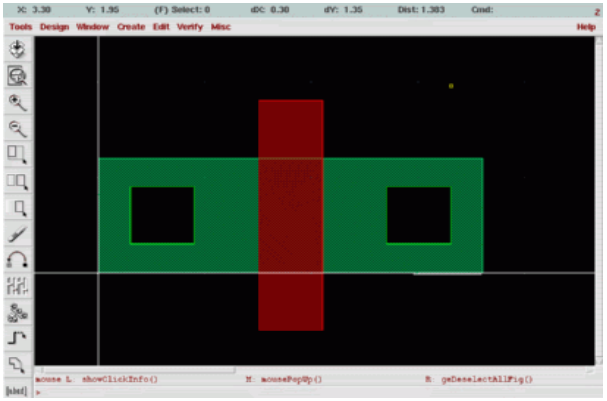
The Gate Poly



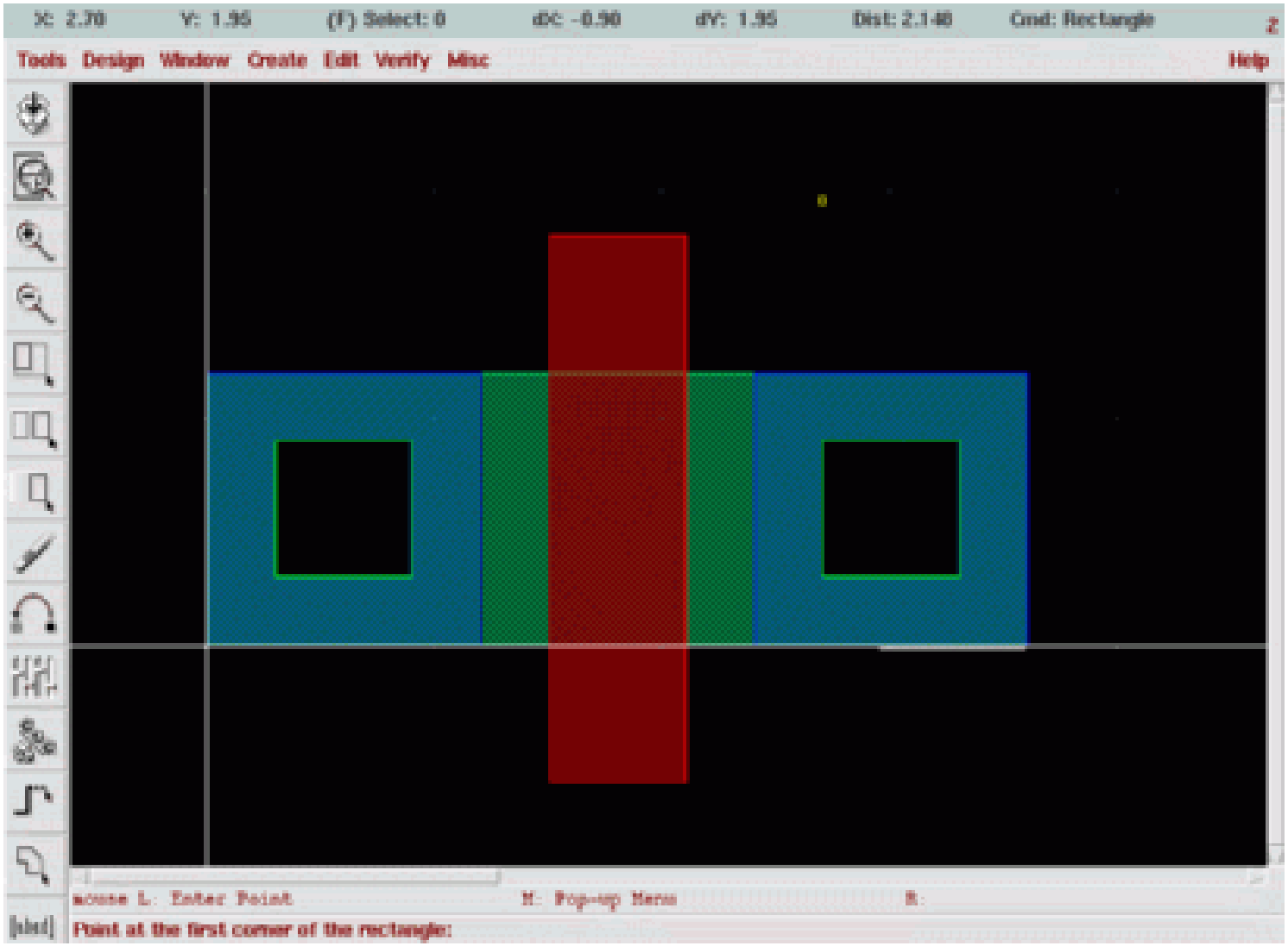
Making Active Contacts



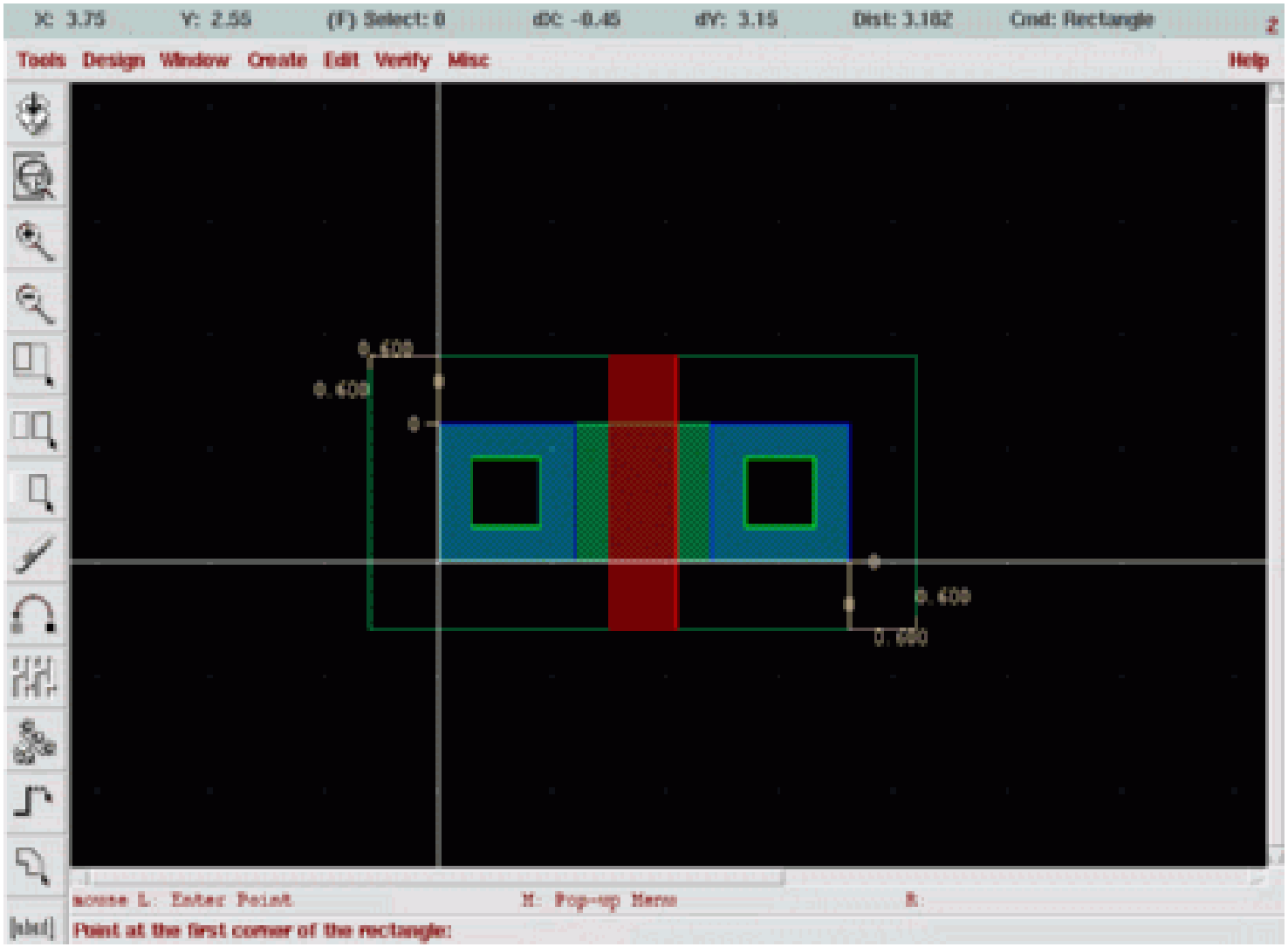




Covering Contacts with Metal-1

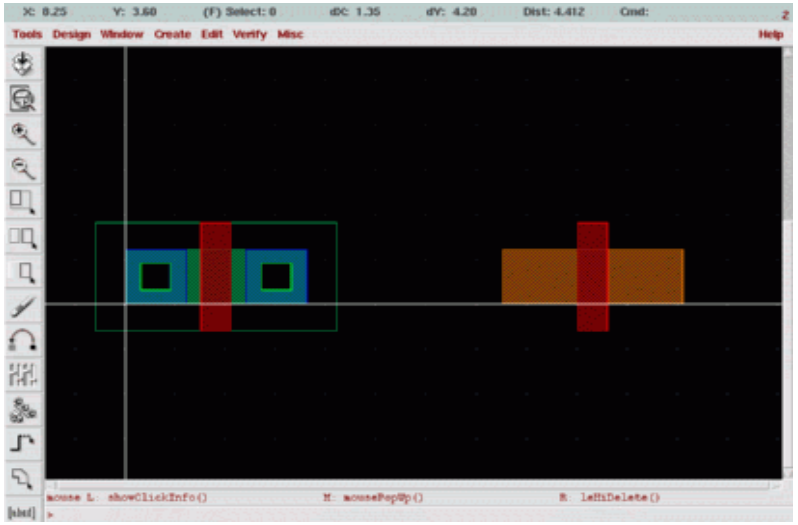


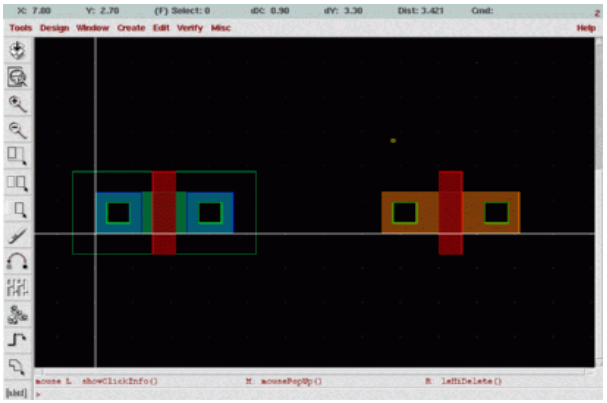
The N-Select Layer

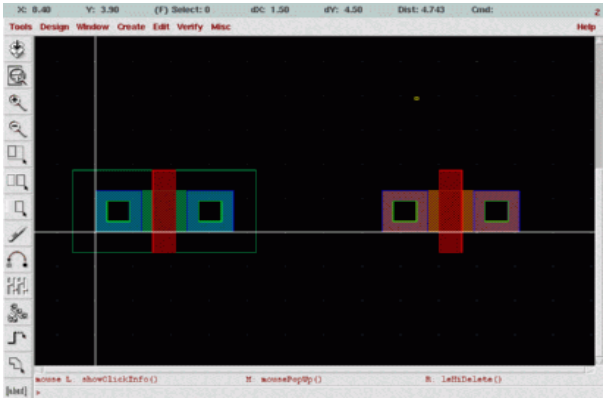


Drawing the P-Diffusion (Active)

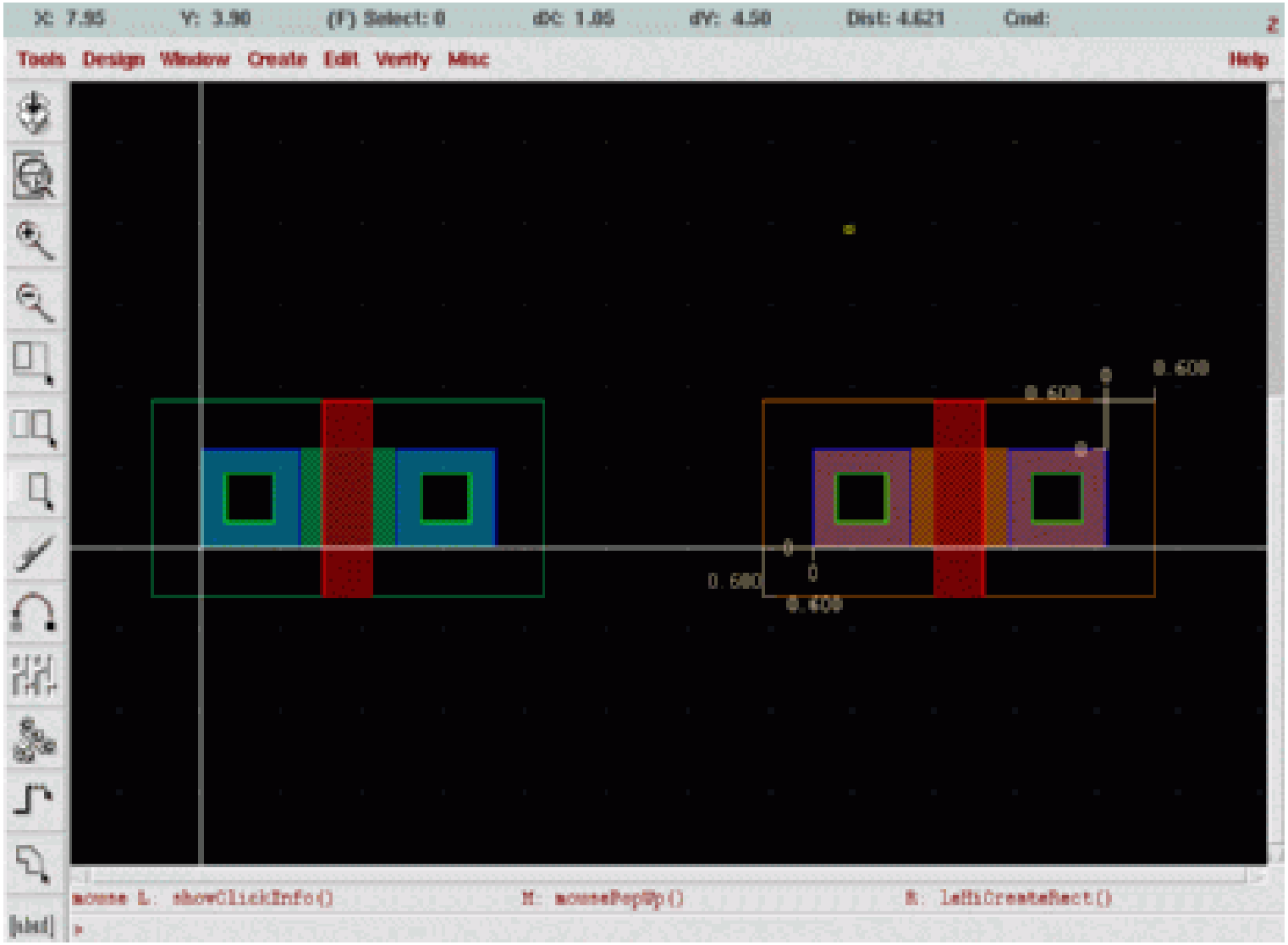
Transistor Features



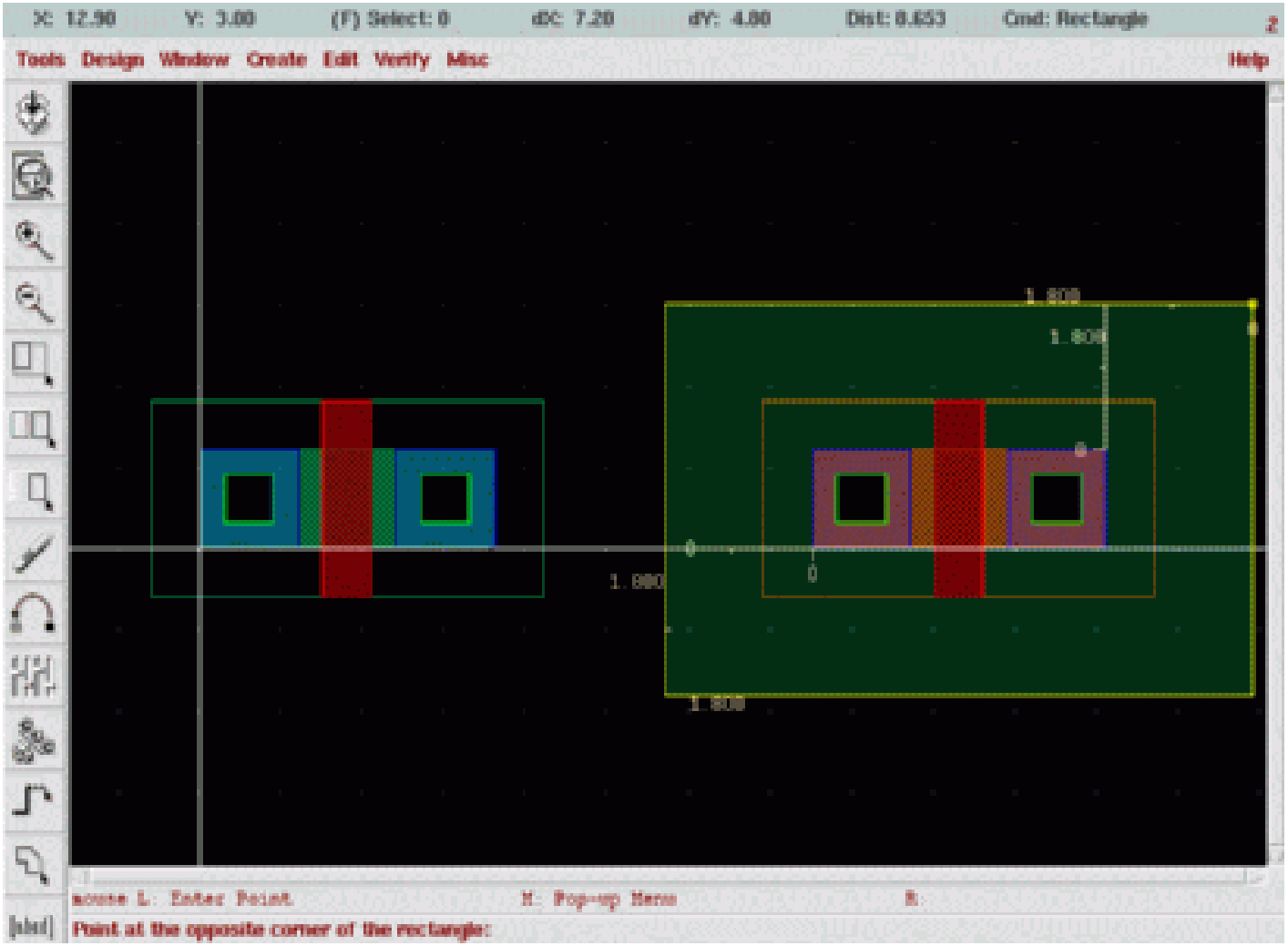




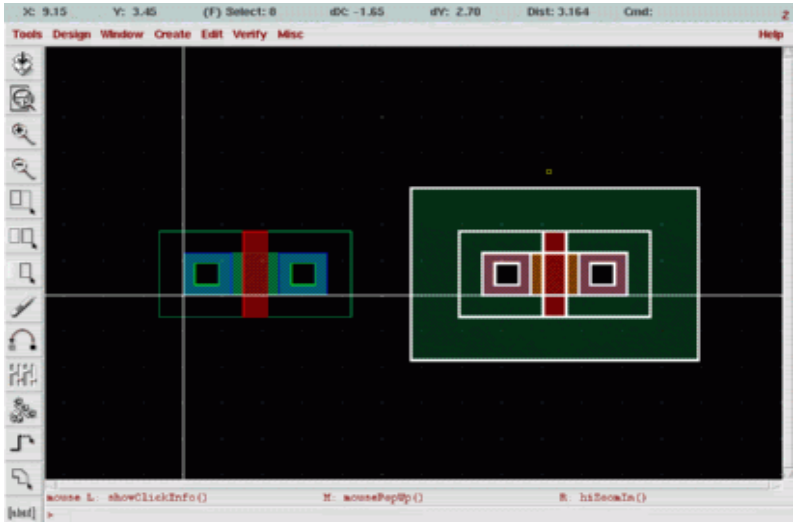
The P-Select Layer

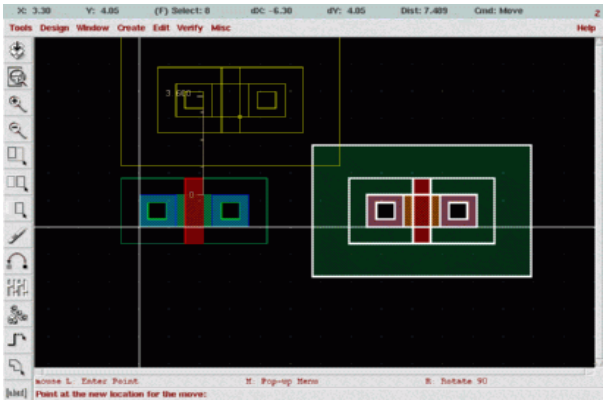


Drawing the N-Well

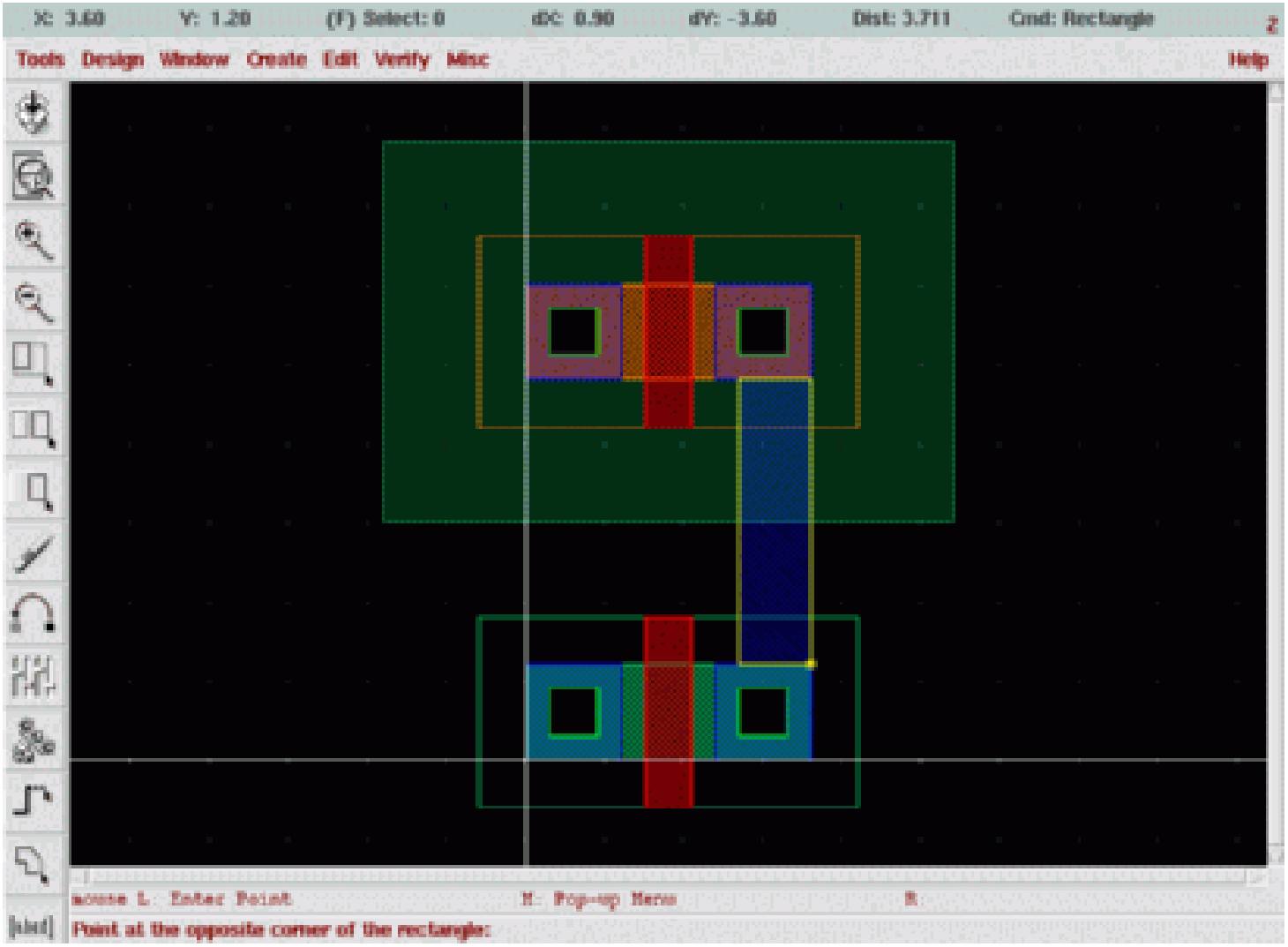


Placing the PMOS and NMOS transistors

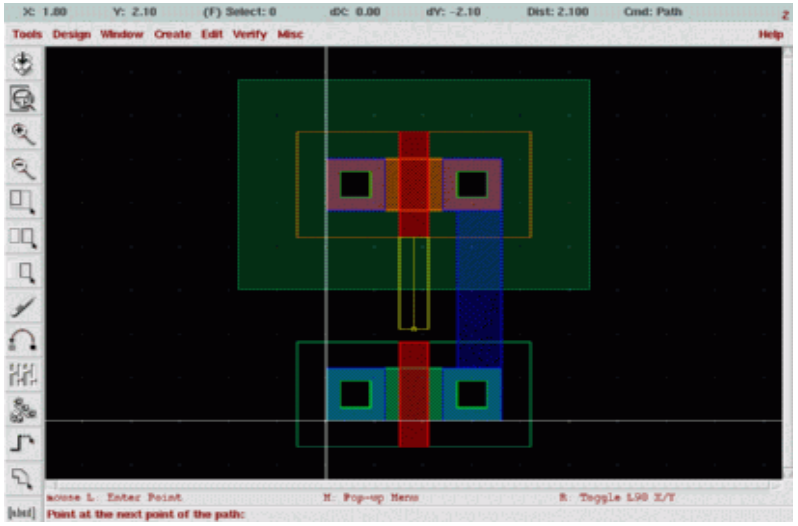


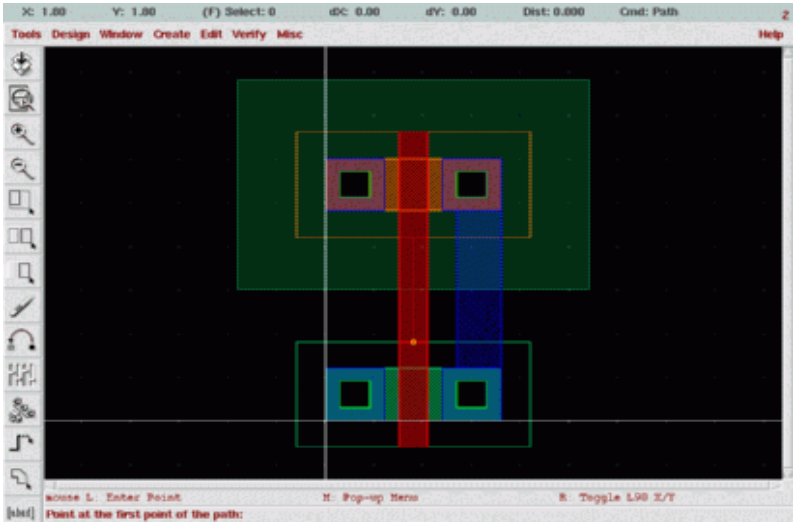


Connecting the Output

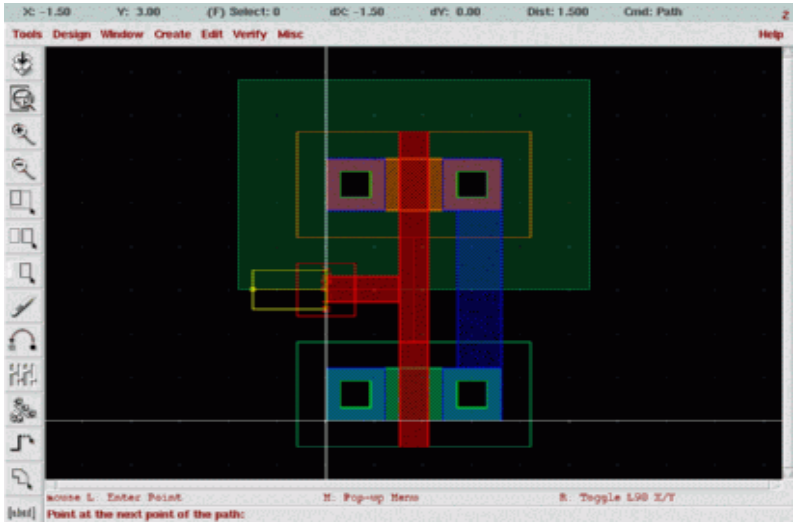


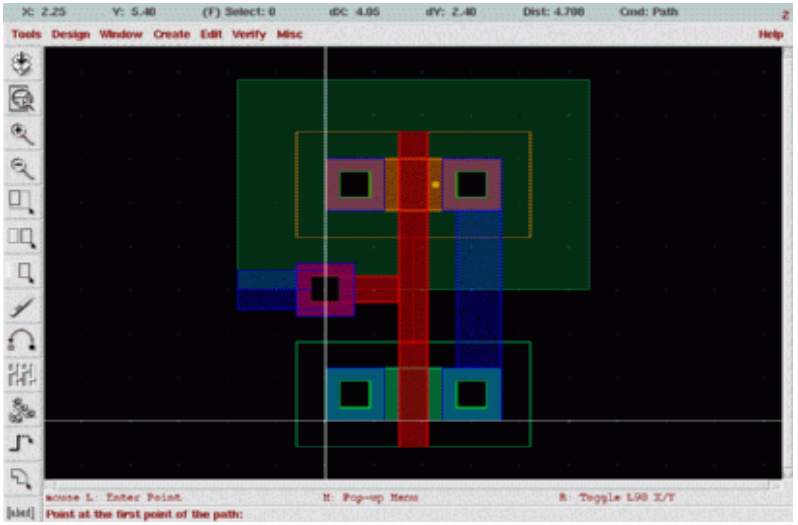
Connecting the Input



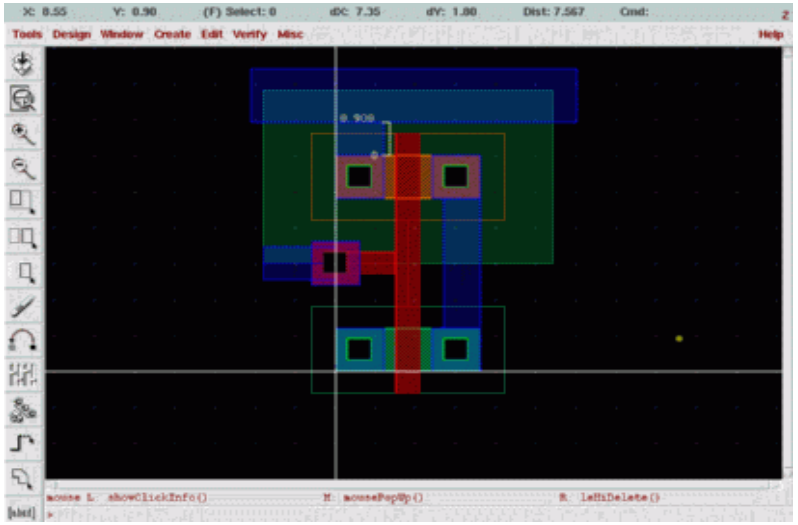


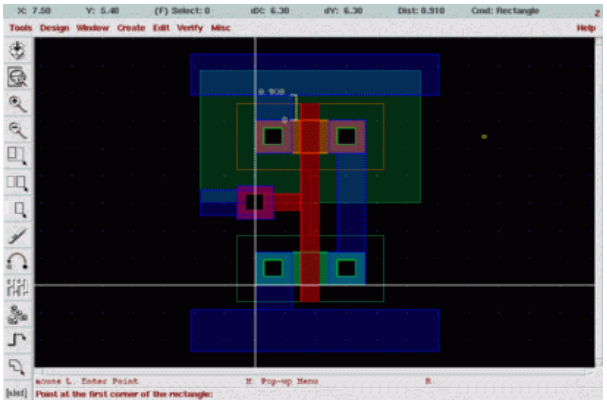
Making a Metal-1 connection for the Input

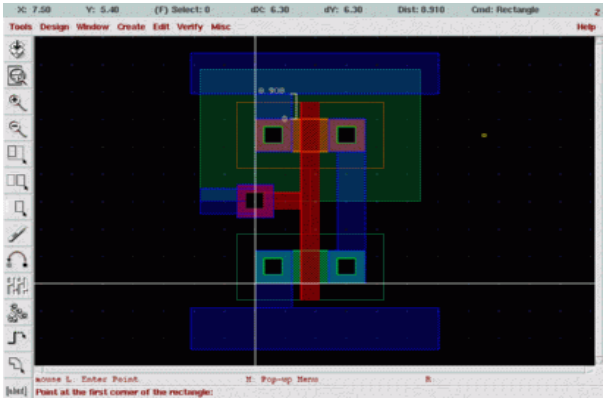




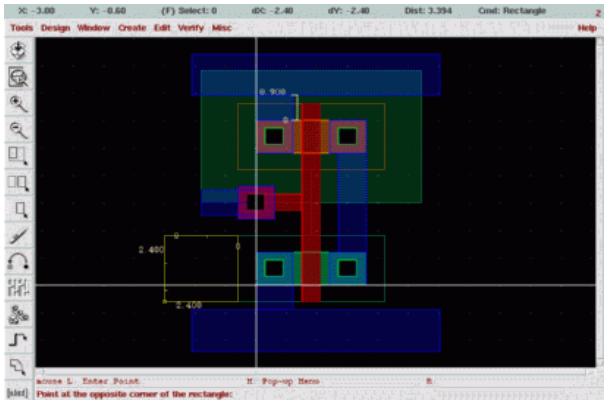
Power Rails

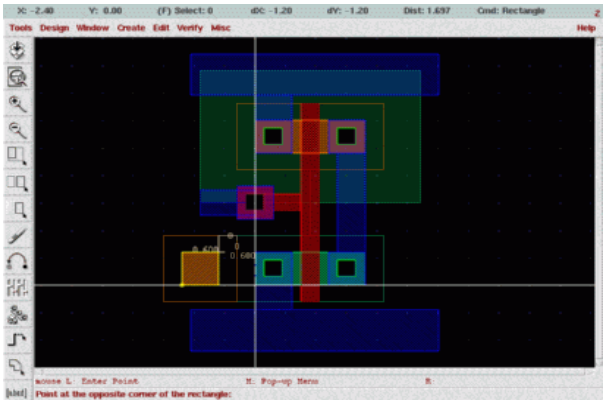


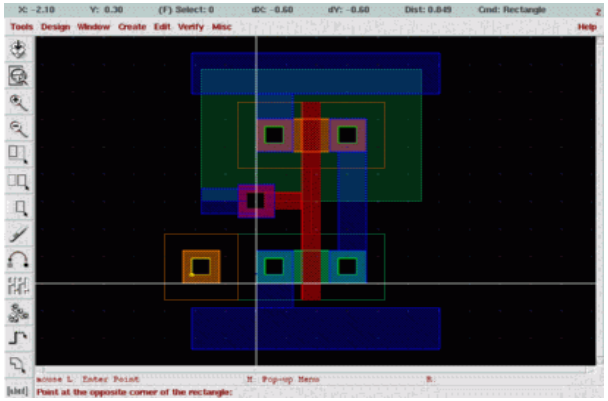


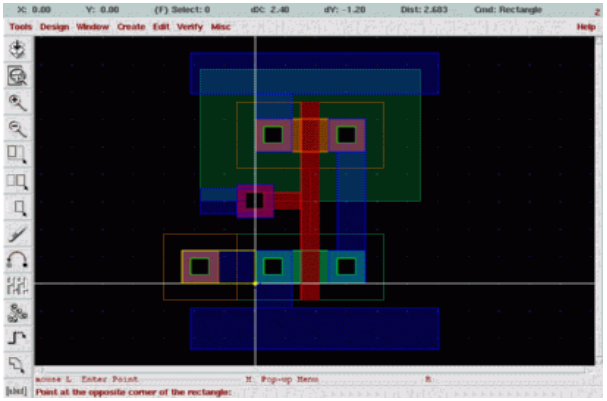


P-Substrate Contact

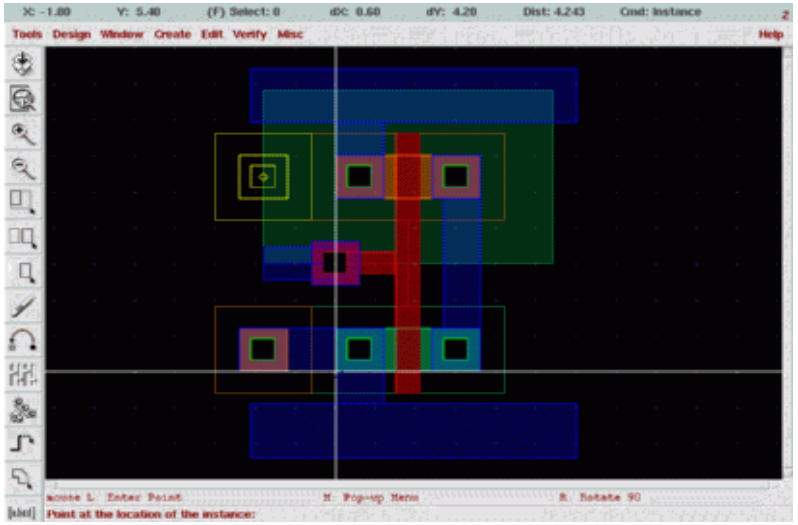


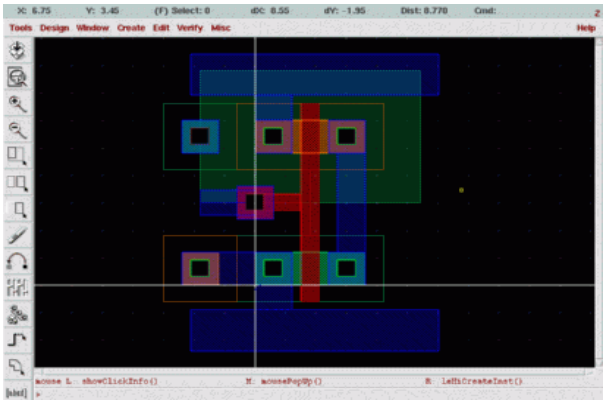


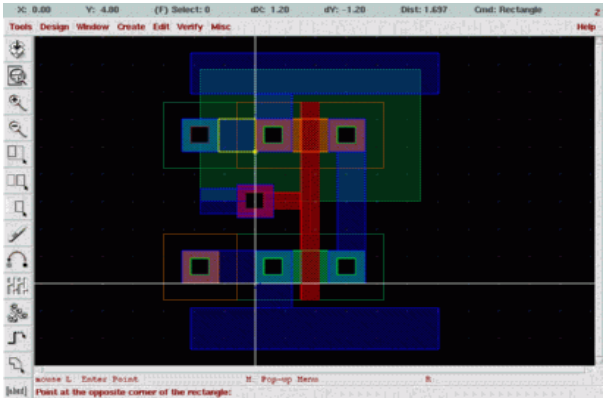




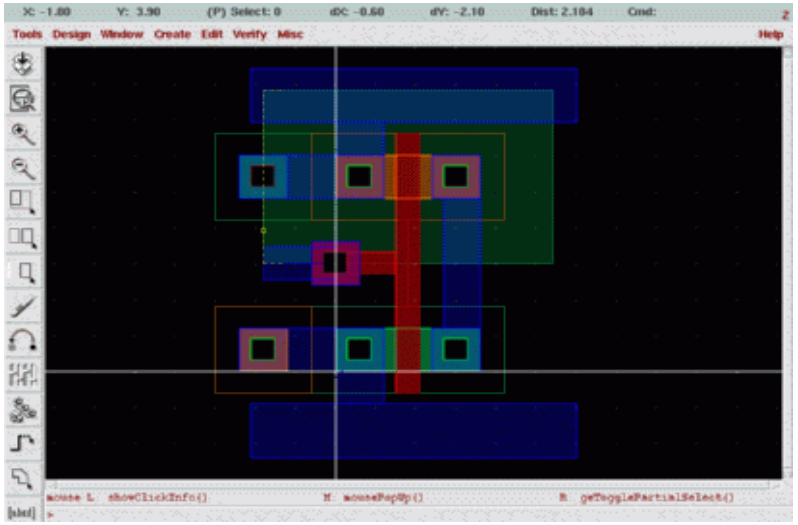
N-Substrate Contact

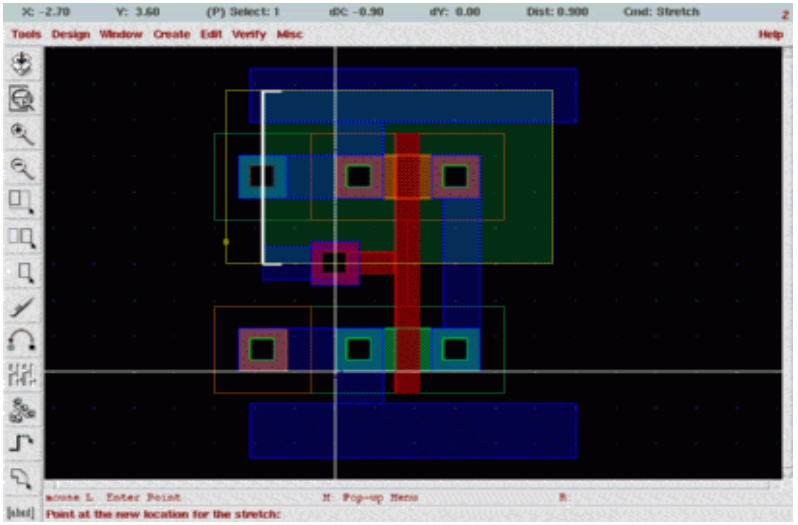




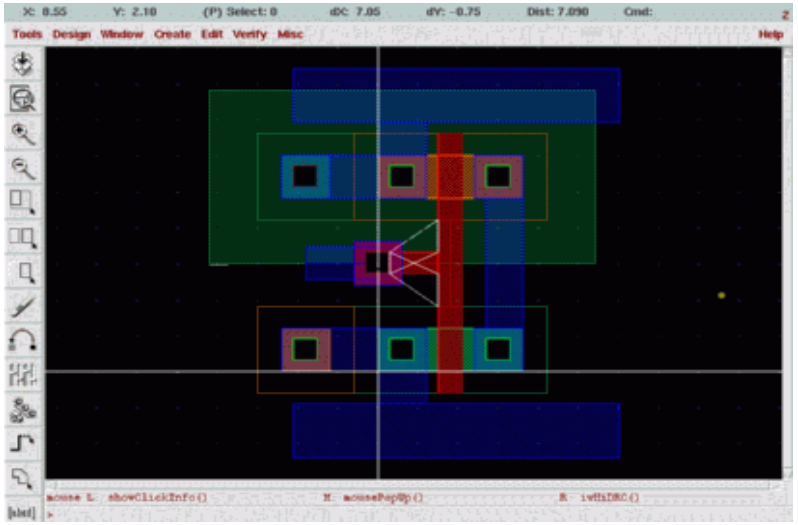


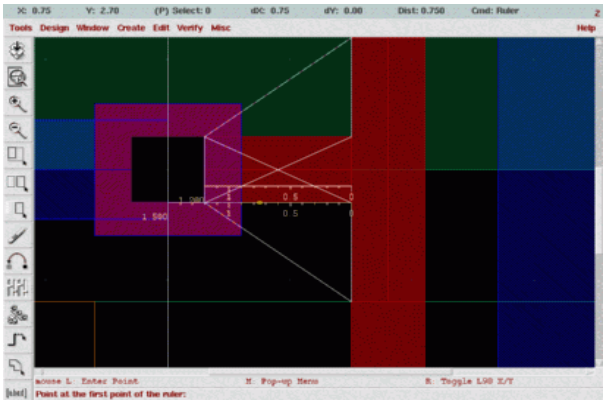
Enclosing the substrate contact

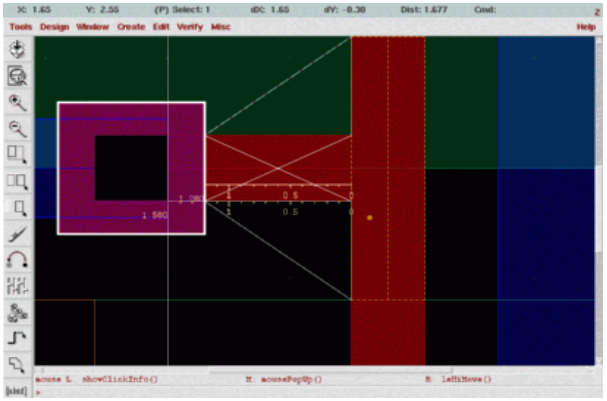




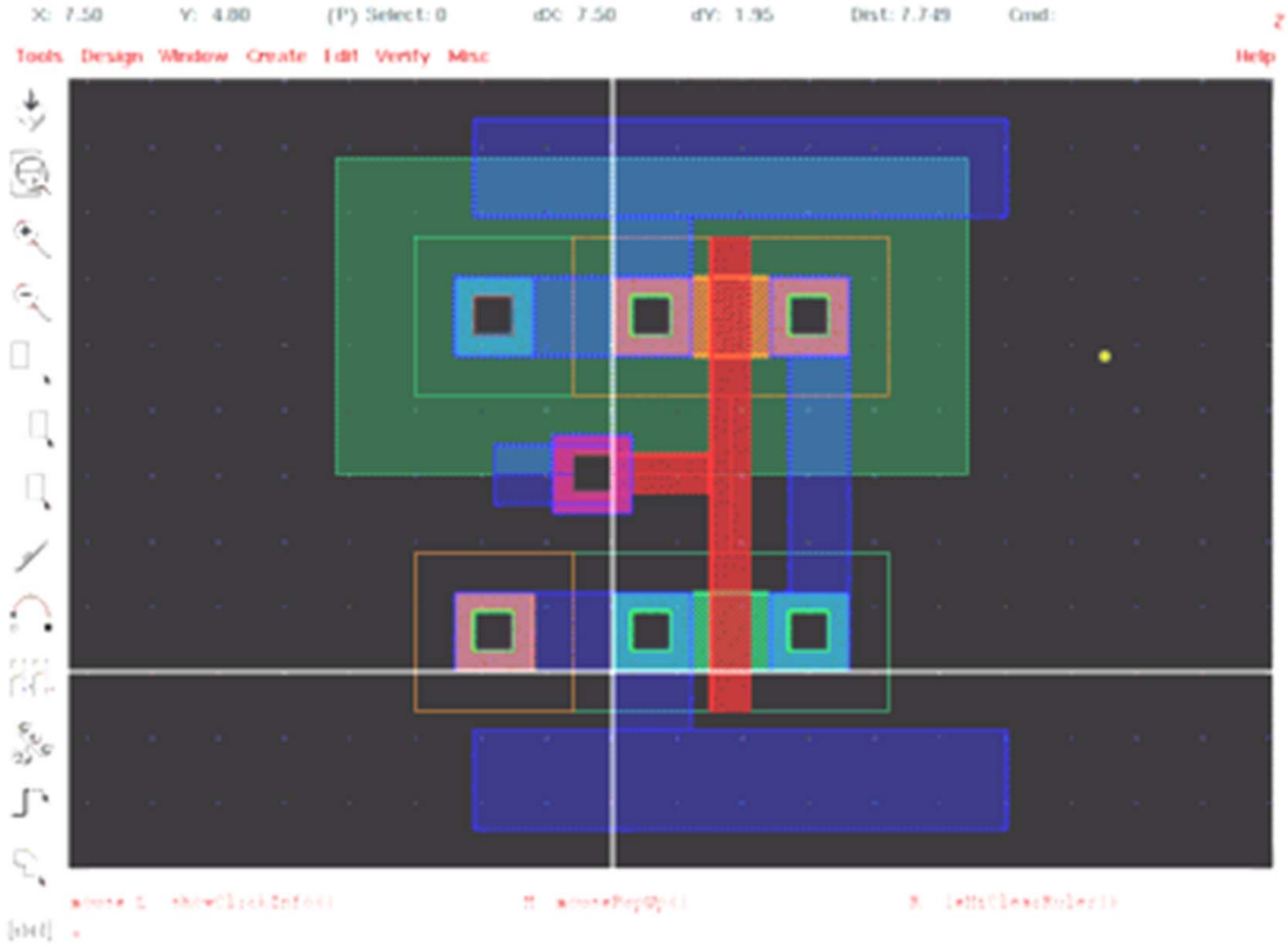
Design Rule Checking







Final Layout



结　　论

- 静态CMOS逻辑电路噪声容限较大
- CMOS电路的特点之一是功耗小，其静态功耗几乎为0
- CMOS反相器为无比反相器
- CMOS反相器的PMOS和NMOS沟道宽的比值大约为2：1(L 相同)时，t_{PLH}和t_{PHL}大致相同，上升时间和下降时间也大致相同
- 为了减小t_{PHL}（或下降时间t_f），可增大NMOS的尺寸
- 为了减小t_{PLH}（或上升时间t_r），可增大PMOS的尺寸

作业

1. 考虑具有如下参数的**CMOS**反相器

$$nMOS \quad V_{TN}=0.6 \quad \mu_n C_{ox}=60\mu A/V^2 \quad (Wn/Ln)=8$$
$$pMOS \quad V_{Tp}=-0.7 \quad \mu_P C_{ox}=25\mu A/V^2 \quad (Wp/Lp)=12$$

求电路的噪声容限以及逻辑阈值.电源电压取**3.3V.**

2. 设计一个**CMOS**反相器:
器件参数同上题,电源电压为**3.3V**,两个晶体管的沟道长度为**Ln=Lp=0.8UM.**
a: 求当电路的逻辑阈值为1.4V时,**Wn/Wp**的值.
b:这个反相器的CMOS制作工艺允许**VTn,VTp**的值在标称值有正负15%的变化.
假定其他参数仍为标称值，求电路的逻辑阈值的上下限.

3. 名词解释: 有比逻辑电路；无比逻辑电路；逻辑门的静态功耗；逻辑门动态功耗；逻辑阈值。

.