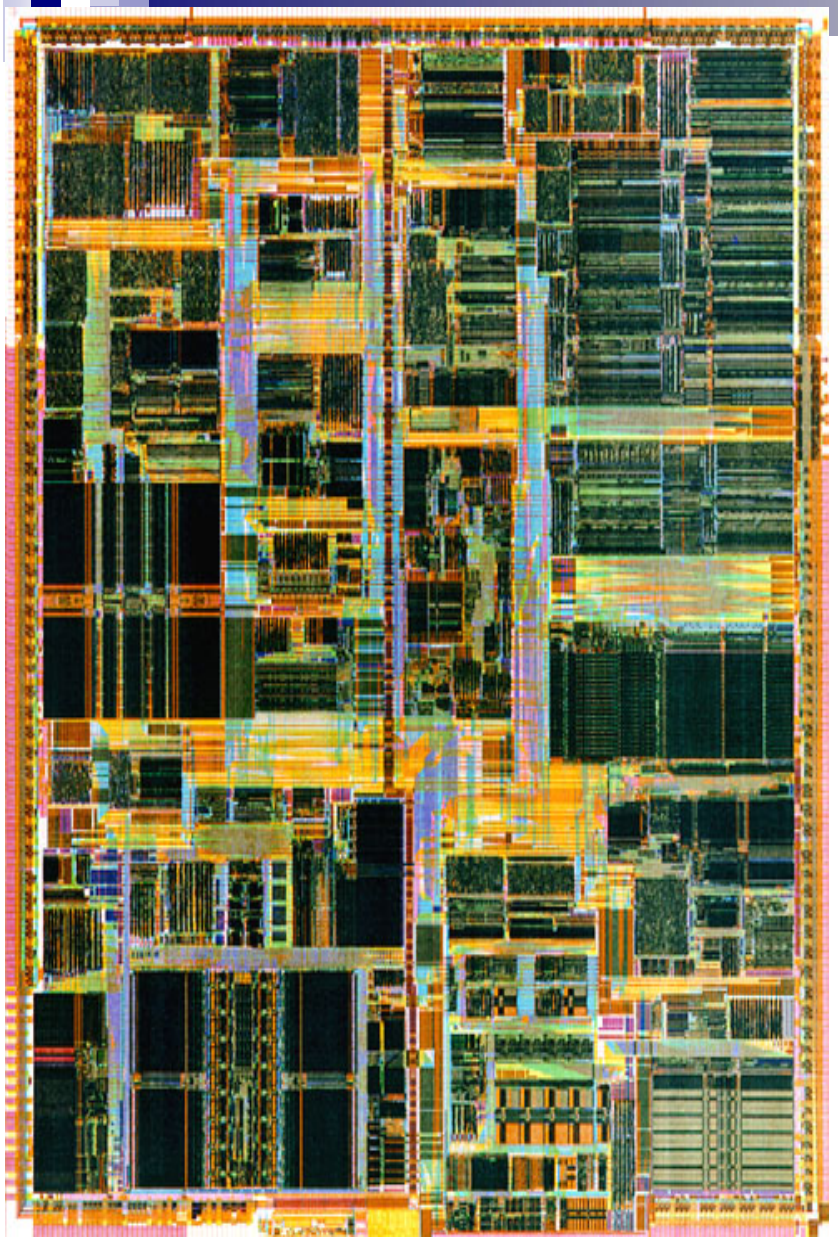


半导体集成电路

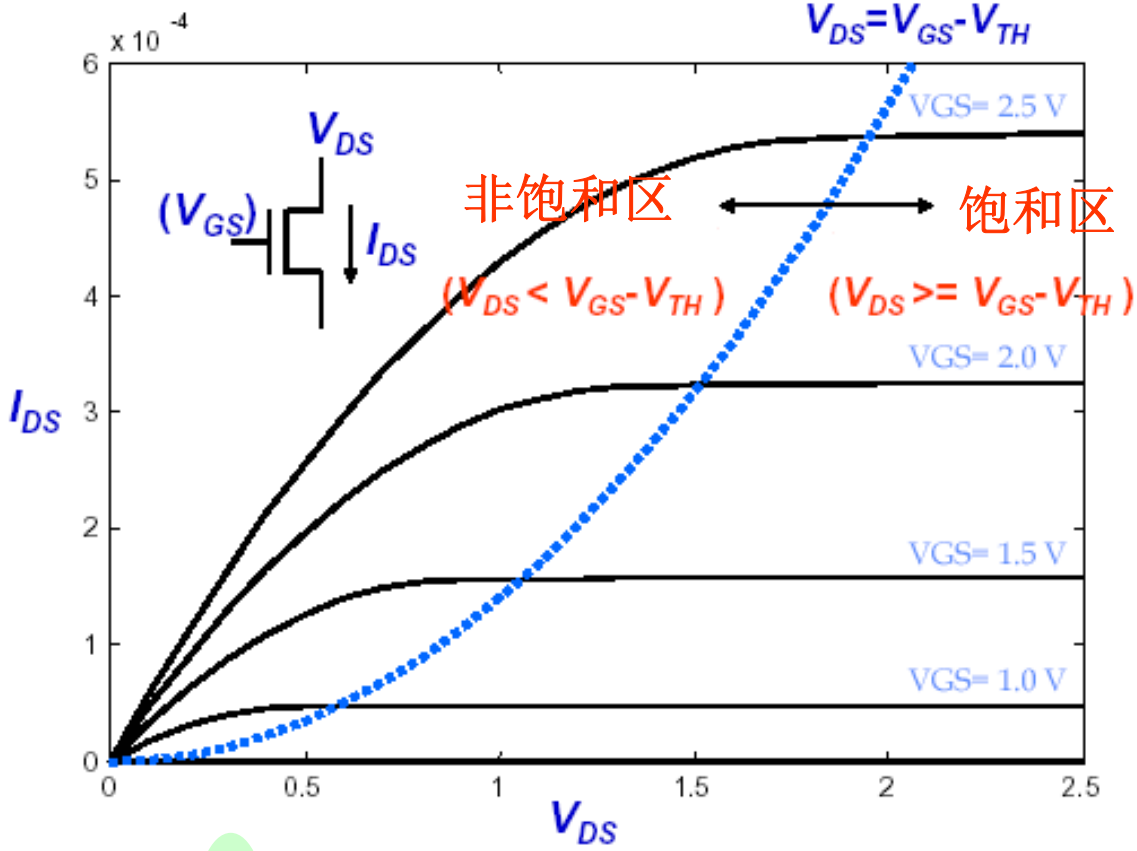
学校：西安理工大学
院系：自动化学院电子工程系
专业：电子、微电
时间：秋季学期

2012/11/27

上节课内容要点

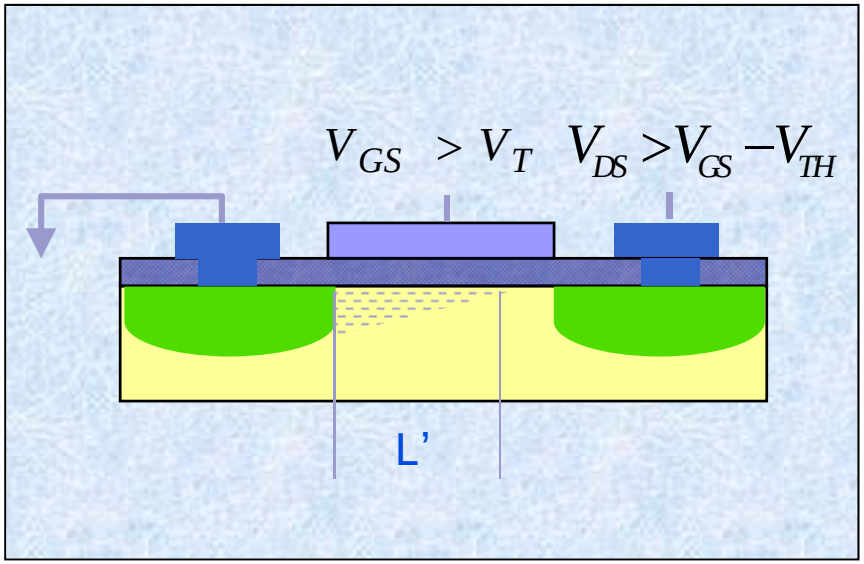
- **MOS晶体管的小尺寸效应**
- **MOS晶体管的电容**
- **MOS晶体管的导通电阻**

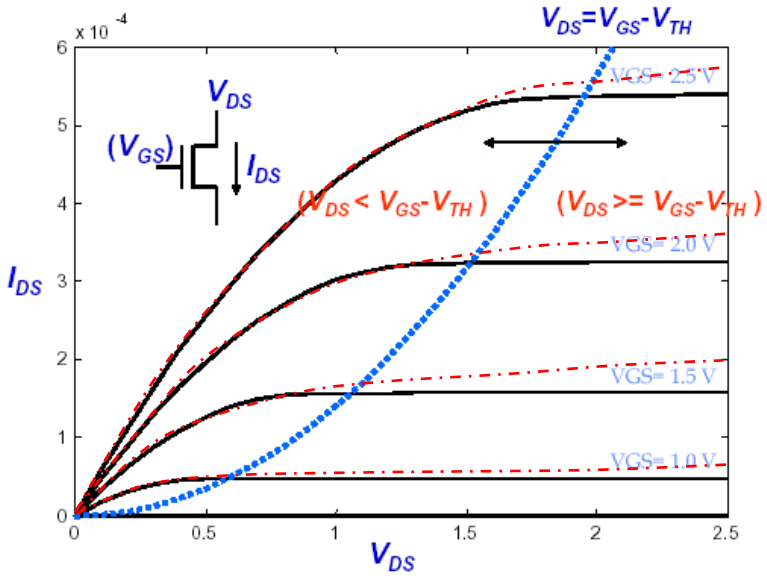
◆基本要求



$$\mathbf{I_D}\begin{cases} I_{DS}=\mu C_{ox}\frac{W}{L}[(V_{GS}-V_{TH})V_{DS}-\frac{1}{2}V_{DS}^{\ 2}] & (\mathbf{0<V_{DS}<V_{GS}-V_{TH}}) \\ I_{DS}=\frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 & (\mathbf{0< V_{GS}-V_{TH} < V_{DS}}) \end{cases}$$

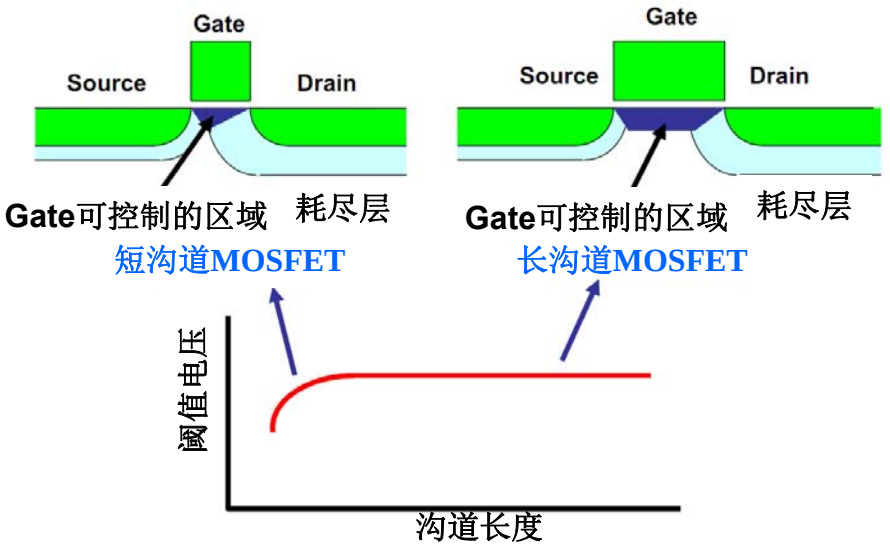
◆沟道长度调制效应



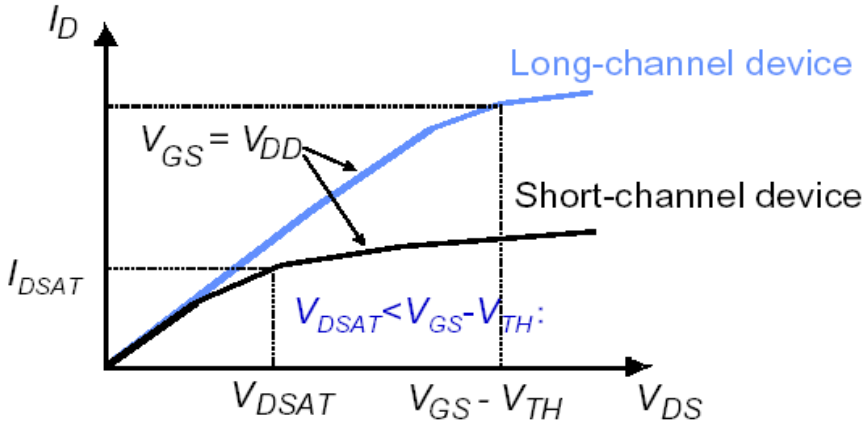


$$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

◆短沟道效应



◆速度早期饱和



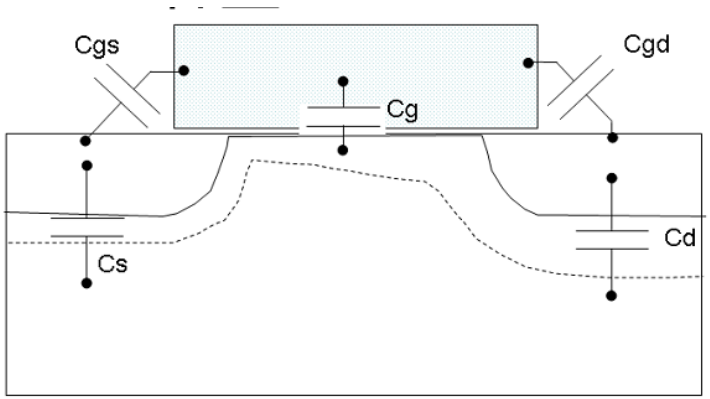
饱和早期开始

短沟道MOSFET的电流方程

$$I_{DS} = K_n' \cdot \frac{W}{L}\left\{(V_{GS} - V_{TH})V_{\min} - \frac{1}{2}V_{\min}^{\ 2}\right\}(1 + \lambda V_{DS})$$

$$V_{\min} = (V_{GS} - V_{TH}, V_{DS}, V_{DSAT})$$

MOS晶体管的电容

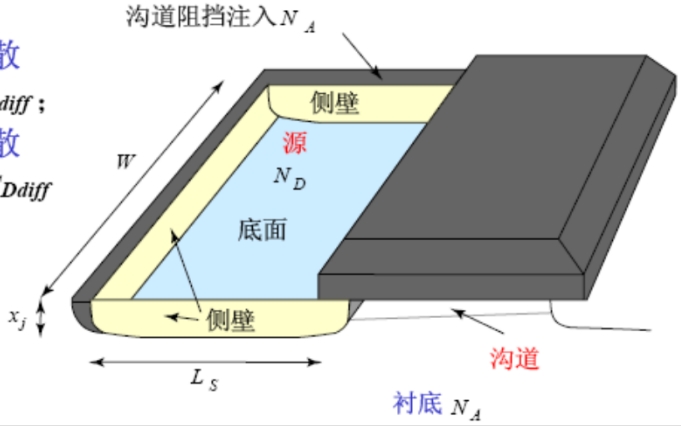


源扩散

$C_{SB} = C_{sdiff}$;

漏扩散

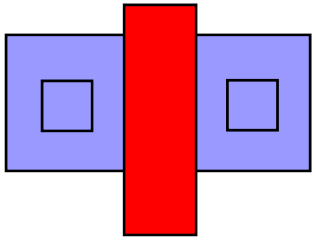
$C_{DB} = C_{Ddiff}$



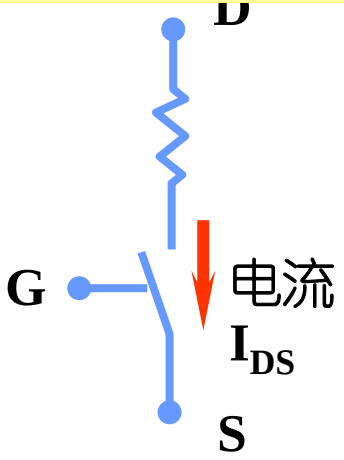
$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

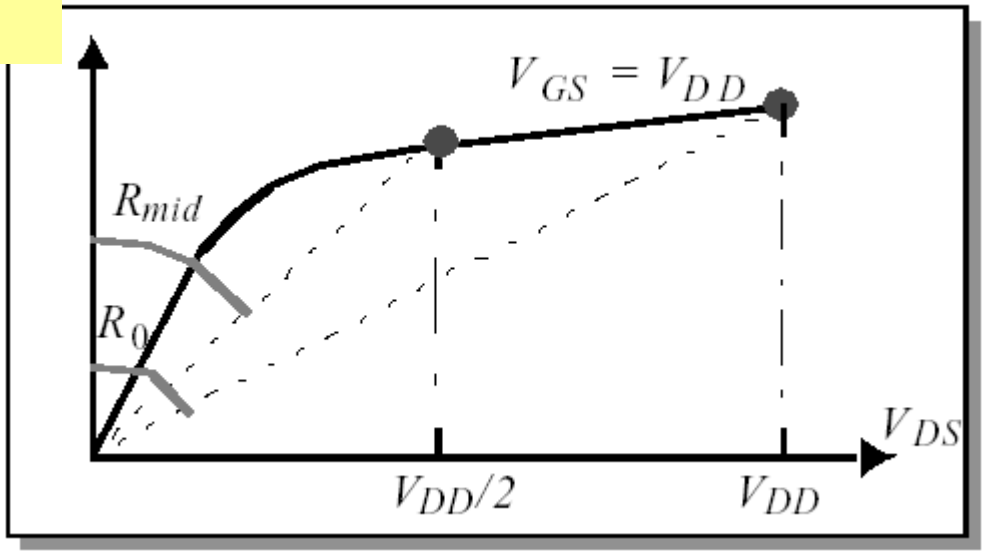
栅极电容作为前一级的负载电容

漏源电容作为自身负载电容



MOS晶体管的电阻



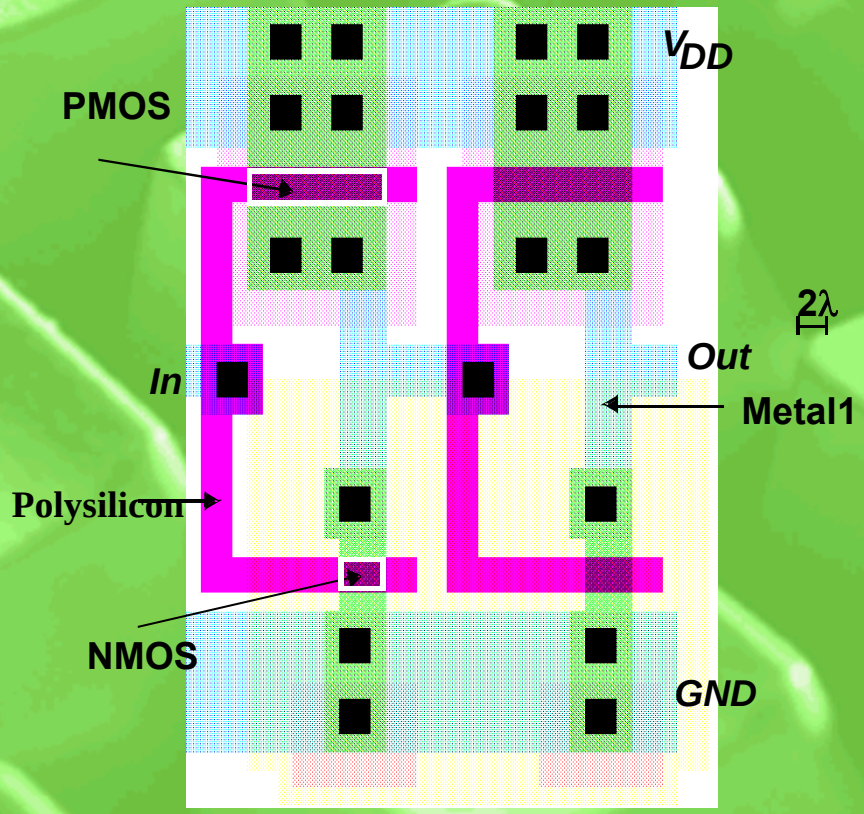


- 导通电阻是一个非线性电阻，与器件的工作状态有关,平均电阻一般取**0.75R_0**
- 在非饱和区，导通电阻近似为线性电阻

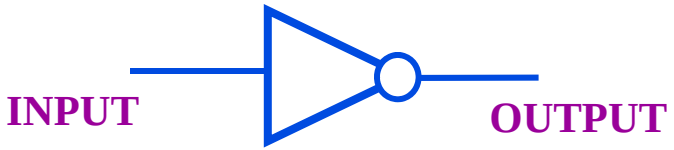
$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})}$$ 即**R_{on}=1/g_m**

- 导通电阻反比于（**W/L)**，**W**每增加一倍，电阻减小一半

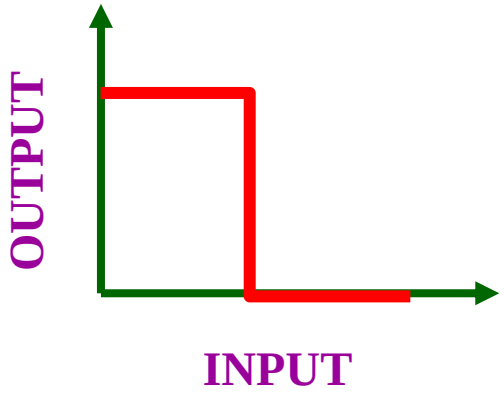
MOS反相器

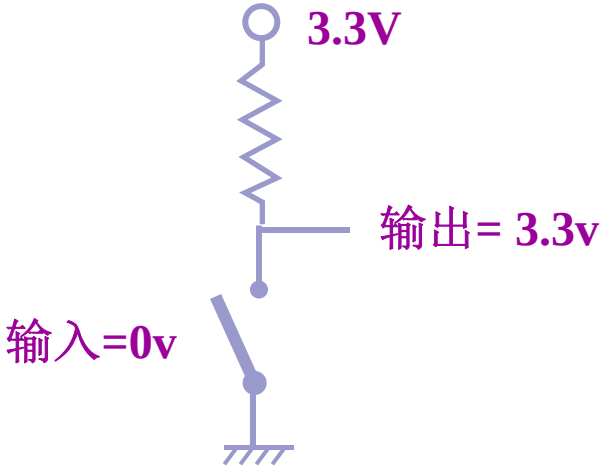


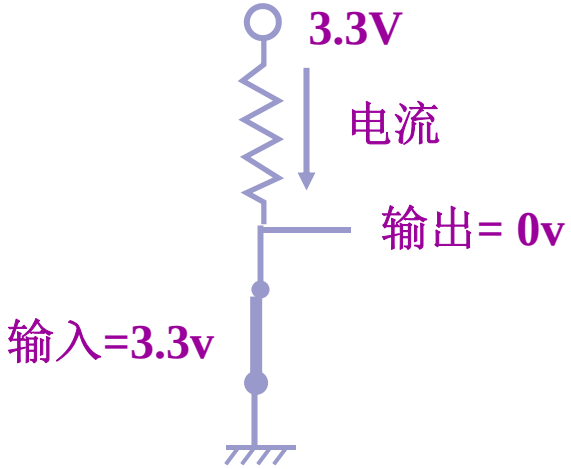
MOS反相器的静态特性



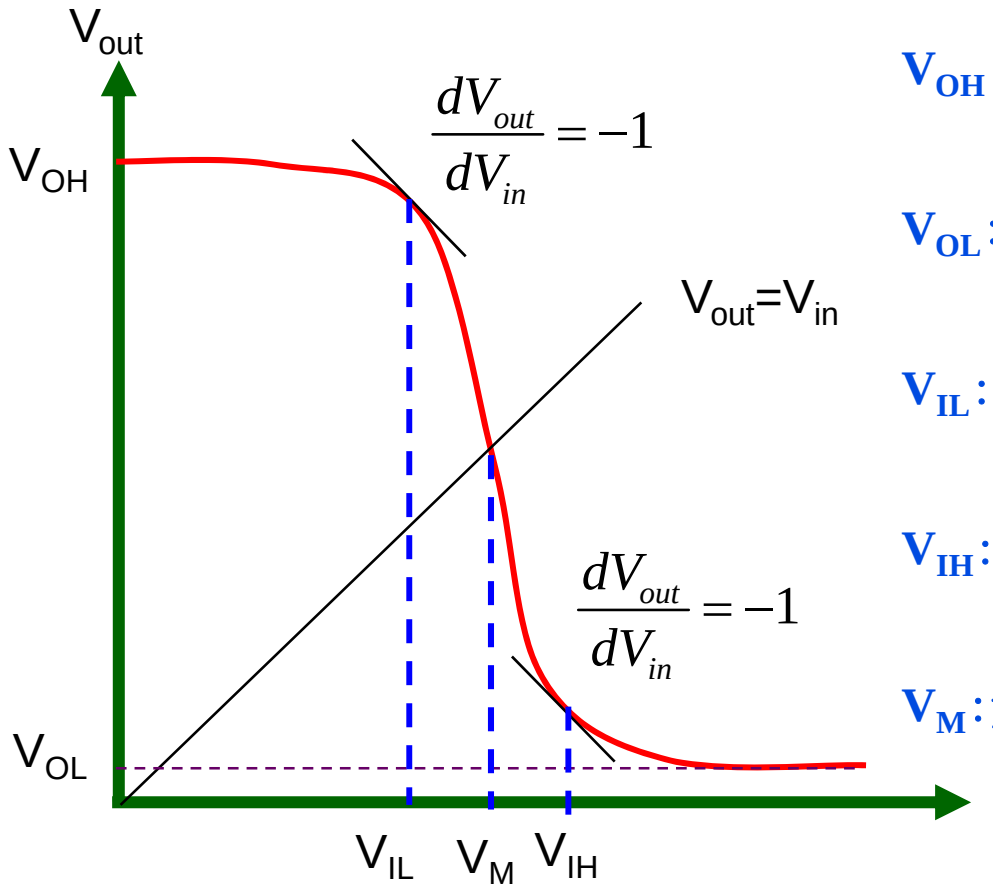
INPUT	OUTPUT
0	1
1	0







MOS反相器的电压传输特性



V_{OH}：输出电平为逻辑”1”时的最大输出电压

V_{OL}：输出电平为逻辑”0”时的最小输出电压

V_{IL}：仍能维持输出为逻辑”1”的最大输入电压

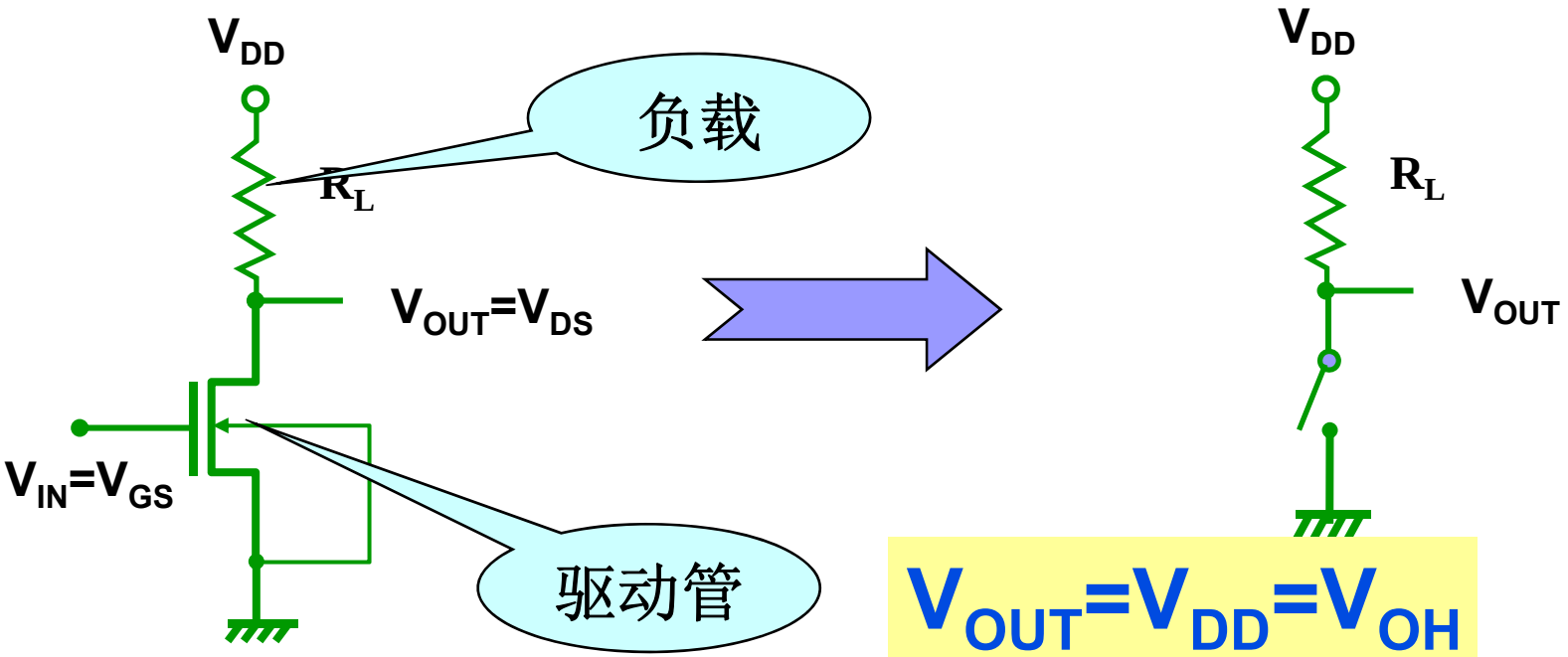
V_{IH}：仍能维持输出为逻辑”0”的最小输入电压

V_M：逻辑阈值，输入等于输出

电阻负载型反相 器

1. $V_{IN}=V_{LOW}\approx 0V$时

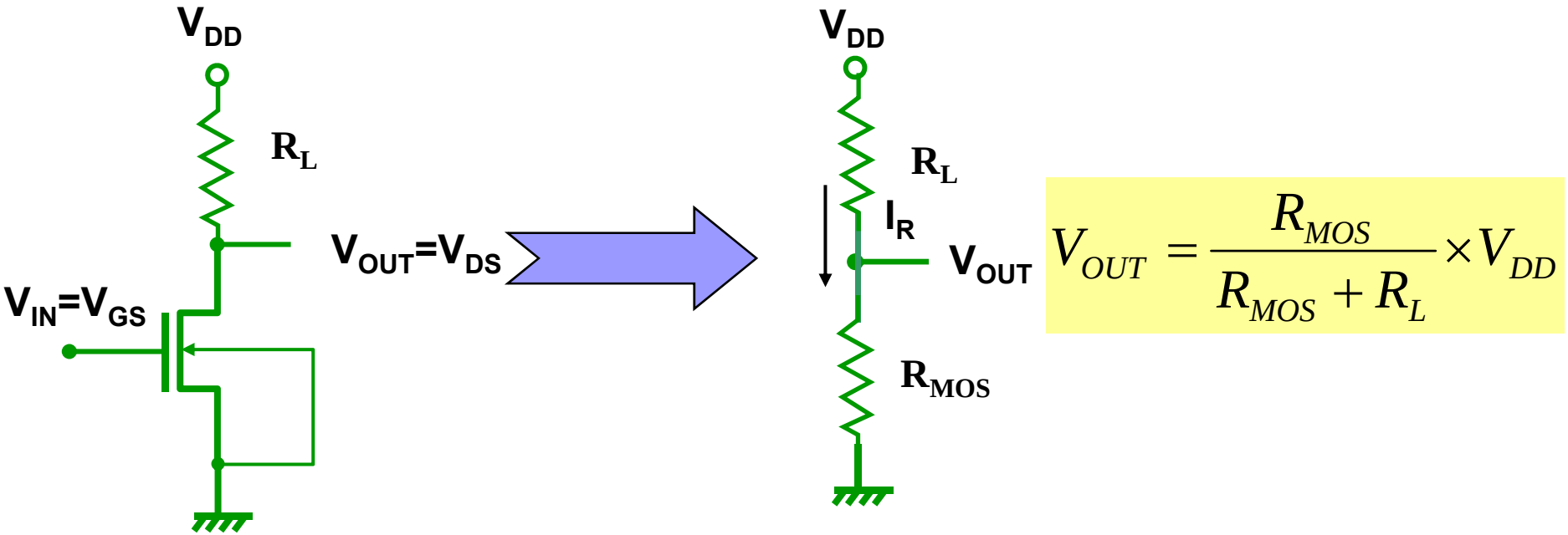
N管截止



$V_{OUT}=V_{DD}=V_{OH}$

2. $V_{IN}=V_{HIGH}\approx V_{DD}$时

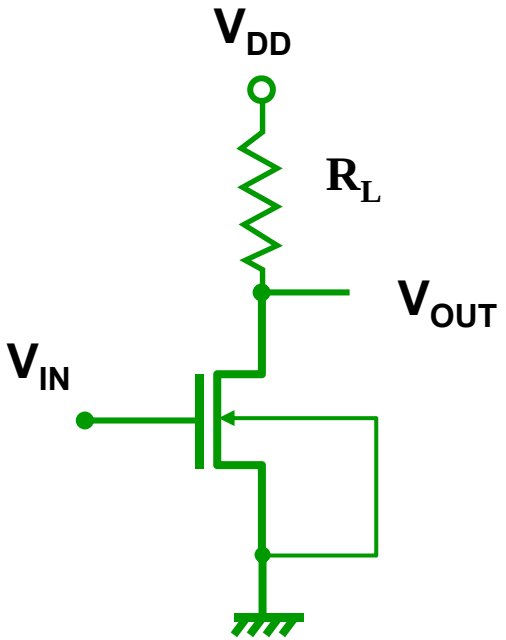
N管导通,可将MOS等效为可变电阻R_{MOS}

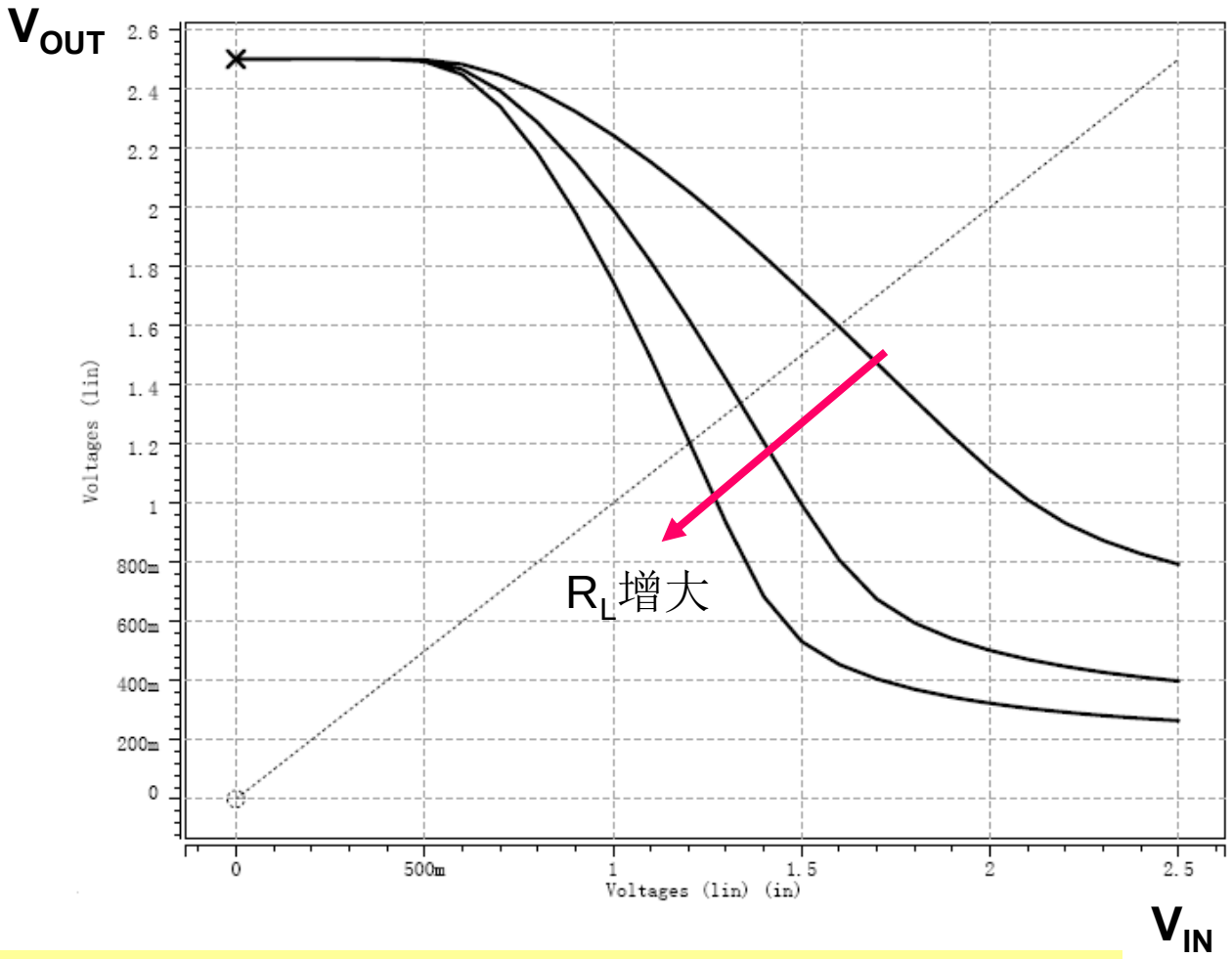


$$V_{OUT}=\frac{R_{MOS}}{R_{MOS}+R_L}\times V_{DD}$$

若$R_L>>R_{MOS}$则$V_{OUT}\approx 0=V_{OL}$

❖ 电阻负载型反相器电压传输特性

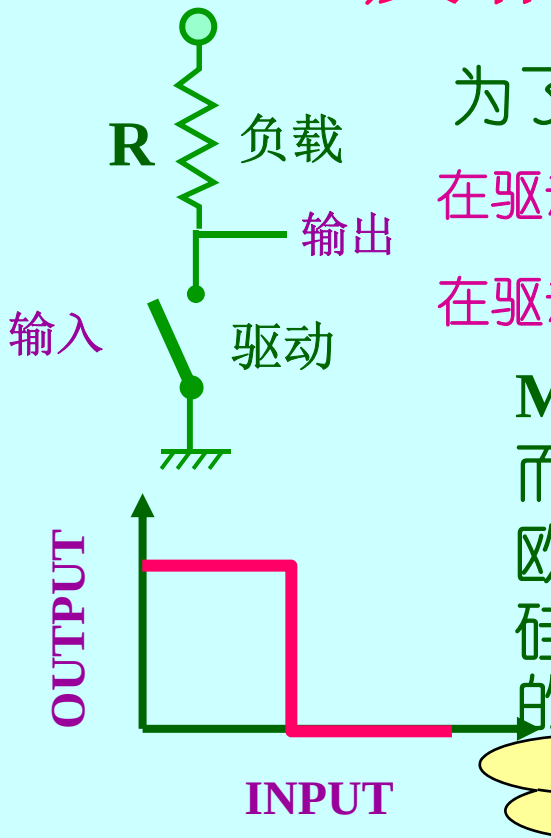




随着R_L的增大，输出低电平降低，逻辑阈值亦减小

反 相 器

反相器中电阻的实现



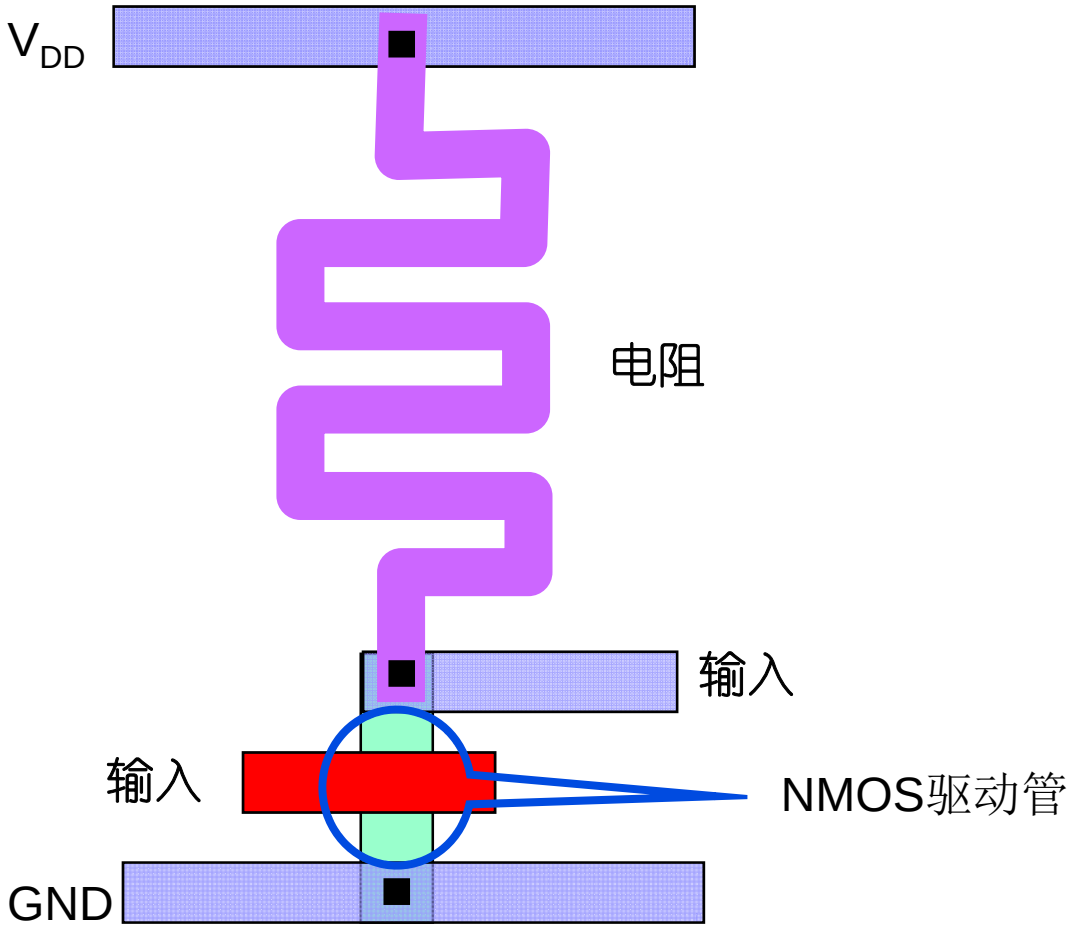
为了使反相器的传输特性好

在驱动管开关断开时，负载电阻相对于开关的电阻足够小

在驱动管开关闭合时，负载电阻相对于开关的电阻足够大

MOS晶体管的导通电阻随管子的尺寸不同而不同，通常在K欧数量级，假设它为3K欧，负载电阻取它的10倍为30K欧，用多晶硅作负载电阻时，如多晶硅的线宽为2微米的

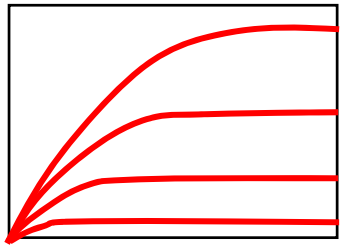
占面积很大，因此通常用MOS管做负载



占用面积过大

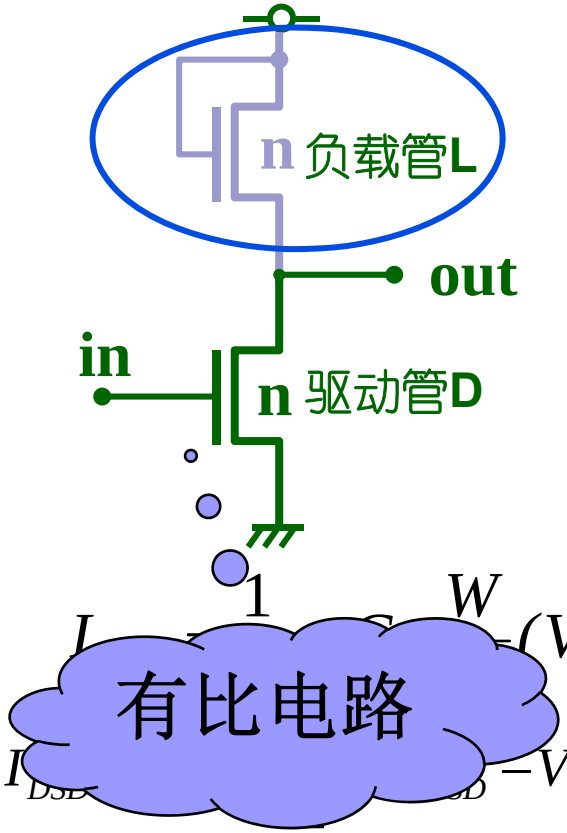
反相器的几种实现方法

1. E/E MOS反相器（介绍饱和MOS负载反相器）



工作在饱和区

$V_{ds}=V_{gs}>V_{gs}-V_{th}$



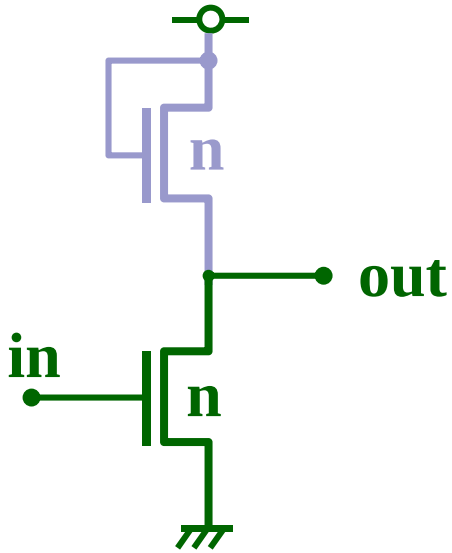
$V_{IN} \rightarrow 0$

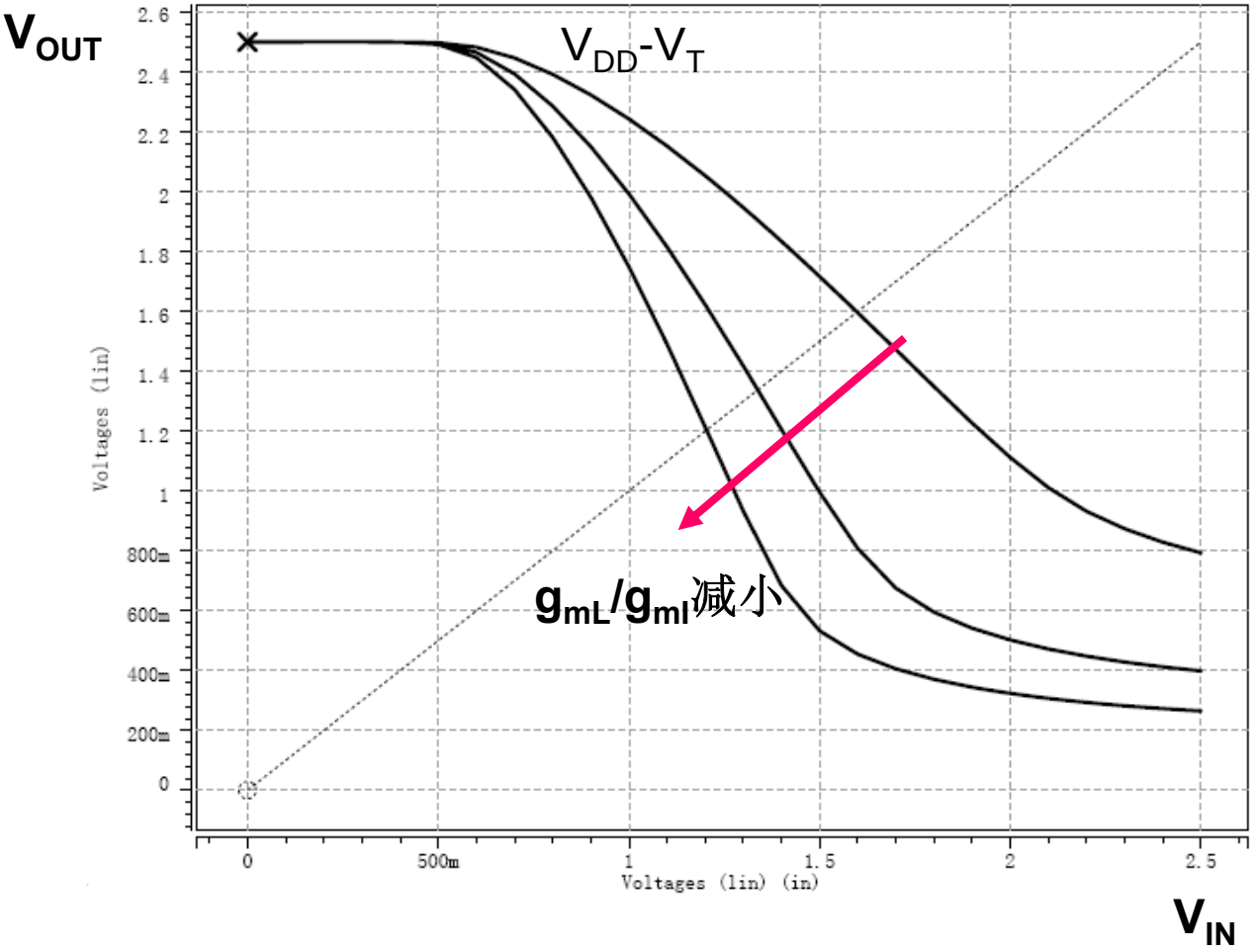
$$V_{OH} = V_{DD} - V_{THL}$$

$$V_{OL} = \frac{1}{2}\frac{g_{mL}}{g_{mD}}(V_{DD} - V_{THL})$$

为使V_{OL}接近0，要求$g_{mL} << g_{mD}$

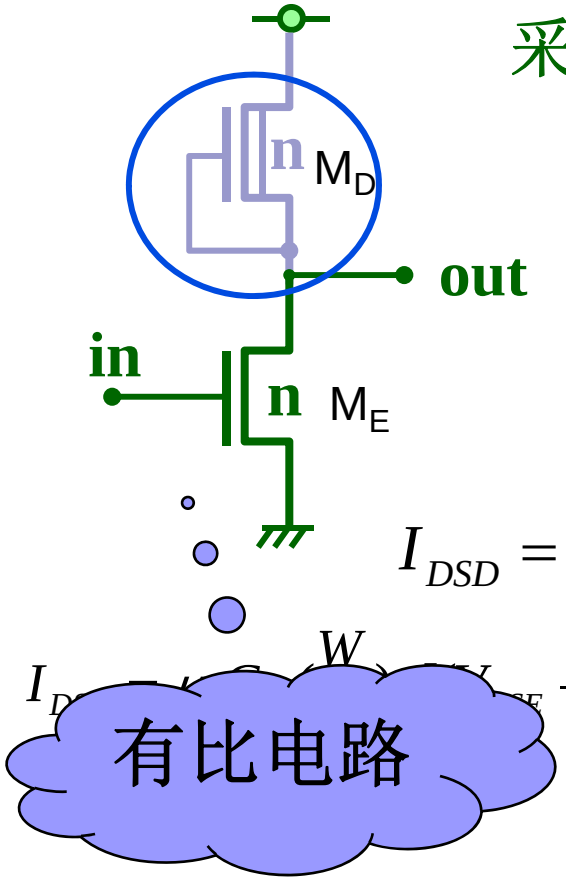
❖ E/E MOS反相器电压传输特性





反相器的几种实现方法

2. E/D MOS反相器



采用耗尽型，$V_{GS}=0$时,一直工作处于导通状态

$V_{IN} \rightarrow 0$ 驱 $V_{OH} \approx V_{DD}$ DD

$$V_{OL} \approx \frac{V_{TD}^{\ 2}}{2K_R(V_{DD}-V_{TE})}$$

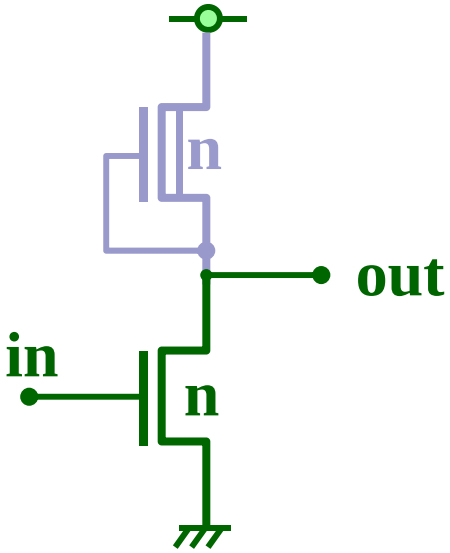
饱和导通

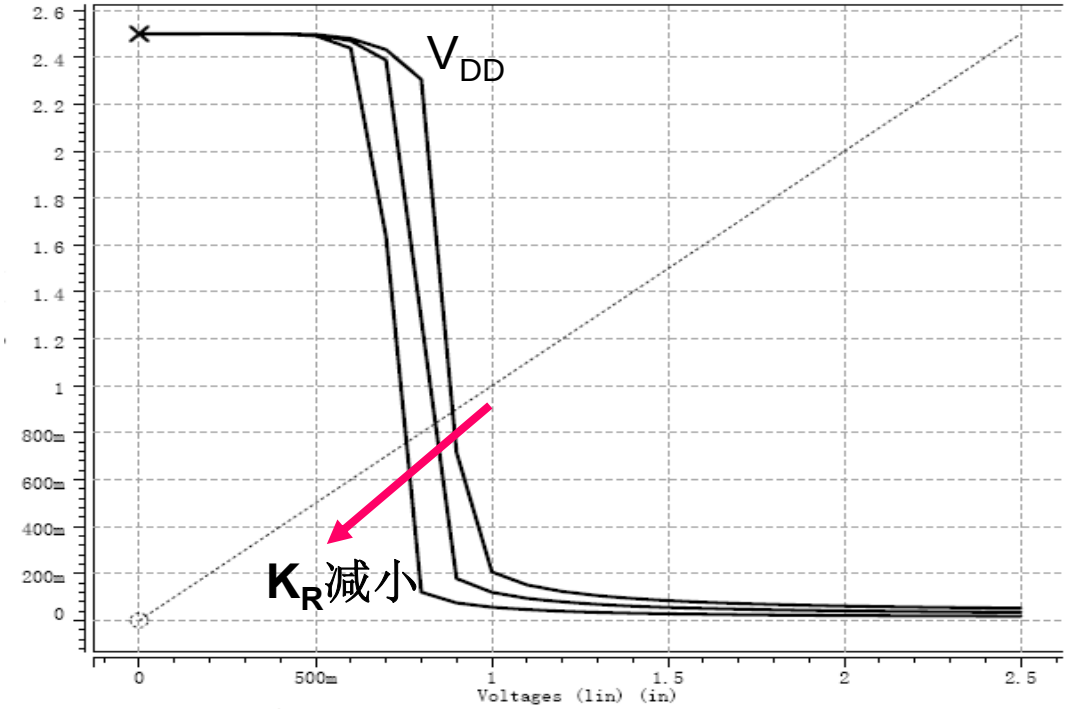
$$I_{DSD} = -$$

$$I_{D} = K_{x}(\frac{W}{L})_{I}[(V_{DD}-V_{TE})V_{OUT}-\frac{1}{2}V_{OUT}^{\ 2}]$$

$$K_R = \frac{\mu_n C_{ox}(\frac{W}{L})_E}{\mu_n C_{ox}(\frac{W}{L})_D}$$

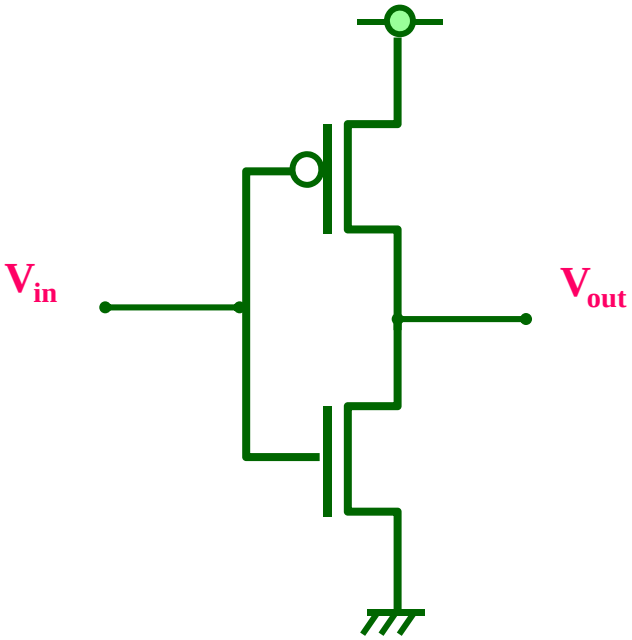
❖ E/D MOS反相器电压传输特性





反相器的几种实现方法

3. CMOS反相器



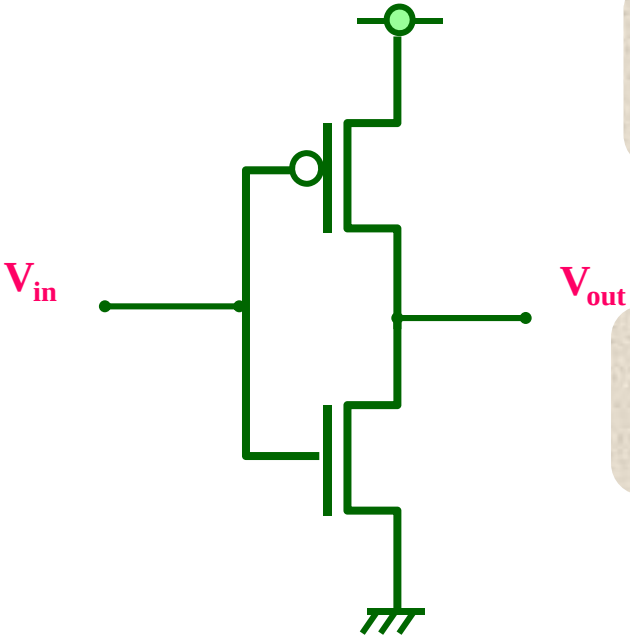
由PMOS和NMOS
所组成的互补型电路叫做
CMOS

C：complementary

CMOS电路的特点：低功耗

CMOS已成为现代集成电路特别是数字电路的主流

❖ CMOS反相器工作原理



当输入电压V_{in}为高电平时，PMOS截止，NMOS导通，$V_{out}=0$

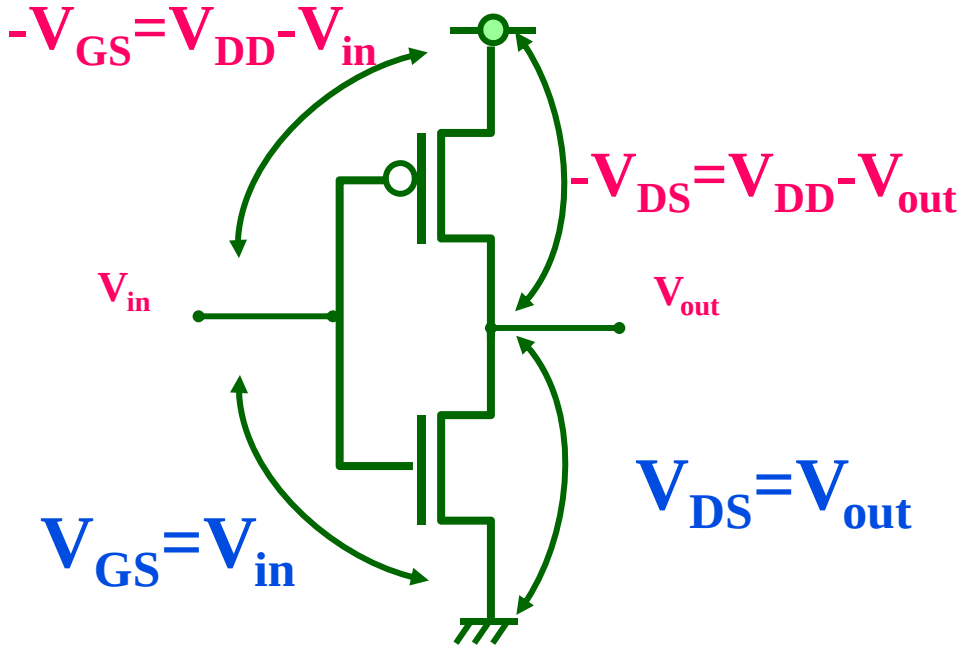
$V_{OL}=0$

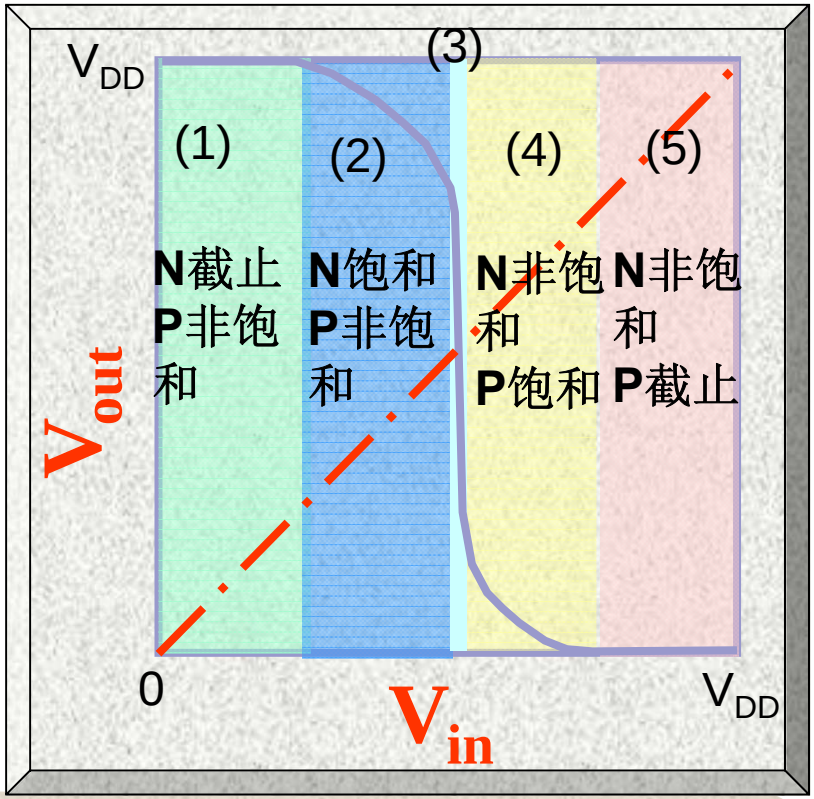
当输入电压V_{in}为低电平时，PMOS导通，NMOS截止，$V_{out}=V_{DD}$

$V_{OH}=V_{DD}$

在输入为0或1（V_{DD})时，两个MOS管中总是一个截止一个导通，因此没有从V_{DD}到V_{SS}的直流通路，也没有电流流入栅极，因此其静态电流和功耗几乎为0。这是CMOS电路低功耗的主要原因。CMOS电路的最大特点之一是低功耗。

CMOS反相器的传输特性





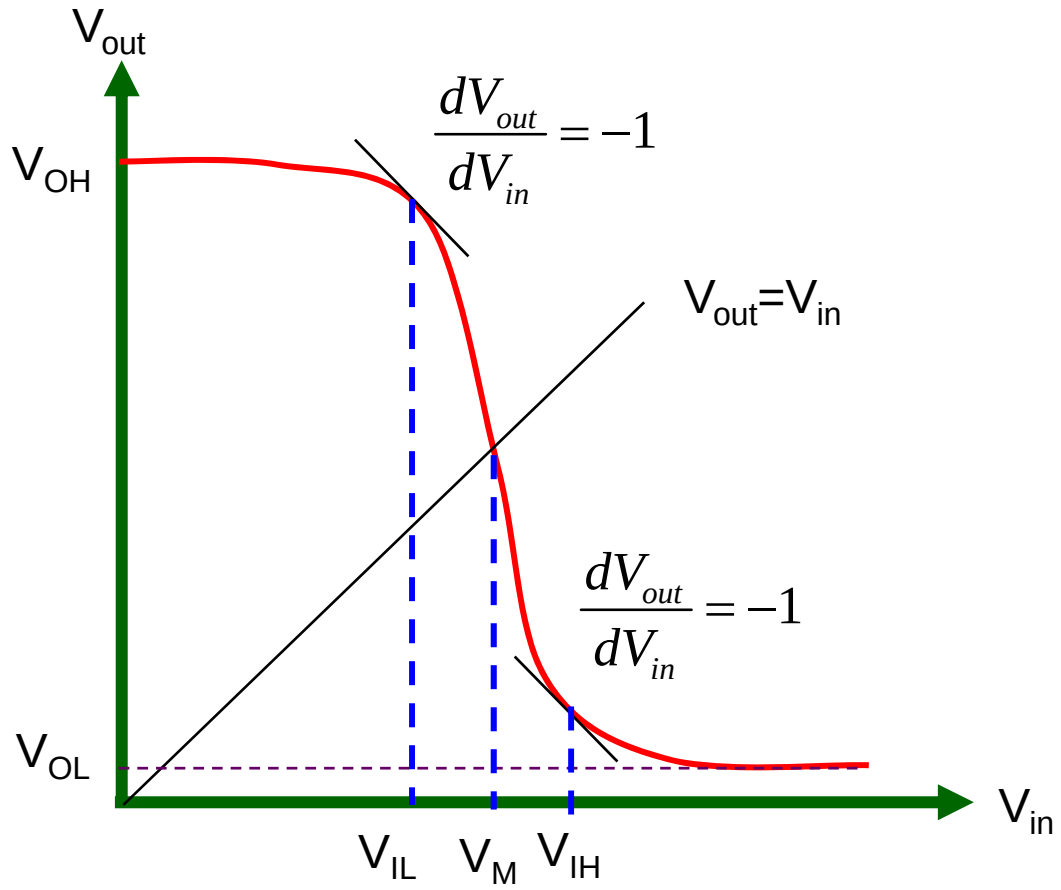
NMOS

$V_{in}<V_{tn}$	截止
$V_{in}-V_{tn}<V_{out}$	饱和
$V_{in}-V_{tn}>V_{out}$	非饱和

PMOS

$(V_{DD}-V_{in}) <-V_{tp}$	截止
$(V_{DD}-V_{in}) +V_{tp}> V_{DD} -Vout$	非饱和
$(V_{DD}-V_{in}) +V_{tp}< V_{DD} -Vout$	饱和

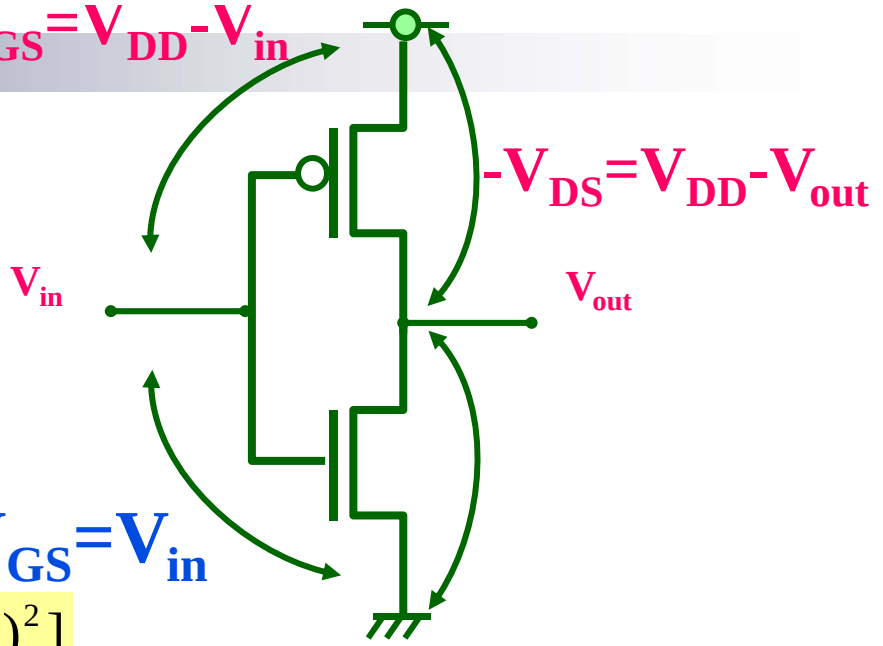
CMOS反相器的几个重要参数



1. V_{IL}的计算

$V_{IN}=V_{IL}$ ⇒ $\dfrac{dV_{out}}{dV_{in}}=-1$

N管工作在饱和区,P管工作在线性区



$$K_P[2(V_{DD}-V_{in}-|V_{TP}|)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2] = K_N(V_{in}-V_{TN})^2 \quad (1)$$

对V_{in}求导，得

$$2K_N(V_{in}-V_{TN}) = 2K_P[(V_{DD}-V_{in}-|V_{TP}|)(-\frac{dV_{out}}{dV_{in}})+$$

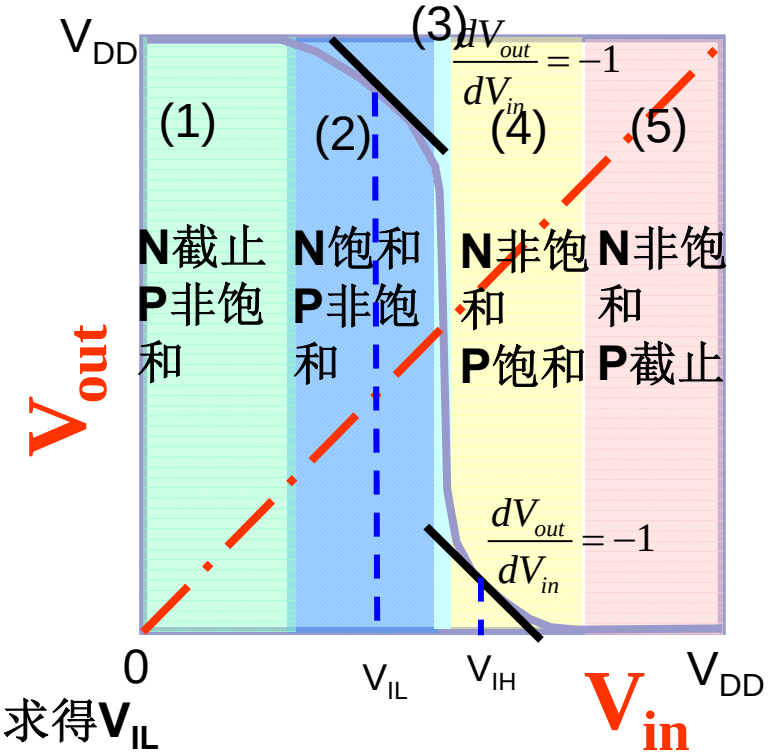
$$(V_{DD}-V_{out})(-1)-(V_{DD}-V_{out})(-\frac{dV_{out}}{dV_{in}})]$$

令 $\dfrac{dV_{out}}{dV_{in}}=-1$，且$V_{in}=V_{IL}$,得

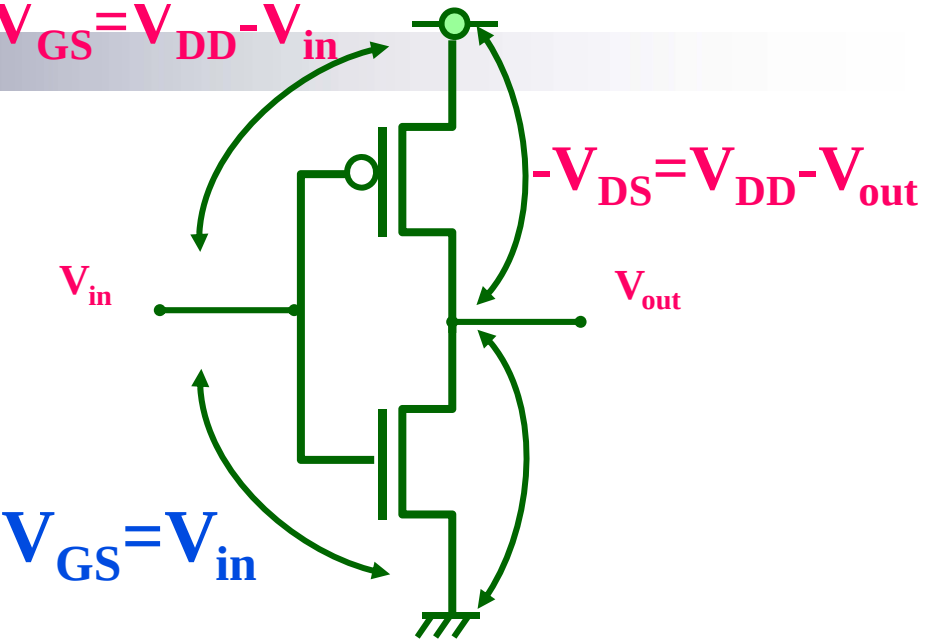
$$K_R=\frac{K_N}{K_P}$$

$$V_{IL}=\frac{2V_{out}+V_{TP}-V_{DD}+k_RV_{TN}}{1+k_R} \quad (2)$$

由（1）（2）式联立可求得V_{IL}



2. V_{IH}的计算



$V_{IN}=V_{IH} \Rightarrow \dfrac{dV_{out}}{dV_{in}}=-1$

N管工作在线性区,P管工作在饱和区

$$K_N[2(V_{in}-V_{TN})V_{out}-V_{out}^{\ 2}] = K_P(V_{DD}-V_{in}-|V_{TP}|)^2 \quad (1)$$

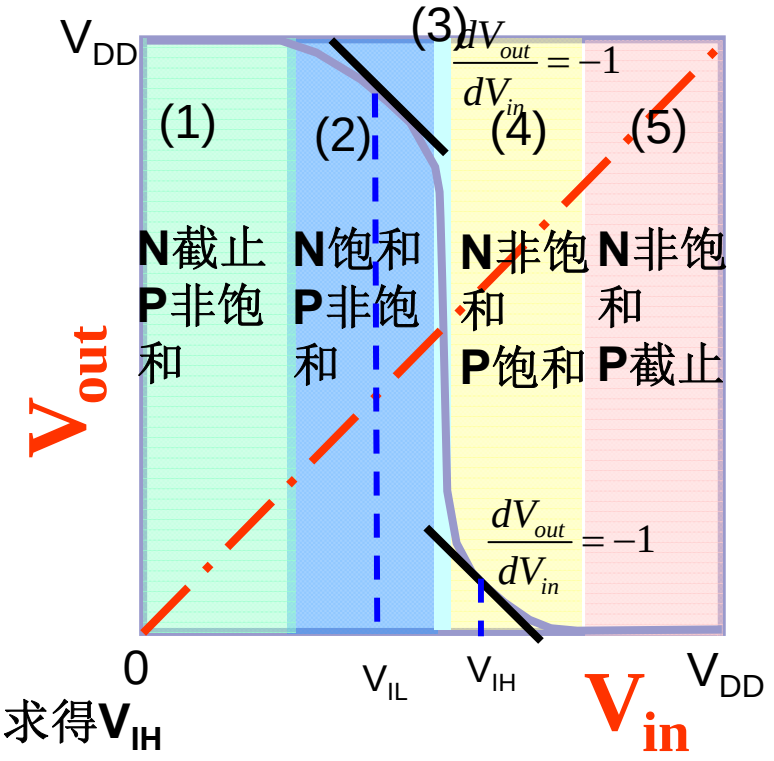
对V_{in}求导，得

$$2K_N[(V_{in}-V_{TN})(\frac{dV_{out}}{dV_{in}})+V_{out}-V_{out}\frac{dV_{out}}{dV_{in}}] = 2K_P(V_{DD}-V_{in}-|V_{TP}|)$$

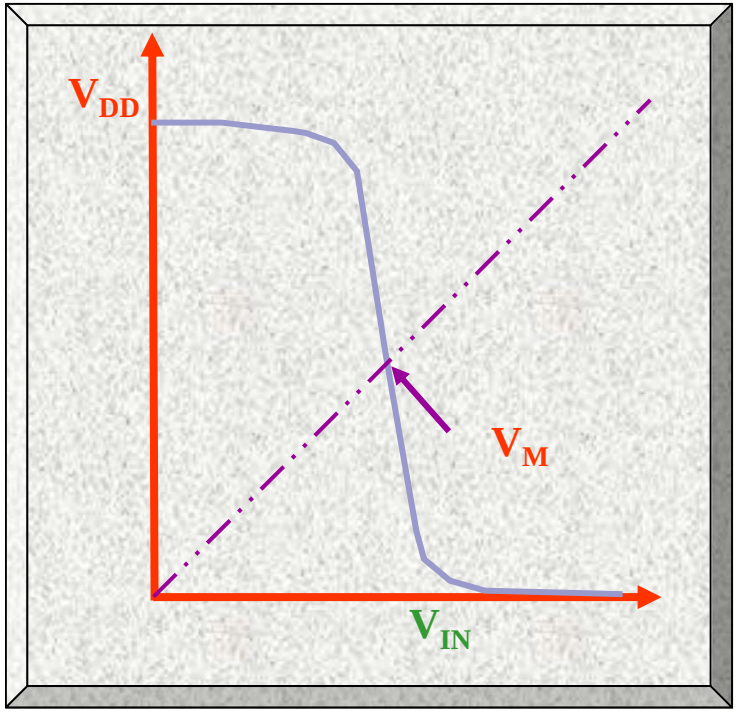
令 $\dfrac{dV_{out}}{dV_{in}}=-1$，且$V_{in}=V_{IH}$,得

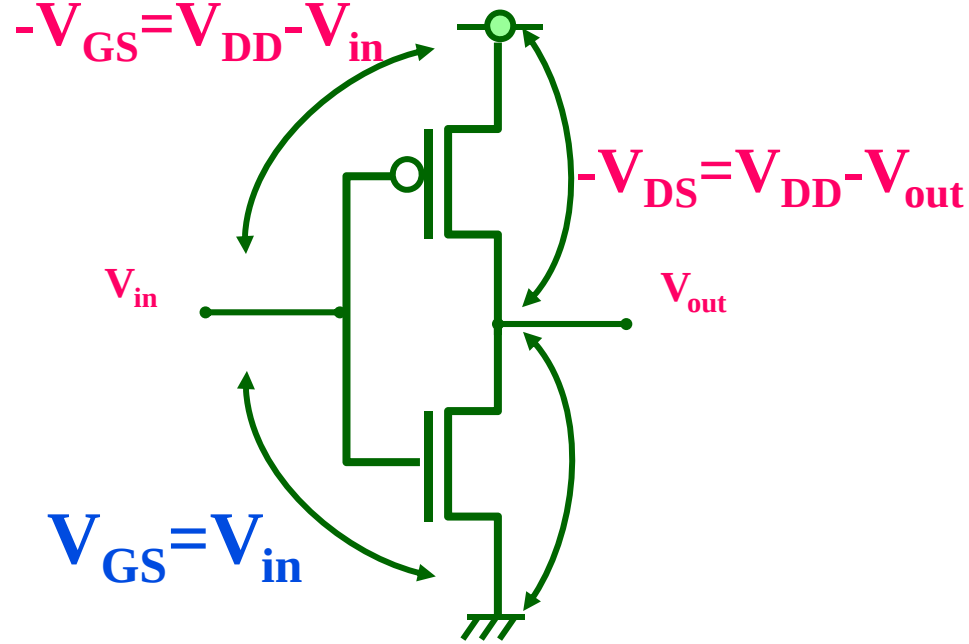
$$V_{IH}=\frac{V_{DD}+V_{TP}+k_R(2V_{out}+V_{TN})}{1+k_R} \quad (2)$$

由（1）（2）式联立可求得V_{IH}



3.逻辑阈值的计算





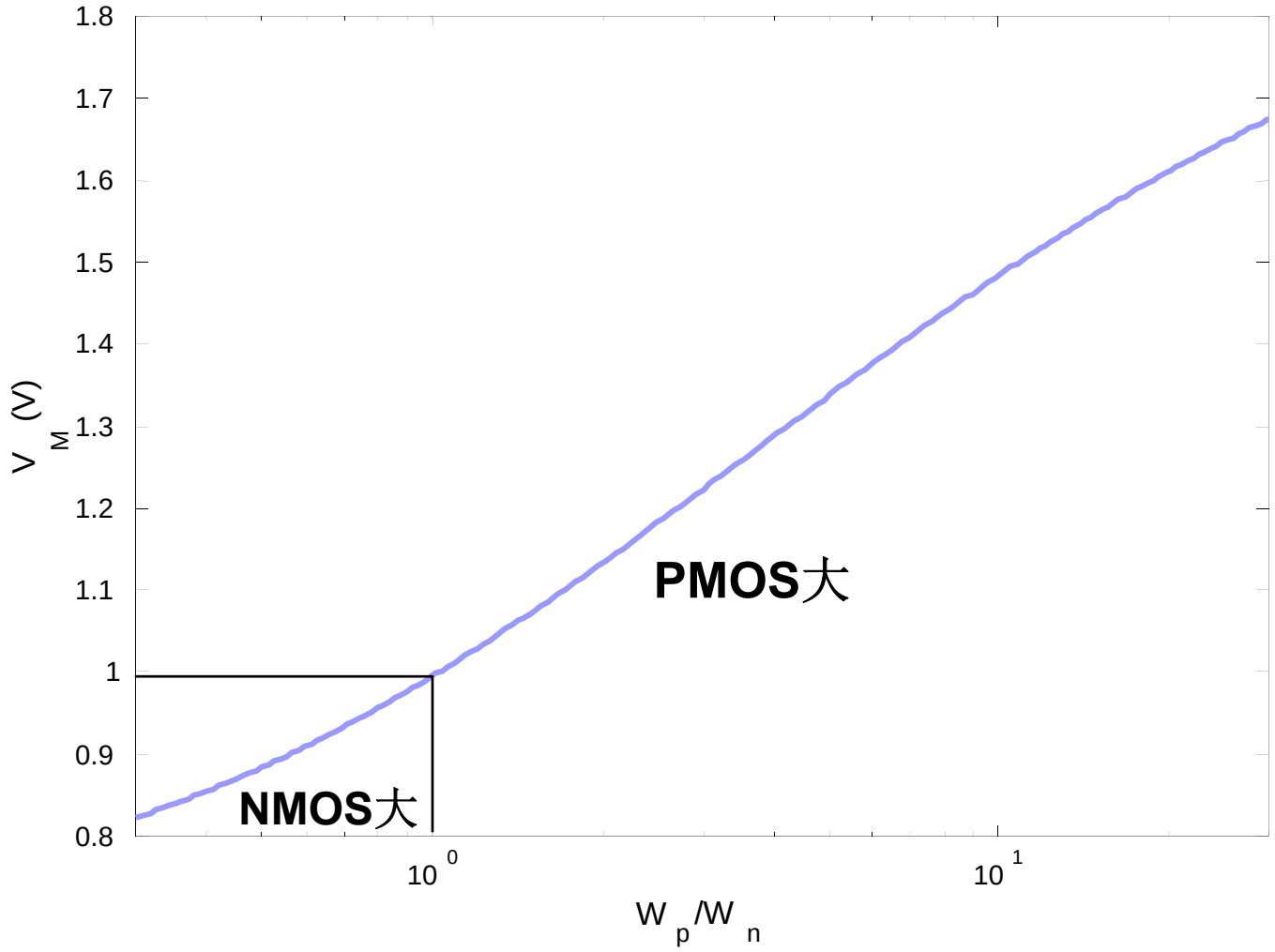
N管和P管均工作在饱和区

$$K_N(V_{in}-V_{TN})^2 = K_P(V_{DD}-V_{in}-|V_{TP}|)^2$$

令 $V_M=V_{in}$ 得

$$V_M = \frac{V_{DD}+V_{TP}+V_{TN}\sqrt{K_R}}{1+\sqrt{K_R}}$$

逻辑阈值与晶体管尺寸的关系



0.25um晶体管
V_{DD}=2.5v

CMOS反相器的噪声容限

$$V_{IL} = \frac{2V_{out} + V_{TP} - V_{DD} + k_R V_{TN}}{1 + k_R}$$

$$V_{IH} = \frac{V_{DD} + V_{TP} + k_R(2V_{out} + V_{TN})}{1 + k_R}$$

$$NM_L = V_{IL} - V_{OL}$$

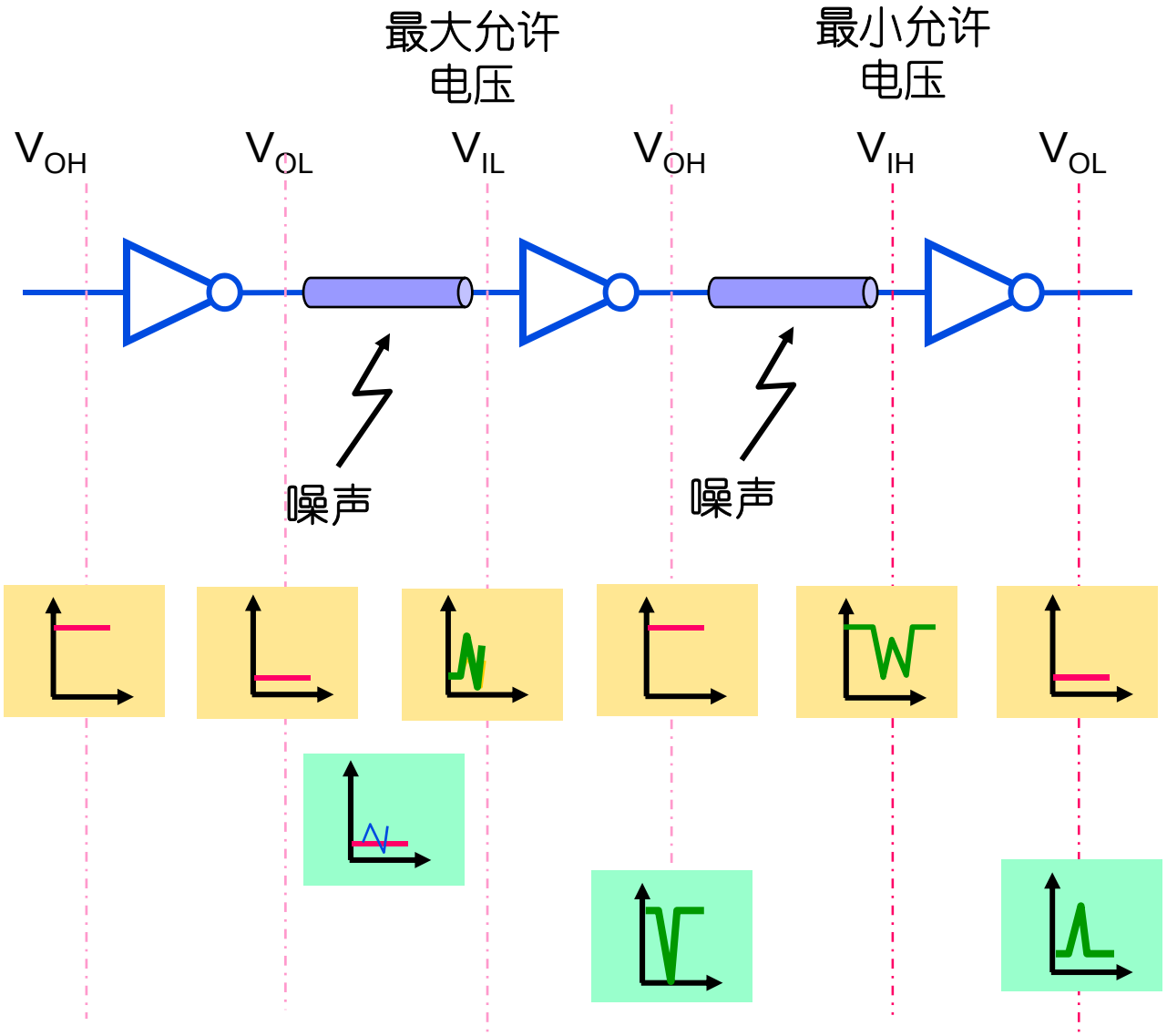
$$NM_H = V_{OH} - V_{IH}$$

例 考虑一个具有如下参数的CMOS反相器电路：

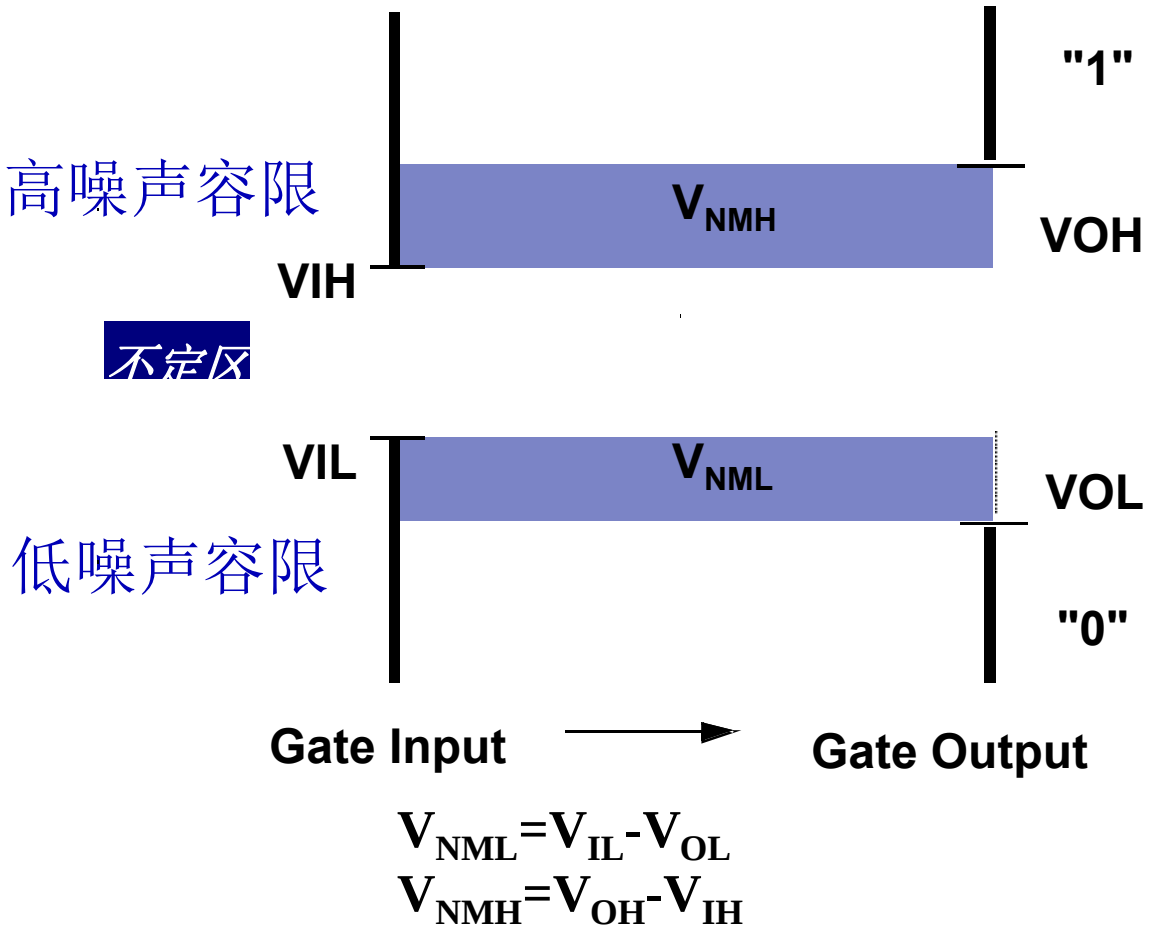
$$V_{DD} = 3.3V, V_{Tn} = 0.6V, V_{Tp} = -0.7V, K_n = 100\mu A/V^2, K_p = 40\mu A/V^2$$

计算电路的噪声容限

噪声抑制与噪声容限

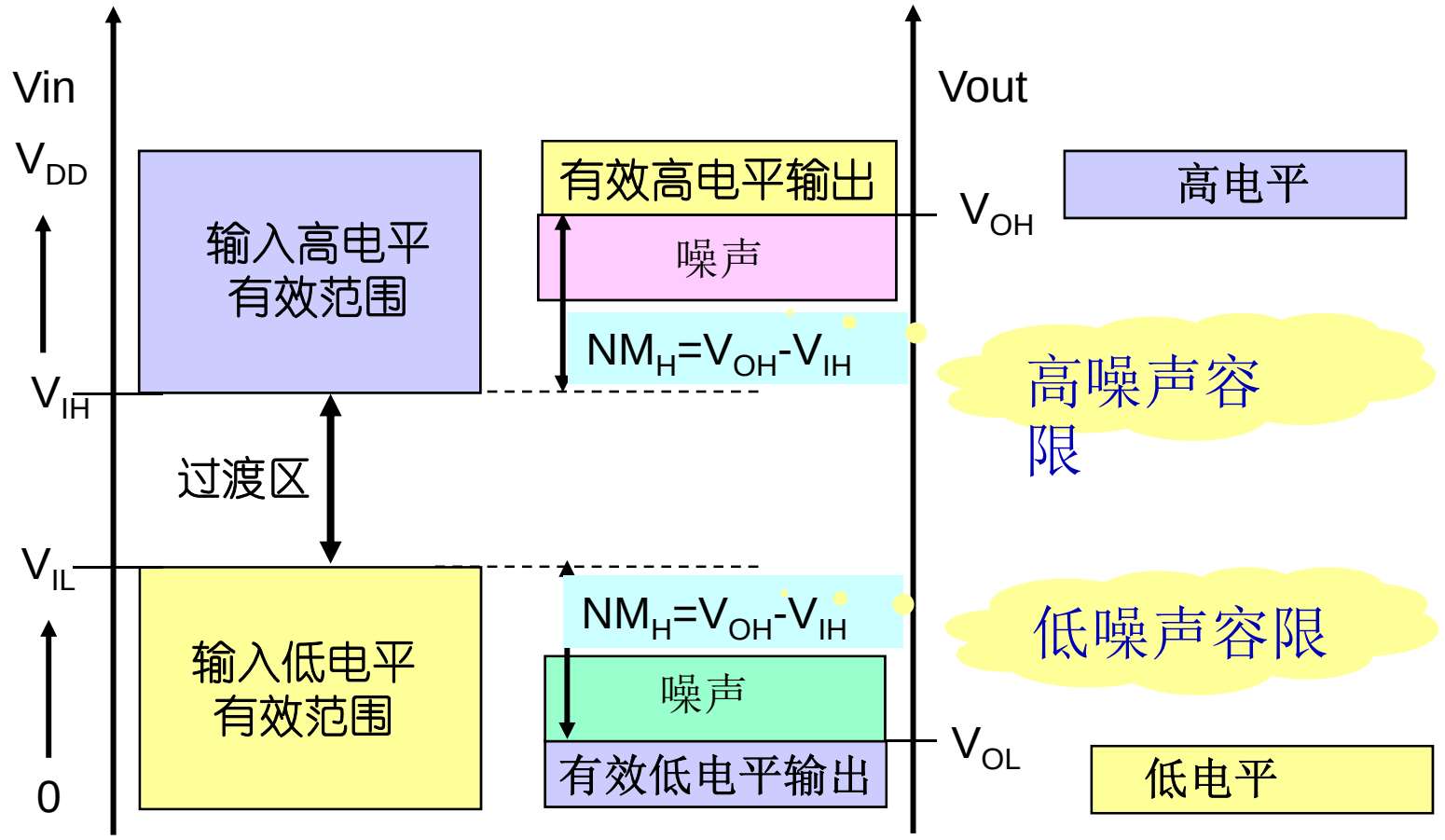


噪声抑制与噪声容限



$$V_{NML}=V_{IL}-V_{OL}$$
$$V_{NMH}=V_{OH}-V_{IH}$$

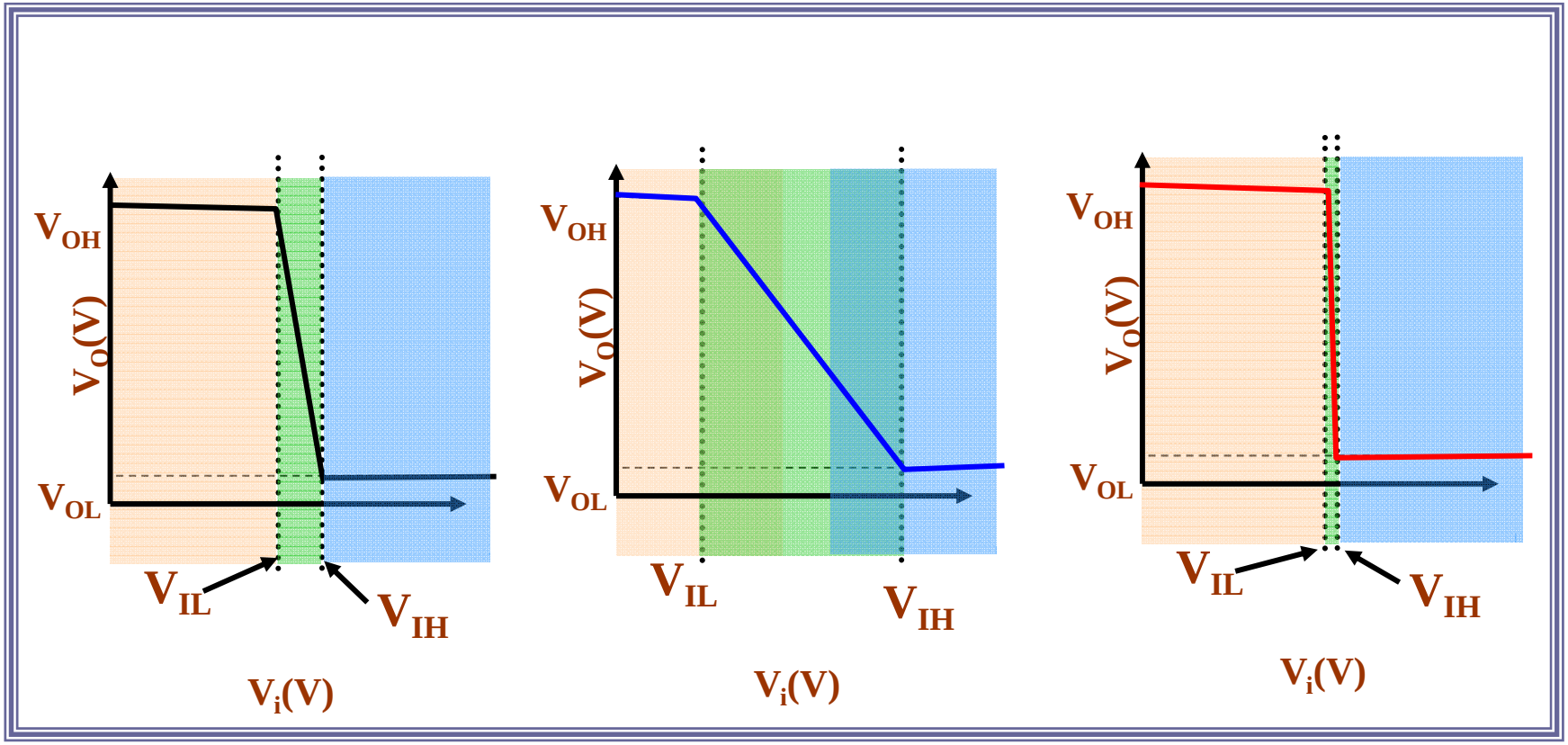
噪声抑制与噪声容限

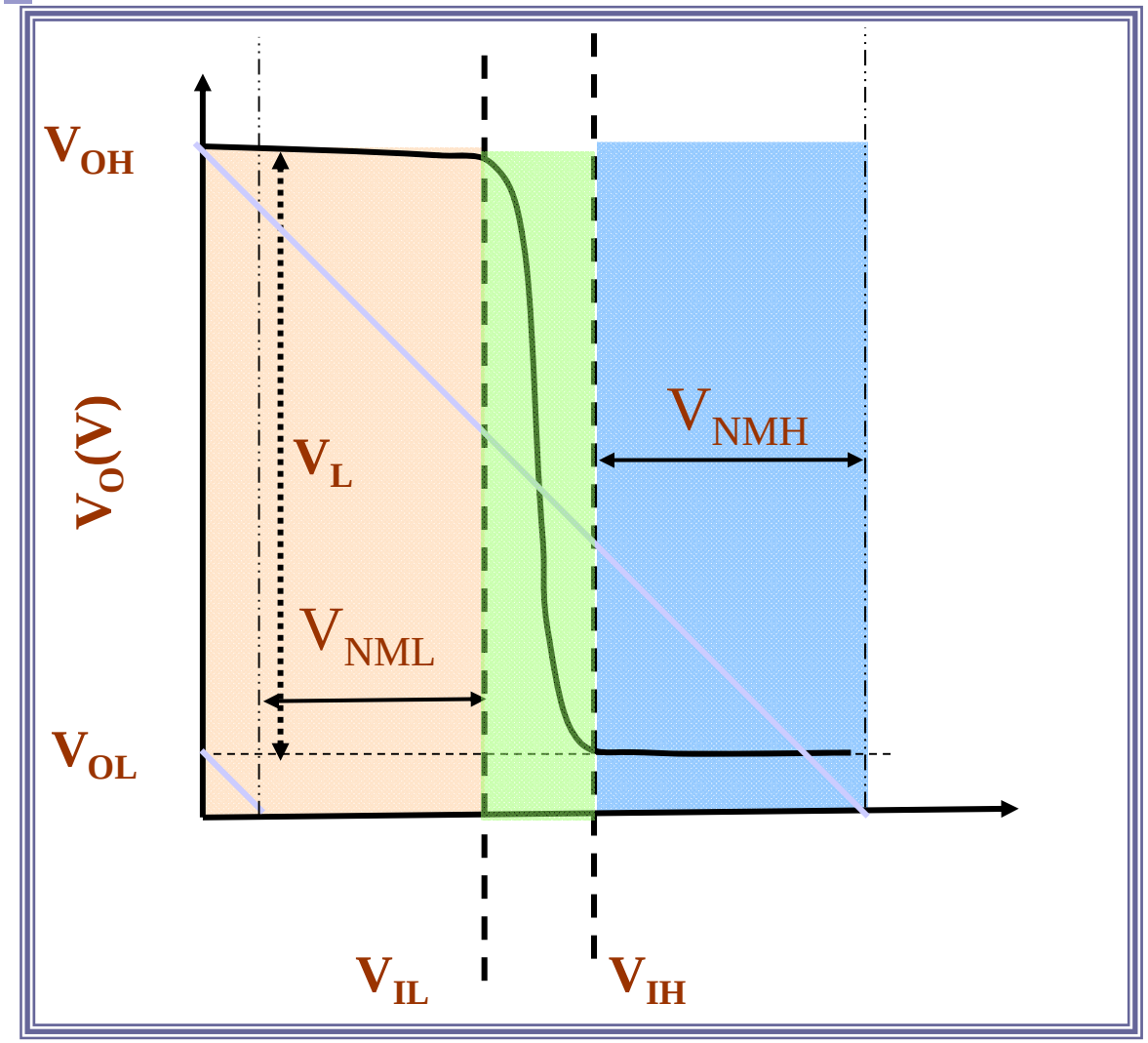


噪声幅值＋$V_{OL}<V_{IL}$ ⟹ 噪声幅值< $V_{IL}-V_{OL}$

噪声幅值＋$V_{IH}<V_{OH}$ ⟹ 噪声幅值< $V_{OH}-V_{IH}$

2.抗干扰能力


V_{OH}
$V_O(V)$
V_{OL}
V_{IL}
V_{IH}
$V_i(V)$
V_{OH}
$V_O(V)$
V_{OL}
V_{IL}
V_{IH}
$V_i(V)$
V_{OH}
$V_O(V)$
V_{OL}
V_{IL}
V_{IH}
$V_i(V)$



$$V_{NMH}=V_{OH}-V_{IH}$$

$$V_{NML}=V_{IL}-V_{OL}$$

解: 对于CMOS反相器来说,V_{OL}=0V,V_{OH}=3.3V

$$V_{IL} = \frac{2V_{out} + V_{Tp} - V_{DD} + K_R V_{Tn}}{1 + K_R}$$

$$= \frac{2V_{out} - 0.7 - 3.3 + 1.5}{1 + 2.5} = 0.57V_{out} - 0.71$$

当V_{IN}=V_{IL}时,nMOS管工作在饱和区,pMOS管工作在线性区

则有: $K_P[2(V_{DD} - V_{in} - |V_{TP}|)(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2] = K_N(V_{in} - V_{TN})^2$

$$40[2(3.3 - 0.57V_{out} + 0.71 - 0.7)(3.3 - V_{out}) - (3.3 - V_{out})^2] = 100(0.57Vout - 0.71 - 0.6)^2$$

$$0.66V_{out}{}^{2} + 0.05V_{out} - 6.65 = 0$$

$$Vout = \frac{-0.05 \pm \sqrt{0.05^2 + 4 \times 0.66 \times 6.65}}{2 \times 0.66}$$

$$= \frac{-0.05 \pm 4.19}{2 \times 0.66}$$

$$V_{out1} = 3.14V$$

$$V_{out2} = -3.17V$$

$$\therefore \quad V_{out} = 3.14V$$

$$V_{IL} = 0.57V_{out} - 0.71 = 1.08V$$

$$V_{IH} = \frac{V_{DD} + V_{Tp} + K_R(2V_{out} + V_{Tn})}{1 + K_R}$$

$$= \frac{3.3 - 0.7 + 2.5(2V_{out} + 0.6)}{1 + 2.5} = 1.43V_{out} + 1.17$$

当$V_{IN}=V_{IH}$时,nMOS管工作在线性区,pMOS管工作在饱和区

则有: $K_N[2(V_{in} - V_{TN})V_{out} - V_{out}^2] = K_P(V_{DD} - V_{in} - |V_{TP}|)^2$

$$100[2(1.43V_{out} + 1.17 - 0.6)V_{out} - V_{out}^2] = 40(3.3 - 1.43V_{out} - 1.17 - 0.7)^2$$

$$100[2(1.43V_{out}+1.17-0.6)V_{out}-V_{out}^{\,2}]=40(3.3-1.43V_{out}-1.17-0.7)^2$$

$$2.61V_{out}^{\,2}+6.94V_{out}-2.04=0$$

$$V_{out}=\frac{-6.94\pm\sqrt{6.94^2+4\times2.61\times2.04}}{2\times2.61}$$

$$V_{out1}=0.27\text{V}$$

$$\therefore V_{out}=0.27\text{V}$$

$$V_{out2}=-2.93\text{V}$$

$$V_{IH}=1.43V_{out}+1.17=1.55\text{V}$$

$$NM_L=V_{IL}-V_{OL}=1.08\text{V}$$

$$NM_H=V_{OH}-V_{IH}=3.3-1.55=1.75\text{V}$$