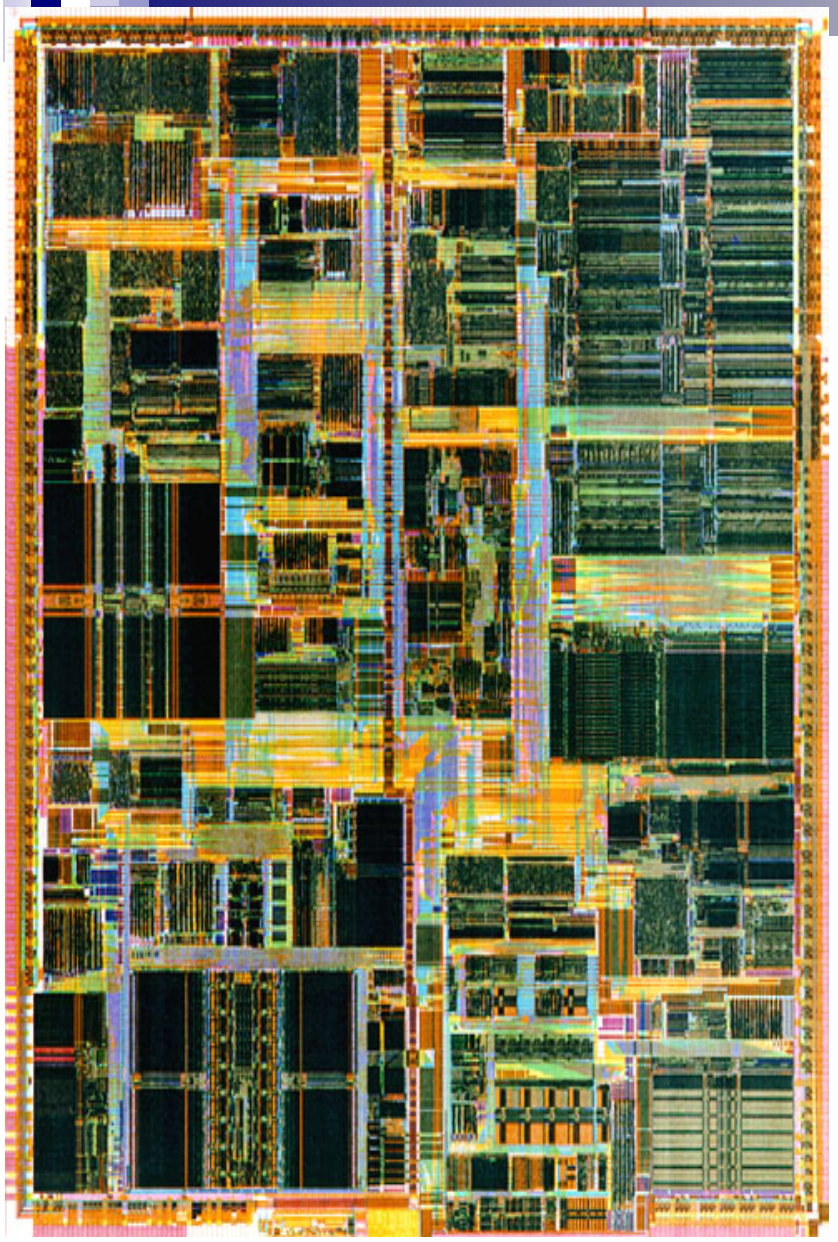


半导体集成电路

学校：西安理工大学
院系：自动化学院电子工程系
专业：电子、微电
时间：秋季学期

2012/11/27

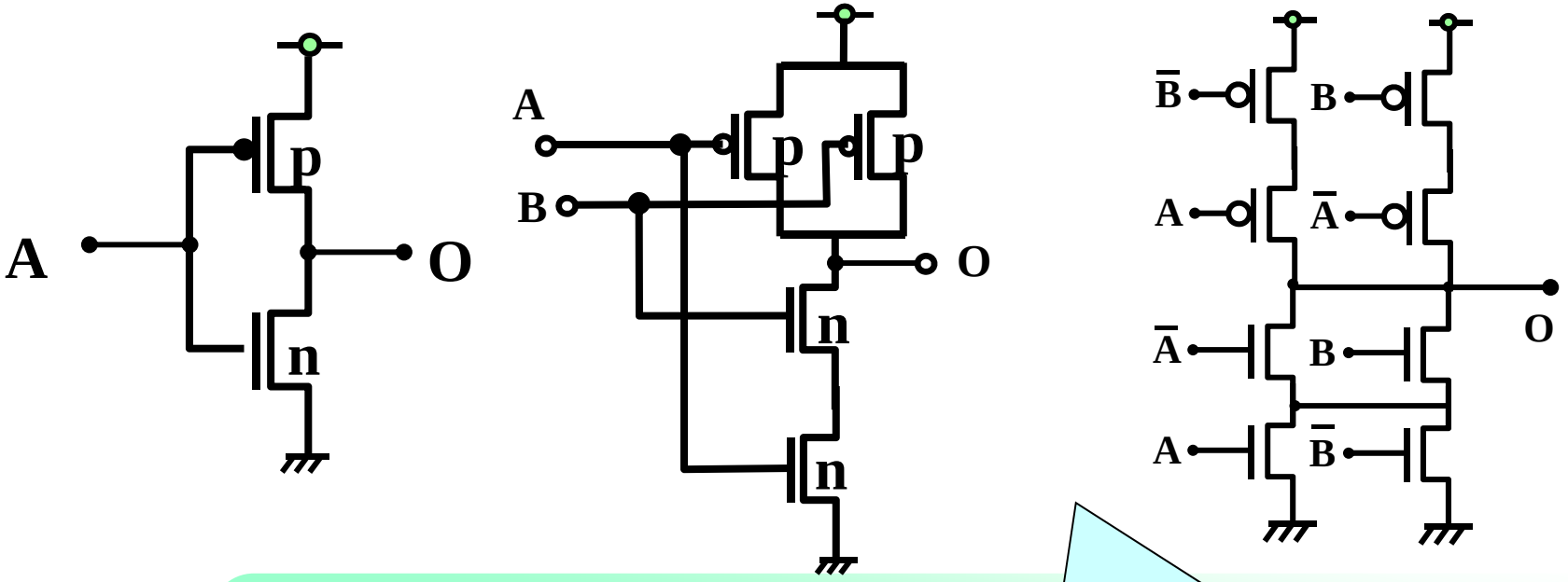
传输门逻辑

2012/11/27

内容提要

- 基本的传输门
- 信号传输延迟
- 传输门逻辑（pass-transistor logic)
- 传输门逻辑版图举例
- 传输门逻辑举例
- pass-transistor logic 的逻辑自动生成
- 小结

静态逻辑电路

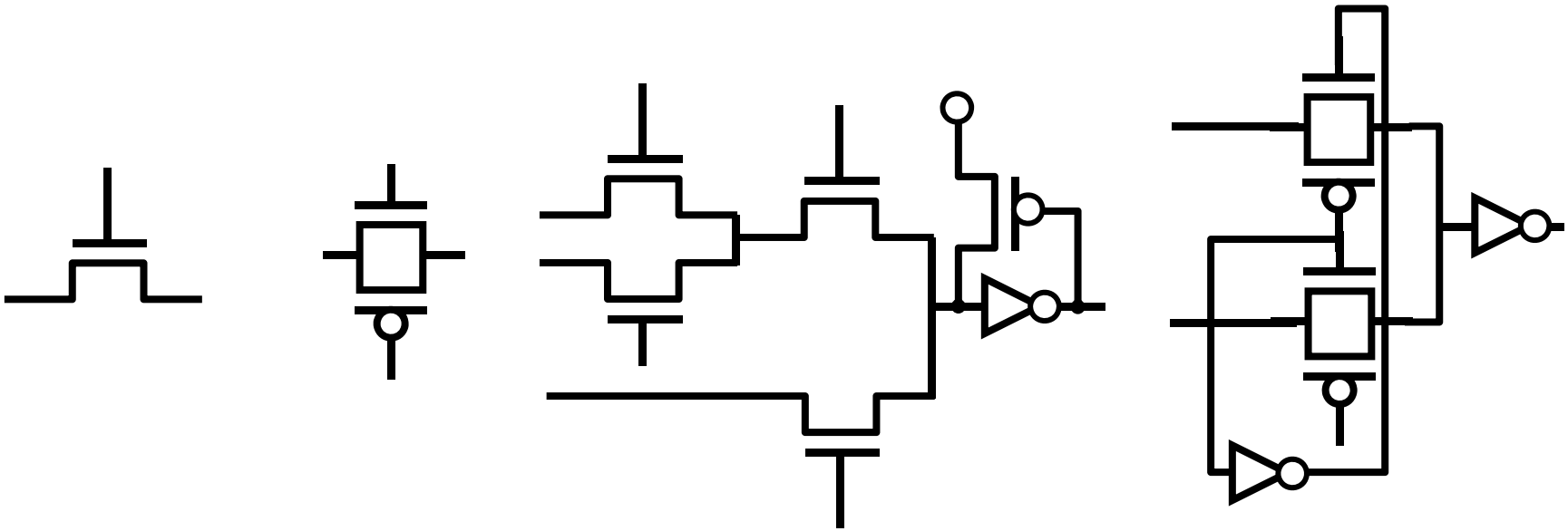


输入信号加在栅极上，而输出
输出为低电平逻辑时
输出为高电平逻辑

优点：低功耗
缺点：随着逻辑的复杂性增加，晶体管成倍增加

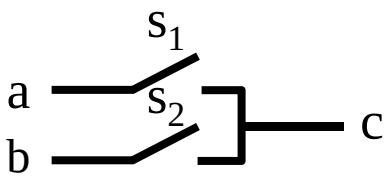
传输门逻辑

传输门逻辑电路



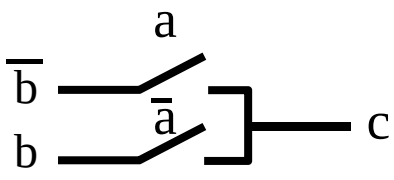
输入信号可以从栅极、源极、漏极输入
使用传输门构成传输门逻辑

传输门逻辑



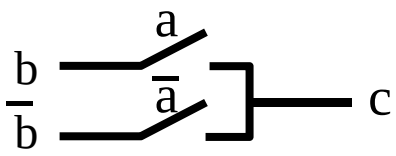
s2	s1	c
0	0	High-Z
0	1	a
1	0	b
1	1	c=a=b

MUX



a	b	c
0	0	0
0	1	1
1	0	1
1	1	0

XOR



a	b	c
0	0	1
0	1	0
1	0	0
1	1	1

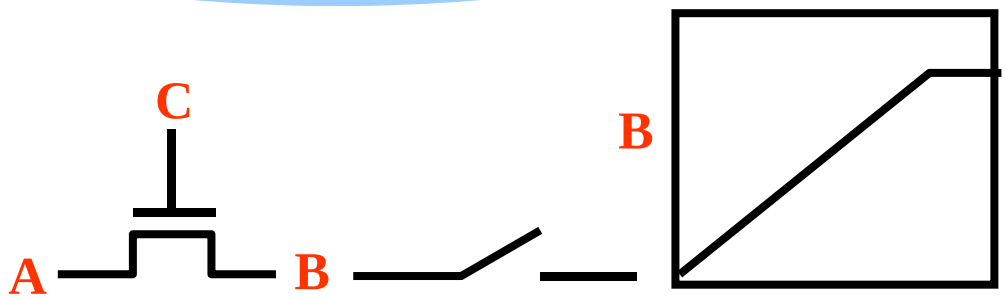
XNOR

一般情况下，不使用S1=S2
通常栅控制极上采用反向信号

特点：需要的晶体管数目少

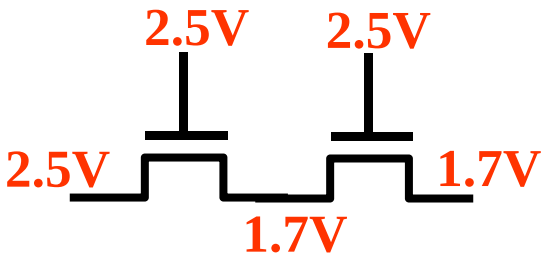
基本的传输门

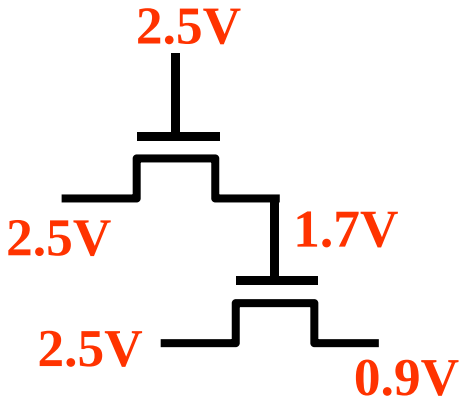
NMOS传输门

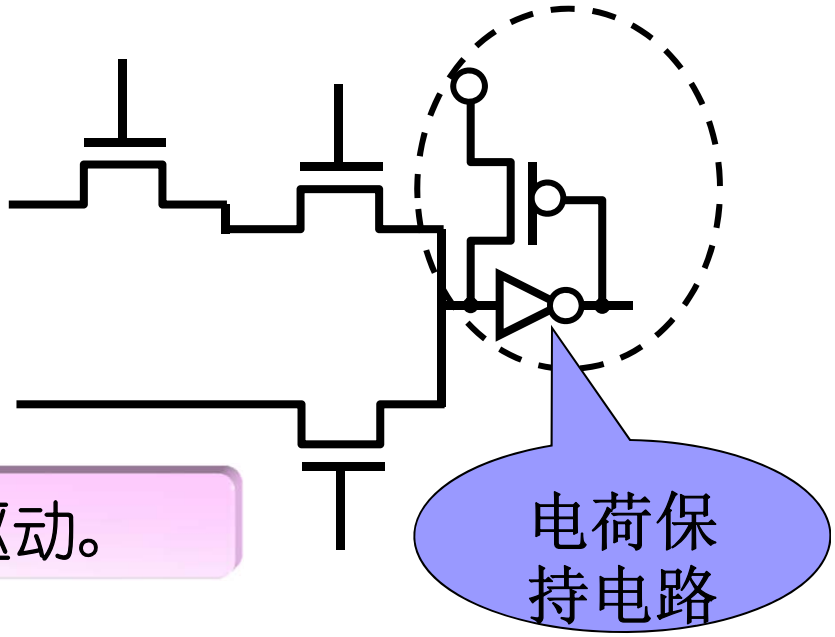


NMOS不能够正确的传输高电平

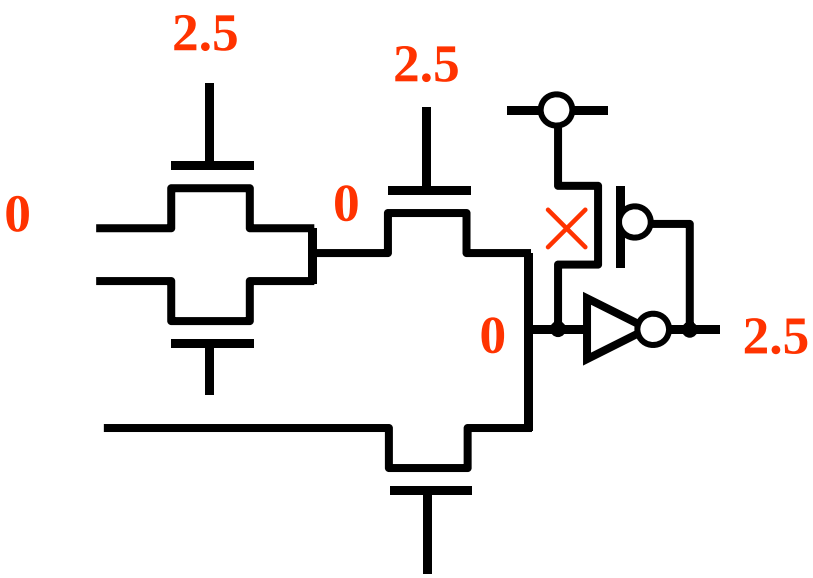
A（C：高电平）

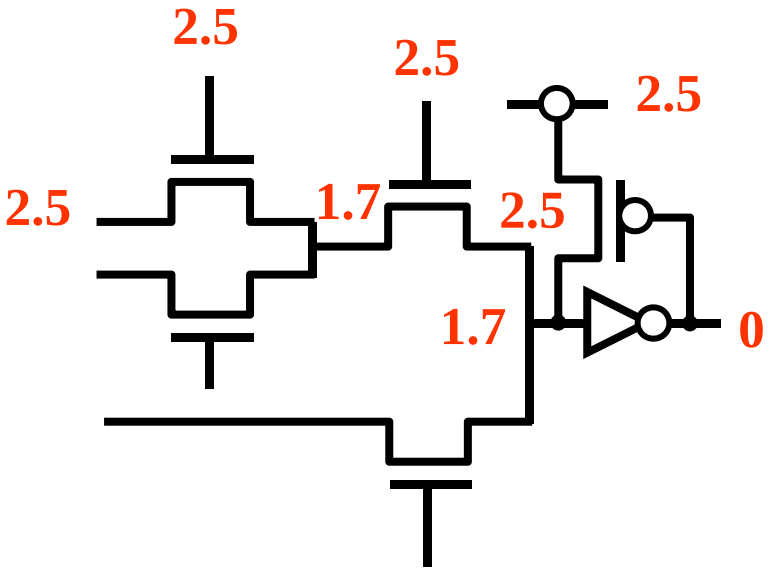


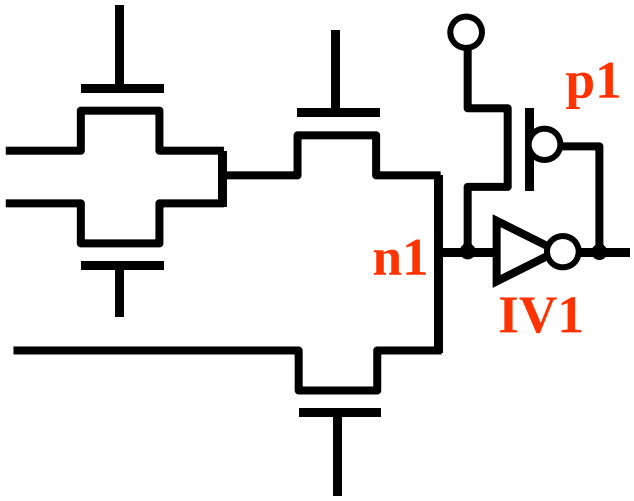




为了恢复全振幅，输出端用反向器驱动。


2.5
2.5
0
0
0
2.5


2.5
2.5
2.5
2.5
1.7
2.5
1.7
0



1. 传输高电平

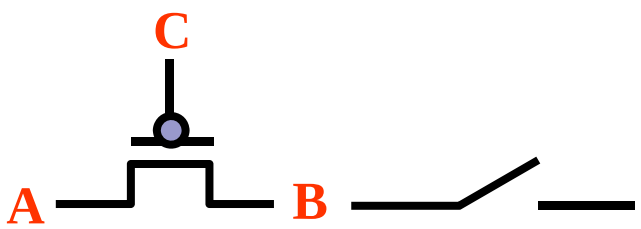
节点**n1**电位升高，当电位大于反向器**IV1**的逻辑阈值时，反向器输出低电平，此低电平加在**P1**管上，**P1**管导通，**n1**的电位可以上升到**VDD**。

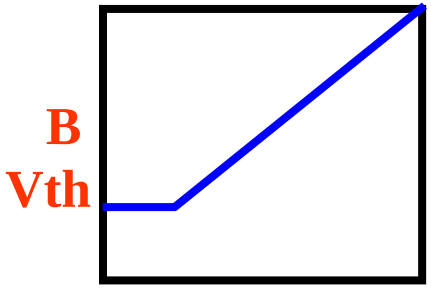
2. 传输低电平

节点**n1**电位较低，当电位小于反向器**IV1**的逻辑阈值时，反向器输出高电平，此高电平加在**P1**管上，**P1**管截止，**n1**的电位保持传输来的低电平。

基本的传输门

PMOS传输门





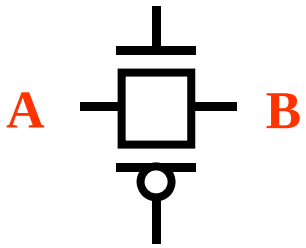
A（C：低电平）

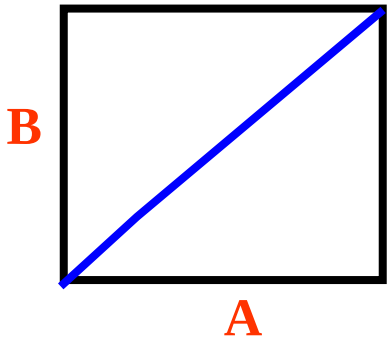
PMOS不能够正确的传输低电平

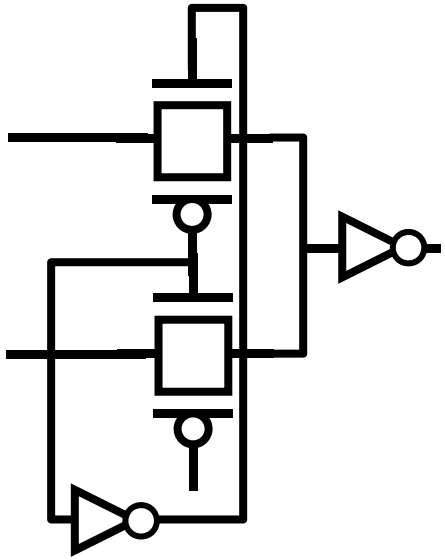
通常在传输固定的高电平时用

基本的传输门

CMOS传输门







传输高电平时**PMOS**工作，传输低电平时**NMOS**工作

高电平、低电平都可以正确传输
但是、电路规模增大

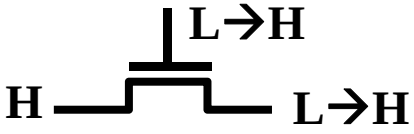
信号传输延迟时间

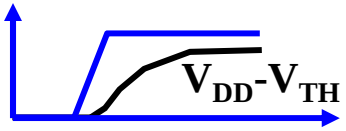
信号传输的4种模式

1. 栅控制端L→H, 漏极H, 源极L

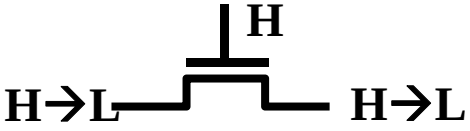
与静态逻辑门相同

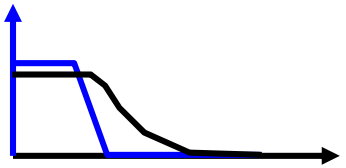
2. 栅控制端L→H, 漏极L, 源极H



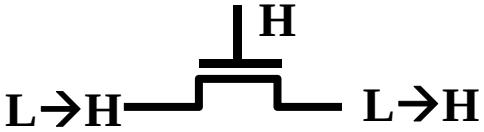


3. 栅控制端H, 漏极H→L, 源极H→L





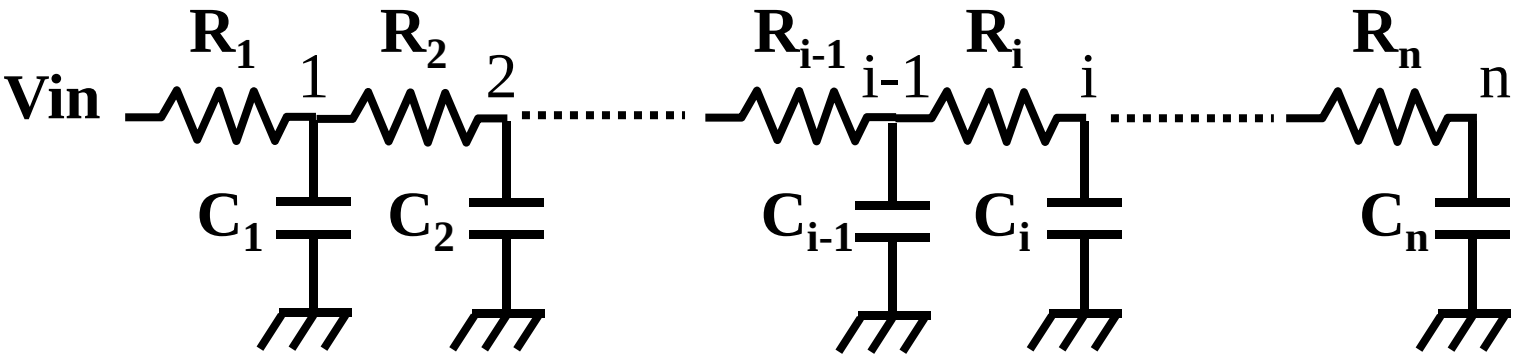
4. 栅控制端H, 漏极L→H, 源极L→H



多数情况下漏源电压较小，传输门晶体管工作在非饱和区，可将管子看作电阻。但是，由于高电平输出只能达到V_{DD}-V_{TH},因此t_{PLH}较大。

信号传输延迟时间

将晶体管作为电阻时：

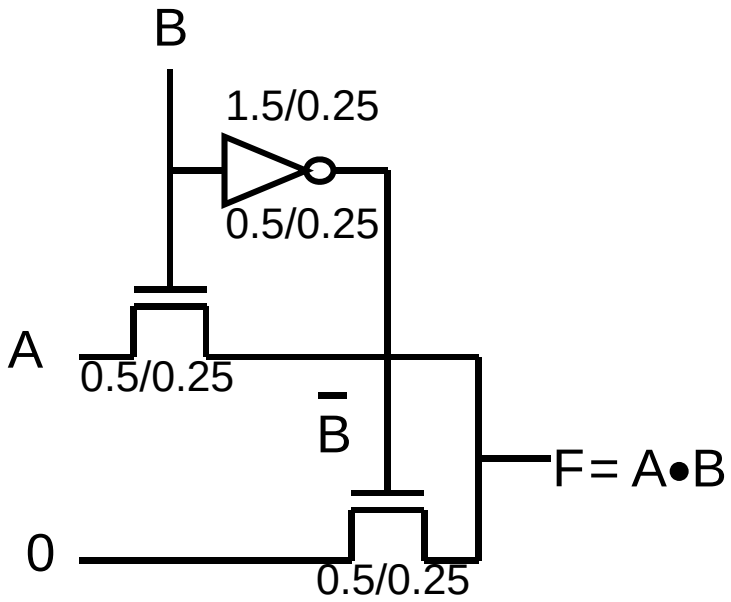


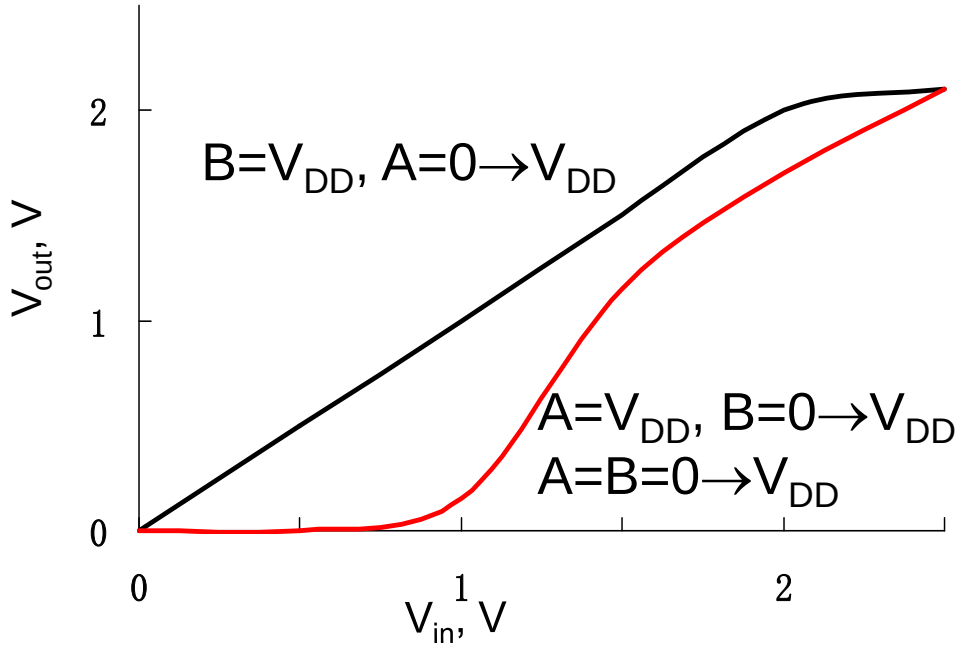
Elmore 近似公式

节点i的时定常数为：$\tau_{Di}=C_1R_1+C_2(R_2+R_1)+\ldots\ldots C_i(R_1+R_2+\ldots+R_i)$

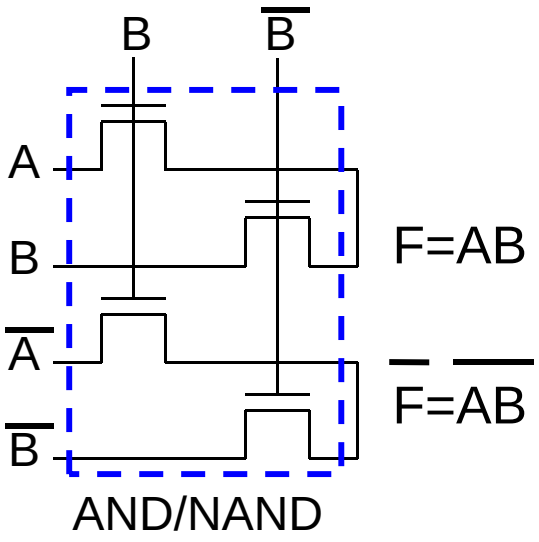
传输门单元串联接续时，段数增加，延迟时间变大，
需要随处插入反向器。（通常串联接续段数控制在4内）

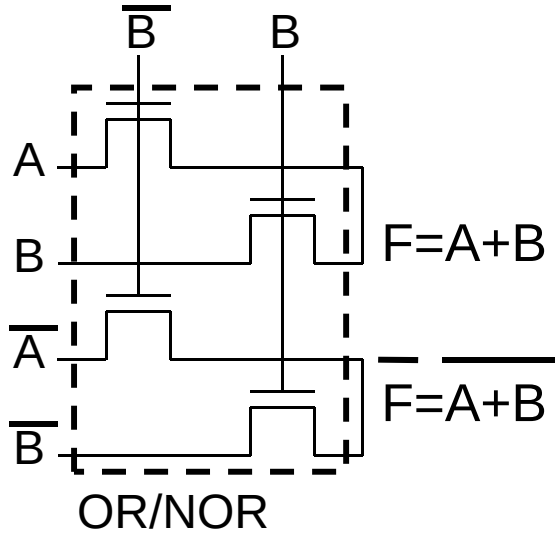
传输门逻辑

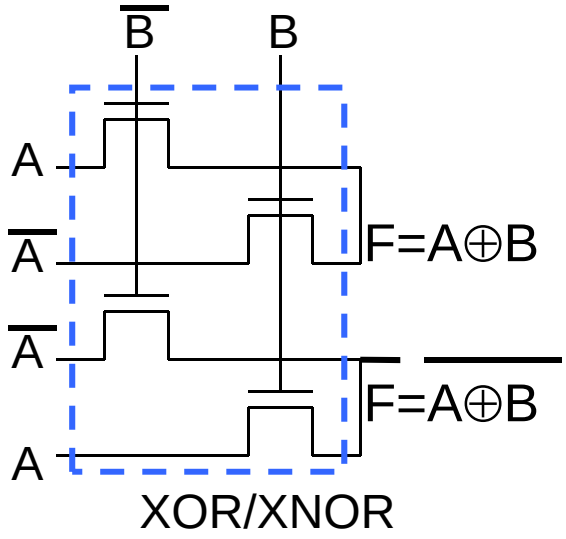

B
1.5/0.25
0.5/0.25
A
0.5/0.25
B
F= A•B
0
0.5/0.25


B=V_DD, A=0→V_DD
A=V_DD, B=0→V_DD
A=B=0→V_DD
V_out, V
V_in, V
0
1
2

传输门逻辑

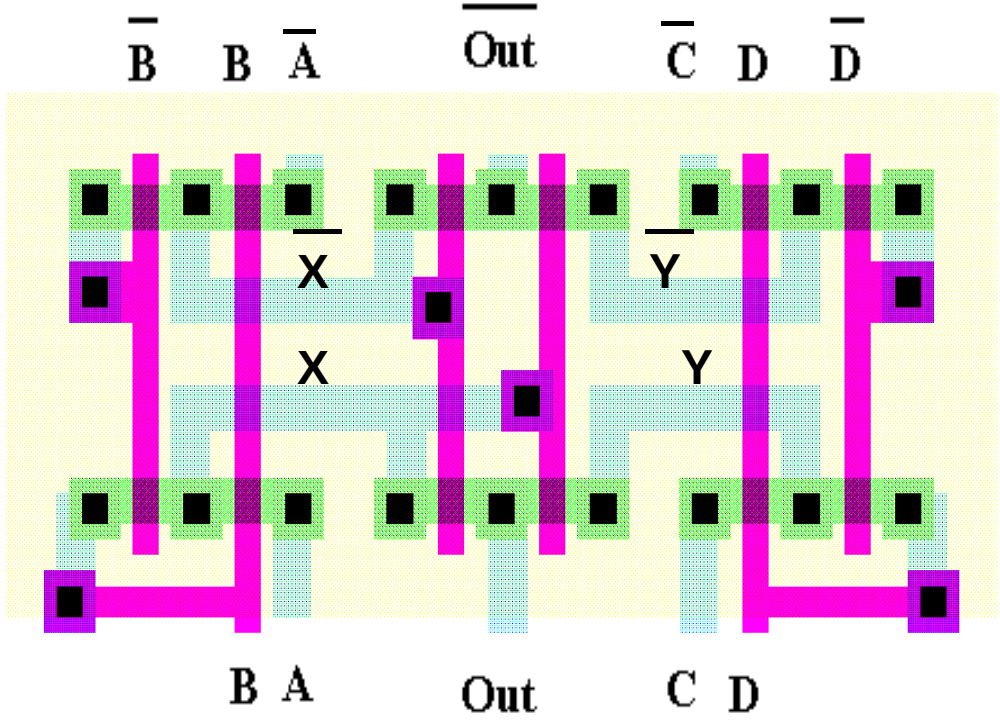


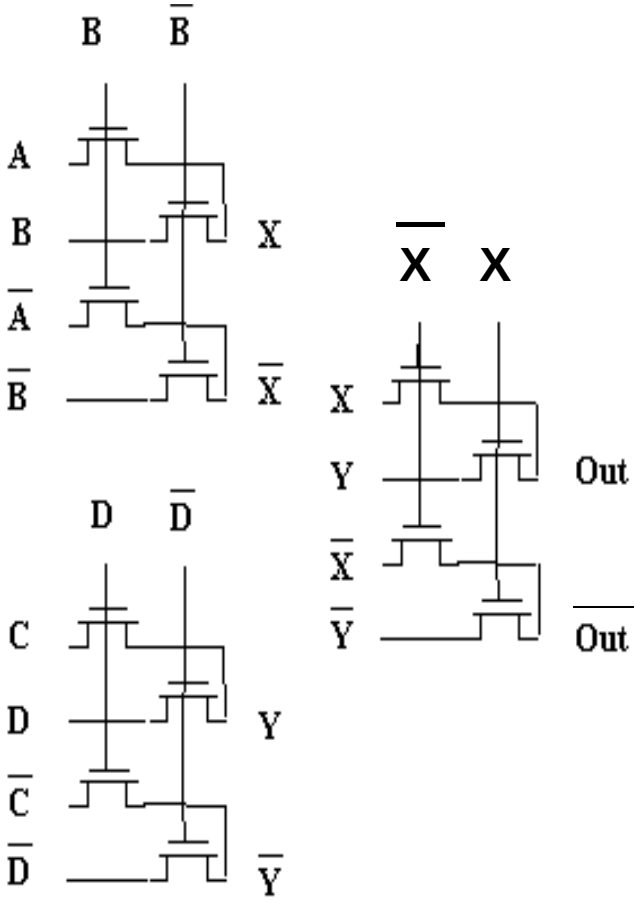




相同的电路结构，输入信号不同时，构成不同的逻辑功能

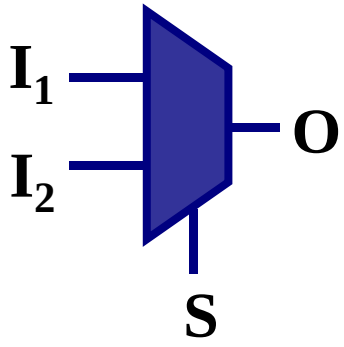
传输门逻辑版图举例

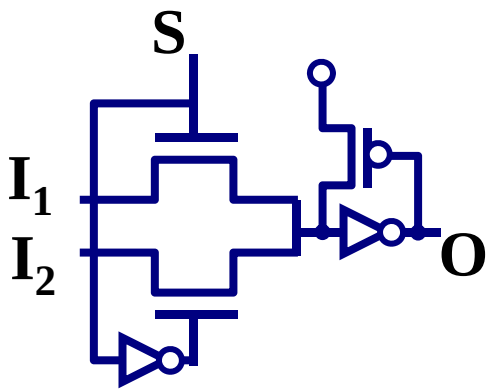




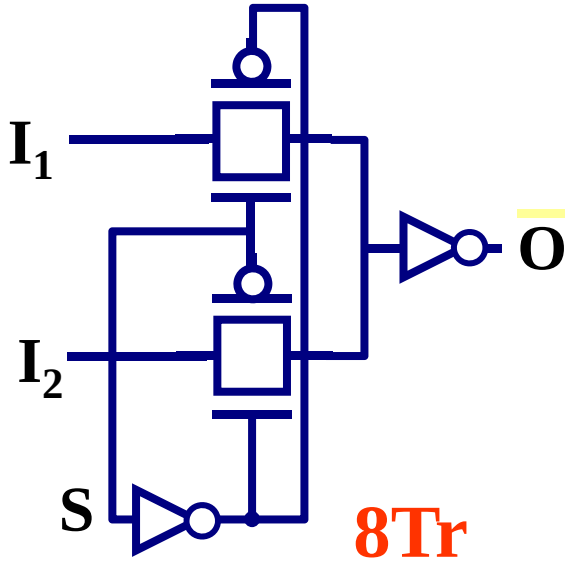
传输门逻辑举例

2输入MUX

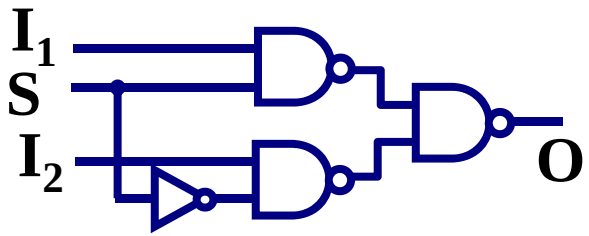




7Tr

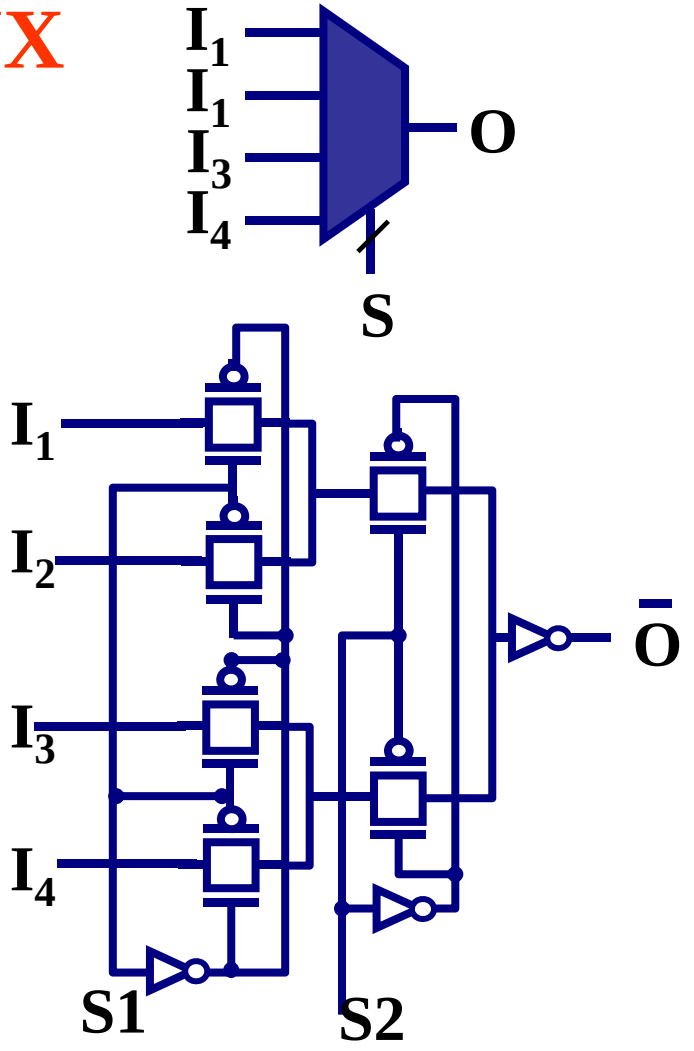


8Tr



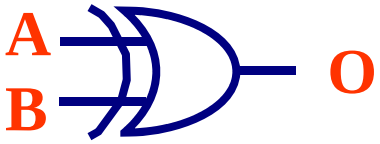
14Tr（静态逻辑）

4输入MUX

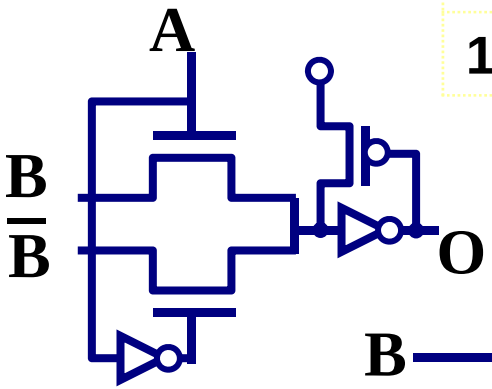


传输门逻辑举例

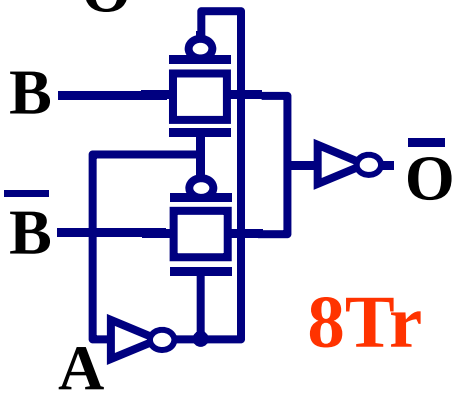
2输入XOR（异或门）



A	B	O
0	0	0
0	1	1
1	0	1
1	1	0

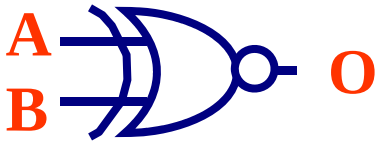


7Tr

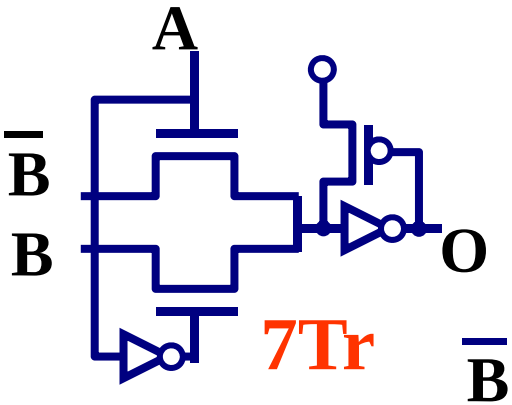


8Tr

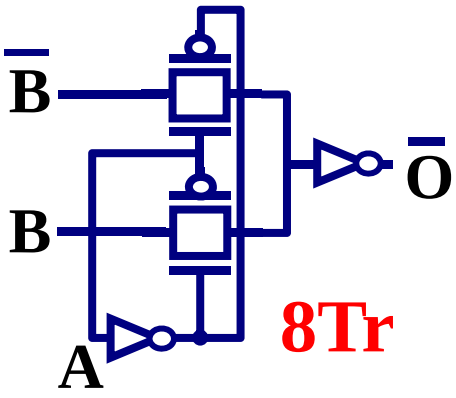
2输入XNOR（同或门）



A	B	O
0	0	1
0	1	0
1	0	0
1	1	1



7Tr



8Tr

移 位 器

- 在实际数据计算时，有时需要进行数据的移位计算。如：

1000 ←→ 8

1000右移一位，变为0100

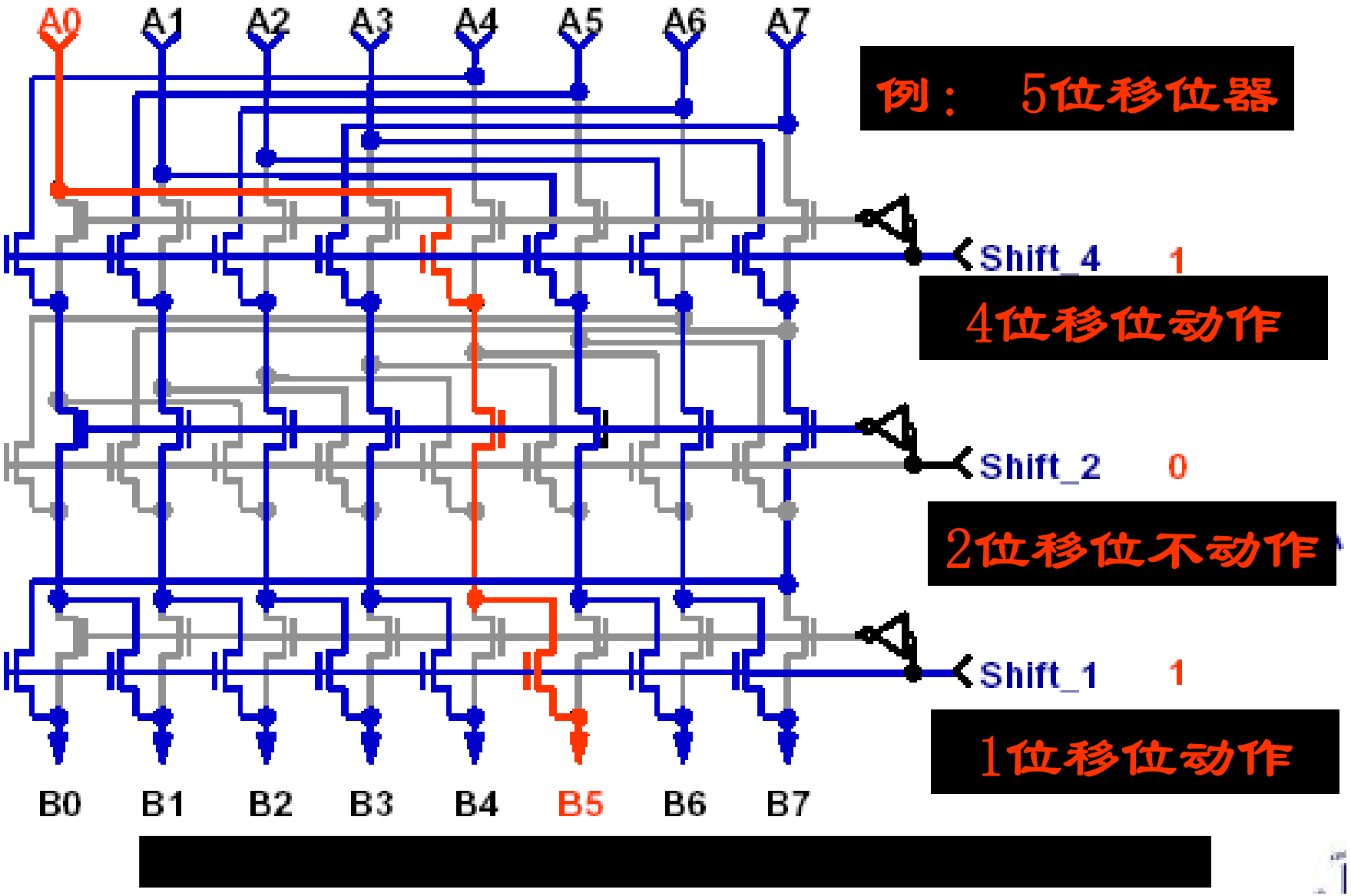
100 ←→ 4

1000右移两位，变为0010

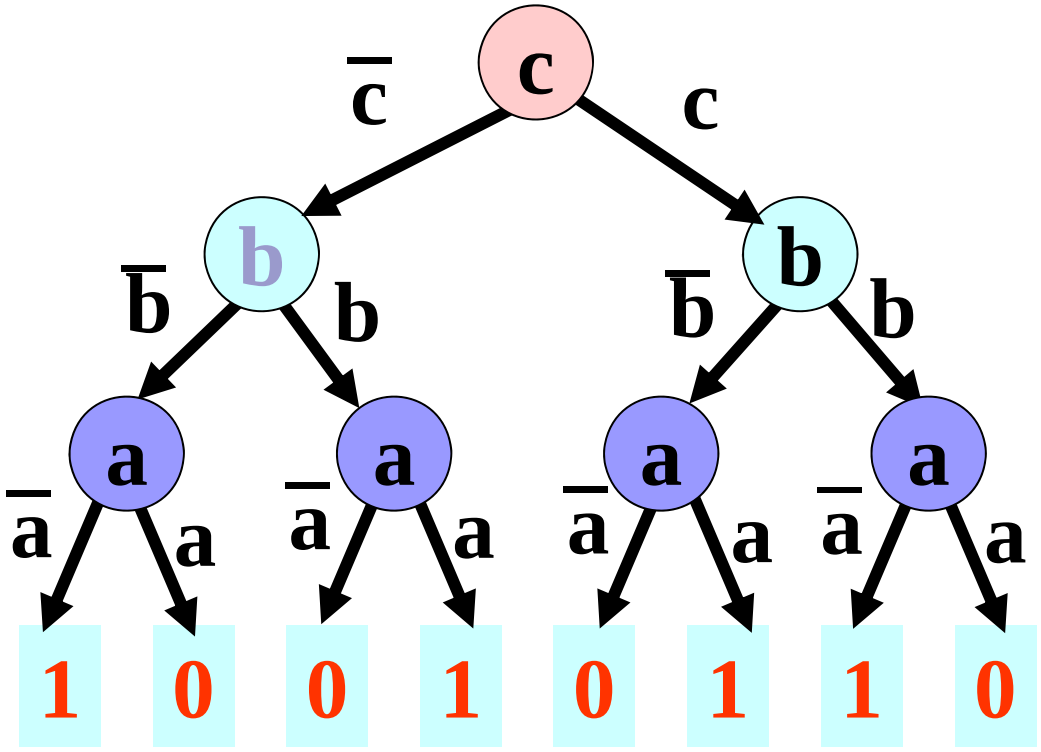
10 ←→ 2

每右移一位就相当于除2

移位器

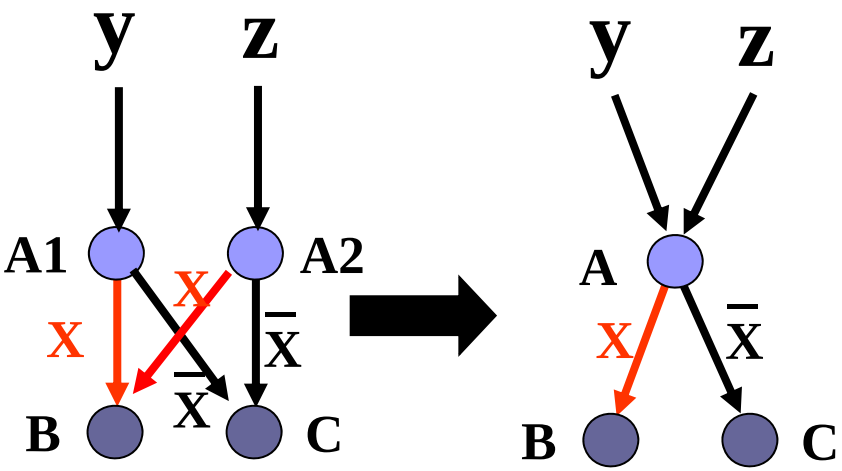

A0
A1
A2
A3
A4
A5
A6
A7
例： 5位移位器
Shift_4 1
4位移位动作
Shift_2 0
2位移位不动作
Shift_1 1
1位移位动作
B0
B1
B2
B3
B4
B5
B6
B7

基于BDD的自动逻辑生成



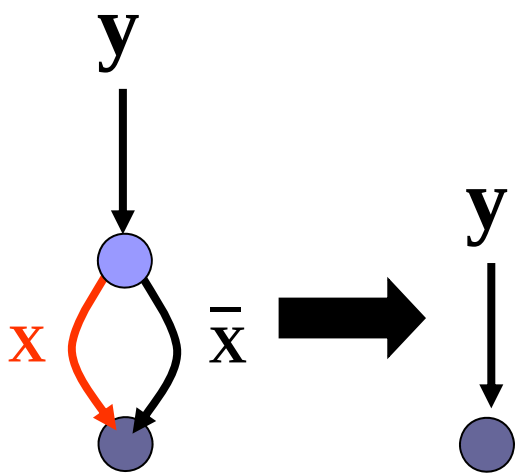
c	b	a	f	$\overline{f}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

BDD的缩小规则



缩减规则1

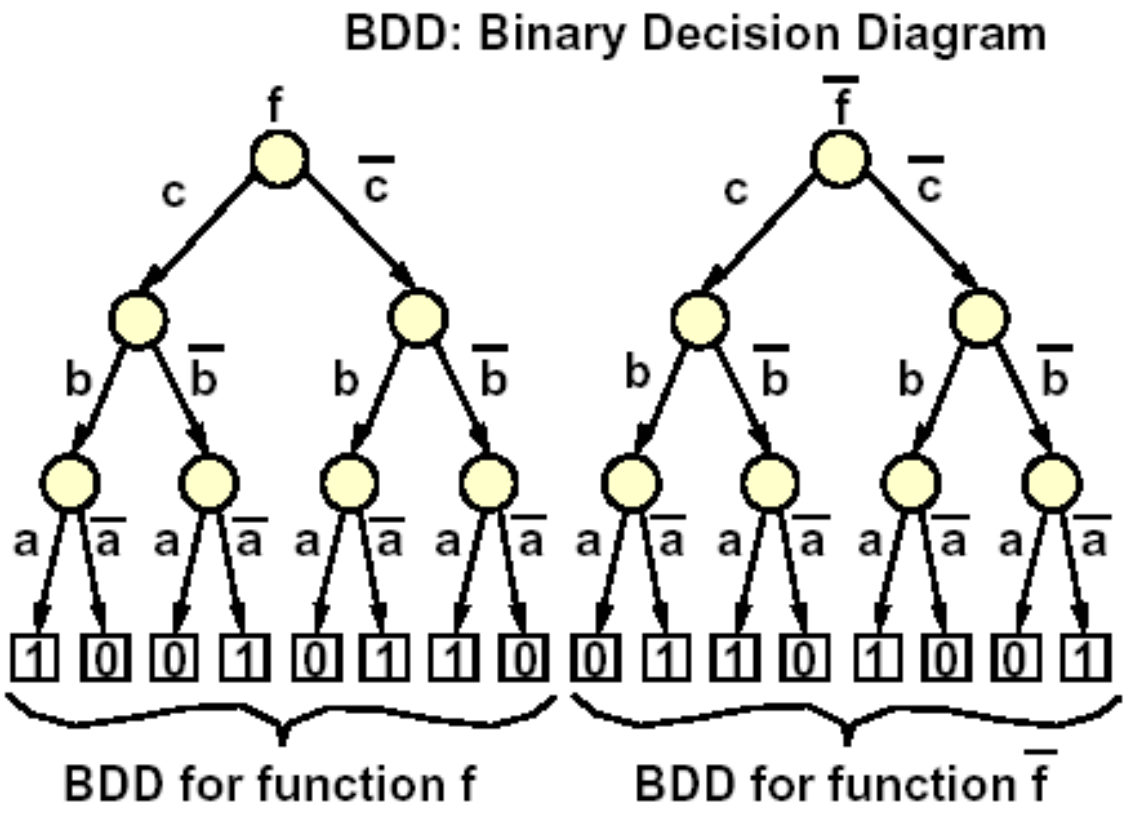
当两个节点的传输到下一级节点的传输路径完全相同时，两个节点可以缩减为1个



缩减规则2

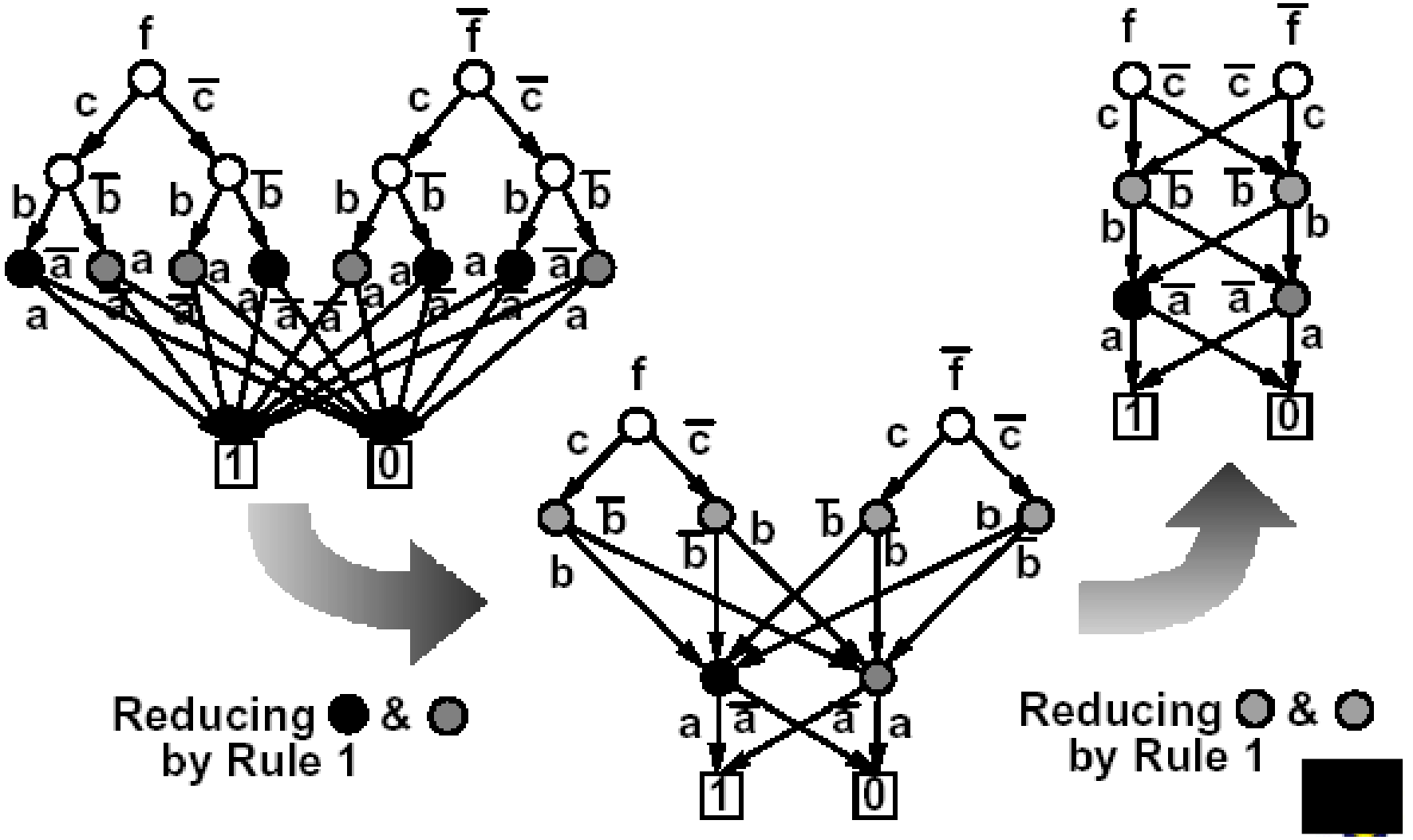
当1节点的所有传输路径都归结到同一个下一级节点时，这个节点可以省略.

基于BDD的自动逻辑生成

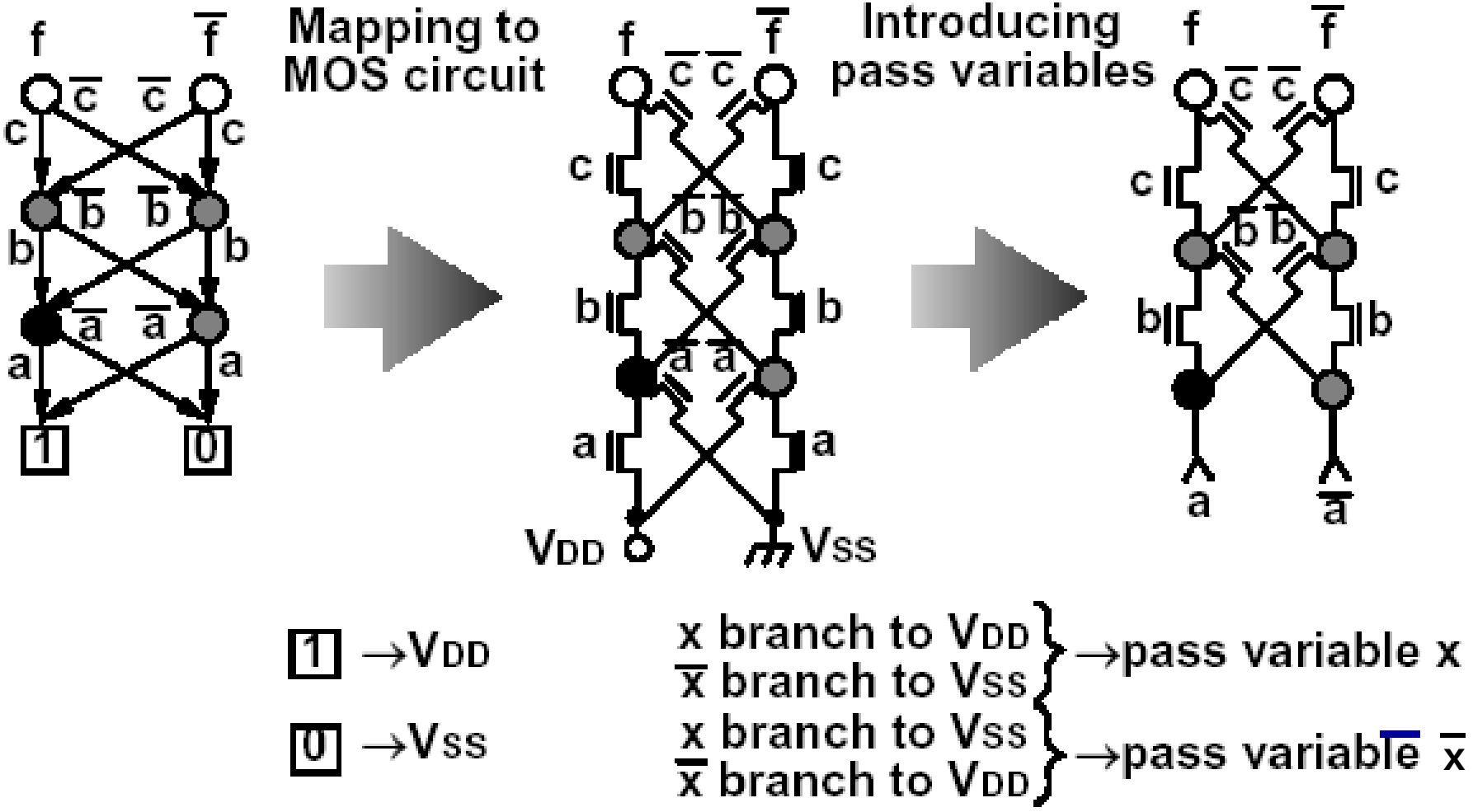


c	b	a	f	$\overline{f}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

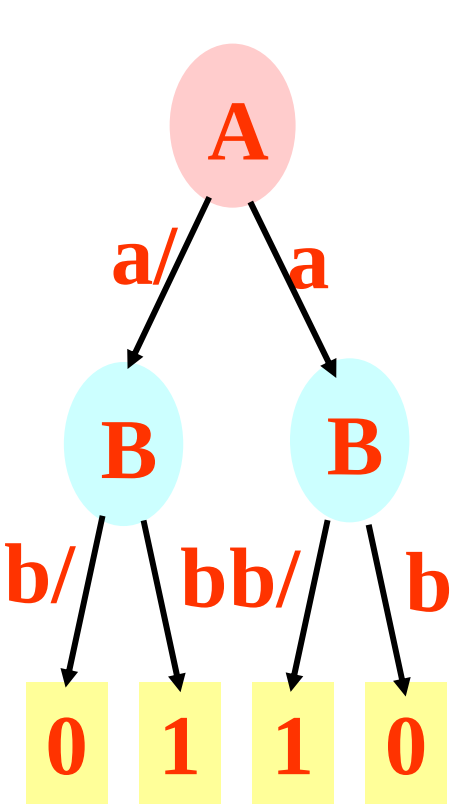
BDD的缩小过程

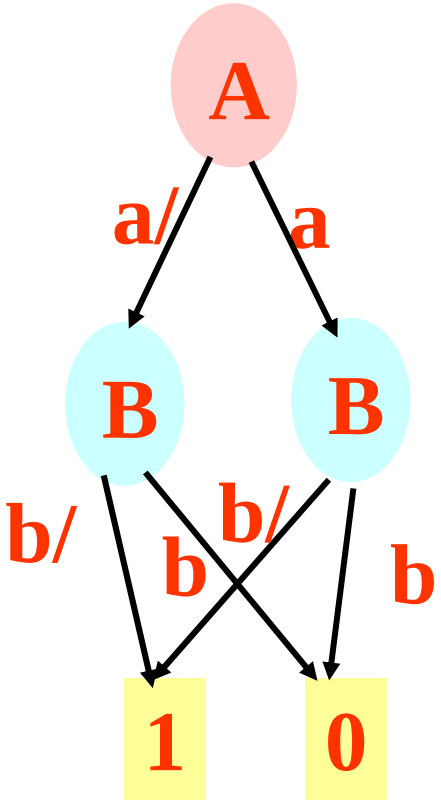


将BDD转换为MOS电路的过程



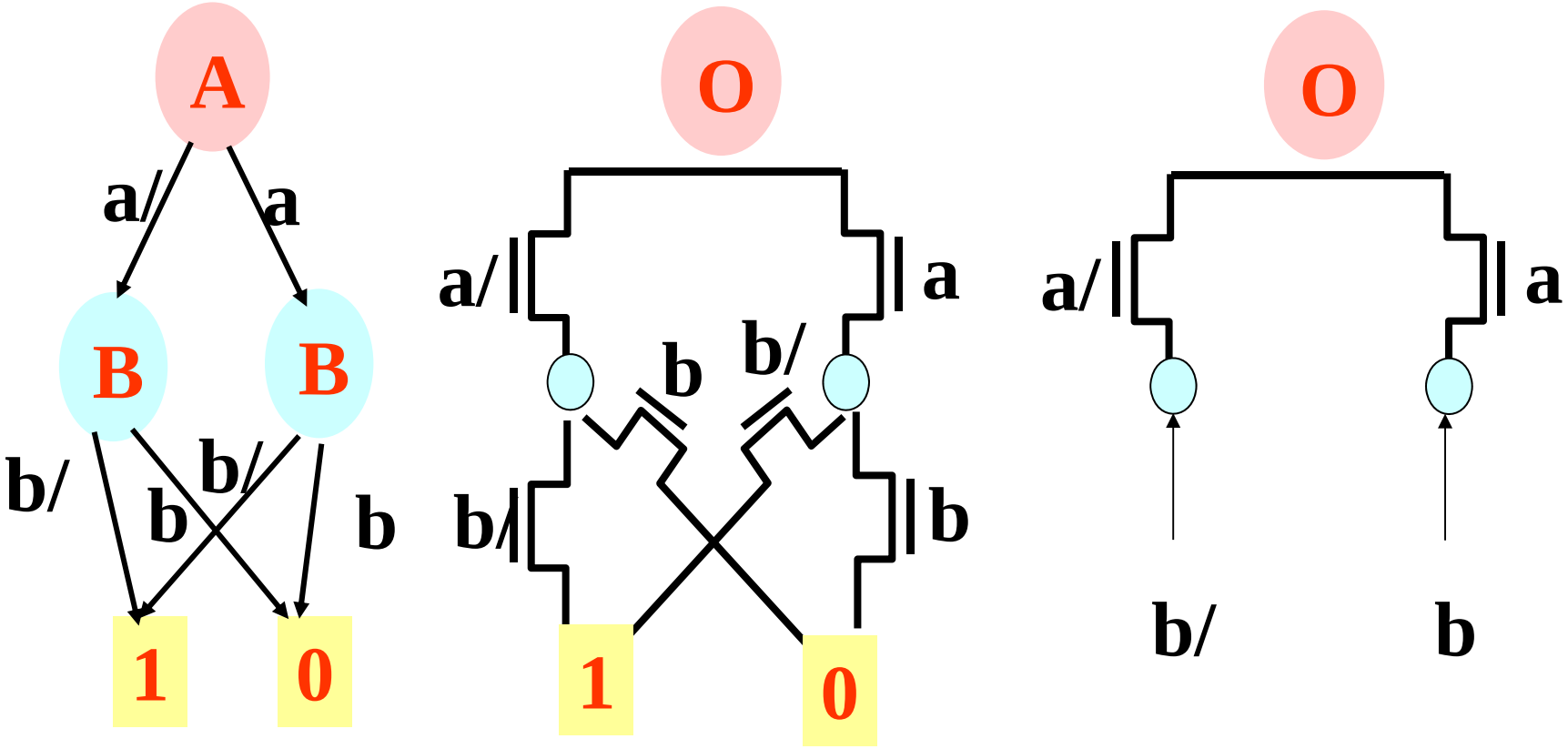
举　例





A	B	O
0	0	0
0	1	1
1	0	1
1	1	0

举　例(续)



总　　结

❖传输门逻辑在构成信号转换电路、信号选择低电路、异或同或逻辑、 运算器时，性能高于静态逻辑电路，使用较为广泛。

❖逻辑门传输电路的振幅由于阈值损失会减小，信号的传输延迟也较 复杂，设计时需注意。通常不作为标准单元使用。

❖传输门单元多段接续时，延迟时间显著增加，一般情况下，每隔**2-4**段，插入反向器。

❖使用**BDD**传输门逻辑可以自动生成。

作业：

1. 采用BDD方法生成基于传输门的异或逻辑F=A⊕B（要求有生成步骤），并画出其版图。
2. 分别阐述PMOS传输门、NMOS传输门和CMOS传输门的特点。