Study of a Low Noise CMOS Readout Circuit for Micro Biosensor *

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Abstract :A CMOS readout circuit for biosensor that used a new Correlated Double Sampling (CDS) circuit was designed. The CDS circuit makes biosensor possible to obtain high sensitivity and low noise features. Simulation was carried out on a 0. 6μ m CMOS process by Spectre simulator. The simulation results showed that a good linear relation between input and output of the biosensor has been obtained by using CMOS readout circuit based on CDS.

Key words :biosensor; potentiostat; CDS; readout circuit EEACC :1205;2570D

一种低噪声的生物微传感器 CMOS 读出电路研究*

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摘 要:为提高生物微传感器的探测灵敏度,设计了一种低噪声的生物微传感器 CMOS 读出电路,提出了一种新型的相关双 采样(CDS)电路,对读出电路的噪声进行抑制。在 0.6 µm CMOS 工艺下,用 Spectre 仿真器对该电路进行了模拟,仿真结果表 明,采用相关双采样的 CMOS 读出电路使传感器的输入输出转换具有良好的线性关系。

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关键词:生物传感器;恒电位仪;相关双采样;读出电路

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In recent years, with the rapid development of bio-chip ,the study of biosensors developed by leaps and bounds and the study of the microarray biosensor have been discussed by many experts^[1]. The biological microelectrode is an important research tool of biosensor, which mainly produces current output, and biosensors detect and recognize the biomolecules by examining the micro-current signal forming in biologic reaction. At present, the research of biological micro-sensors read out integrated circuit (ROIC) focused on micro-current detection and signal processing technology, instead of the noise suppression of biological micro-sensors ROIC^[2-3]. In weak signal detection applications, a critical technology is the suppression of various integrated circuit induced noises, to enhance the output signal-to-noise ratio (S/N). The extent of

noise suppression usually indicates the merits of the extracted signal quality or the effect of the signal processing.

In this paper, we designed a new type of biological micro-sensor CMOS ROIC, which used correlated double sampling (CDS) circuit to suppress the noise of ROIC.

1 Biological Micro-Electrode Electrical Models

The research tool of micro biosensor is microelectrode, as opposed to conventional electrode; it has the advantages of high constant current density, high signal to noise ratio, very small time constant, low solution potential drop, etc. The polarization current of micro-electrode is usually in 10^{-9} A order of magnitude, and even down to

基金项目:Supported by Natural Science Foundation Project of CQ CSTC (2007BB2176) 收稿日期:2009-02-19 修改日期:2009-04-02 10⁻¹² A order of magnitude.

A two-electrode structure of the micro-electrode schematic^[4] shown as Fig. 1. The electrode of Si-substrate mainly consists of reaction pool, sensor pool, working electrode (WE), counter electrode (CE).

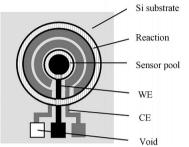


Fig. 1 Architecture scheme of micro electrode

According to Ref. [5], Fig. 2 displays a model of the R-C impedance approximation for the electrode simplified into an equivalent lumped R-C circuit component. In Fig. 2 (a), each consecutive separation of working electrode and counter electrode fingers is represented as one series R-C branch. Fig. 2(b) shows the condensed lumped R-C model.

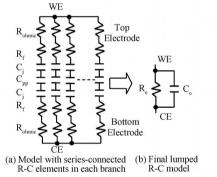


Fig. 2 R-C modeling of the micro electrode setup

2 The Structure and Working Principle of Micro-Sensor ROIC

2.1 ROIC Working Principle

ROIC consists of potentiostat current integral circuit and CDS circuit, shown as Fig. 3. With a pair of electrodes of micro-electrodes into the test solutions in a constant potential ($V_{ref} = 0.3 \sim 0.6 V$), and the micro-electrode produces an DC signal I_{in} proportional to the concentration of the solutions, charges the capacitor C_{int} through Mn and forms an integral signal V_{Cint} proportional to the sensor current signal I_{in} . In the schematic, PMOS transistor Mp is the reset transistor. We can see that the op-amp is working in negative feedback, so as to maintain the micro-electrode on a fixed bias V_{ref} , and ensure the

stability of the circuit. Put the integral signal $V_{\rm Gnt}$ into the correlated double sampling units to carry off noise, and then we can get low noise of the integral signal.

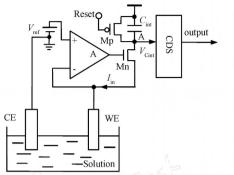


Fig. 3 Schematic of microarray biosensor unit readout circuit

2.2 Potentiostat Integral Circuit

In amp-biological micro biosensor ROIC, the potentiostat is an indispensable component. It maintains a constant voltage to ensure the electrodes for redox reactions. Meanwhile, it separates the part of sensor and readout circuit, to ensure the chemical reaction of the micro-electrode not to be effected by the part of circuit.

In the system of Fig. 3, the potentiostat consists of an op-amp A and a NMOS transistor Mn. The integral circuit contains an integral capacitor and a reset transistor Mp. The detail potentiostat integral circuit is shown as Fig. 4, the constant voltage V_{ref} is 0.5V; the amplifier is used PMOS transistors to be the difference input transistor Mp_2 and Mp_3 , which can reduce the noise 1/f in ROIC; Mp₁ is the constant current source; Mn₄ and Mn₅ is the load transistors; C₁ and two transmission gate transistors Mn7 and Mn8 make up frequency compensation circuit in common; Mp₈ and Mn₉ are common-source amplifier stage; Mp₁₀ is a reset transistor; C_2 is the integral capacitor; Mn_{11} is the potentiostat NMOS transistor; V_b is the gate voltage of Mp1 and Mp8; constant current source I_0 , resistance R_0 and capacitor C_0 are the contents of the model of the micro-electrode.

The opening loop gain of the op-amplifier is:

$$A = \frac{2 g_{m2} g_{m8}}{I_1 I_8 (3 + 5) (8 + 9)}$$
(1)

where g_{m2} and g_{m8} are the transconductances of the Mp₂ and Mp₈, I_1 and I_8 are the currents of the constant current source Mp₁ and Mp₈, respectively; is the channel length modulation coefficient.

The unity gain bandwidth of op-amplifier is:

$$\mathbf{GB} = g_{m2}/C_1 \qquad (2)$$

The amplifier is two-stage amplifier, in which

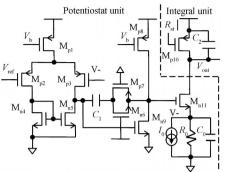


Fig. 4 The integral circuit of potentiostat

capacitor and transmission gate is used to regulate the frequency and phase margin of the amplifier and to ensure a good performance of the amplifier. In a case of 2pF load, an open-loop gain of 71.6 dB, unity-gain bandwidth of 24.6 MHz, and phase margin of 60 °were obtained, its power dissipation is only 0.12mW except bias circuit.

2.3 Noise Analysis of ROIC

In a micro biosensor ROIC, the noise may originates from environment, or ROIC itself. The major sources of noise are inherent noise of the device used in ROIC, and an additional noise induced by the circuit structure and operation modes of circuit. In ROIC, MOS is the major noise source of the device^[6]. There are three kinds of noise in RO-IC as follows:

(1) MOS transistor flicker noise which exists in all active devices, induced by the material surface situation and PN junction leakage current, that is 1/f noise. The flicker noise is more easily modeled as a voltage source in series with the gate and roughly given by^[7]:

$$\overline{V_{1/f}^2} = \frac{K}{C_{\alpha x} WL} \frac{1}{f}$$
(3)

where K is a process dependent constant on the order of 10^{-25} V² F. C_{ax} is unit area gate oxide capacitance; f is the frequency of transistors. The noise spectral density is inversely proportional to the frequency, flicker noise is also called 1/f noise. In the same channel size, the noise 1/f of PMOS transistor is usually lower than that of the NMOS transistor.

(2) The reset noise KTC induced by circuit structure and operation mode of the circuit, whose value of squared voltage is^[8]

$$\overline{V_N^2} = \frac{KT}{C} \tag{4}$$

Because of $V_N = Q/C = nq/C$, the equivalent electron number produced by *KTC* noise is :

$$n = \sqrt{KTC}/q \tag{5}$$

where K is Boltzmann constant, T is temperature, C is head amplifier input capacitance (the total sum of capacity values, that involve the integral capacitance and parasitic capacitance in the integral amplifier), Q is the two-terminal quantity of electricity of C,q is electronic charge.

(3) Material and deviation of micro-electrode formed size caused by manufacture process can bring a constant deviation noise. Its effect could be illustrated by oxygen dissolved micro-electrode, which is the most common current micro-electrode, and the output current is given by^[9]:

$$I_{in} = \frac{nFAS_m D_m P_{o_2}}{Z_m}$$
(6)

where *n* is number of electrons involved in the reduction reaction, *F* is Faraday constant, *A* is cathode area, P_{O_2} is oxygen partial pressure, Z_m is membrane thickness, and S_m and D_m are solubility coefficient and diffusion coefficient of oxygen in the membrane, respectively. We could see that the micro-electrode output current I_m is relative to micro-electrode manufacture, and the material fabrication deviation could bring relating noise to ROIC.

2.4 Correlated Double Sampling Circuit Design

In ROIC, CDS technology is the most successful technology to restrain noise. The CDS could reduce the 1/f noise and KTC noise of $ROIC^{[10]}$. In this paper, we proposed a novel CDS circuit, to reduce the noise of micro biosensor ROIC.

The CDS circuit is shown as Fig. 5. The transmission gate of MOS transistor Mp12 and Mn13 are the sampling switch of CDS unit, and the complementary signal of Sample and Sample ~ are CDS sampling pulse; C_3 is the capacitor stabilizing voltage A; C₄ is the holding capacitor of CDS; Mn₁₄ is output voltage clamping transistor, and Rst is clamping pulse used to multiplexing with integral pulse; the source follower consisting of Mp15 and Mp16 is the output stage of CDS, and Vb1 is the gate voltage of Mp15; C5 is output load capacitor. The CDS circuit in Literature[11] is isolated from the front circuit by N source follower, sampled by a NMOS transistor switch, and the PMOS clamping transistor connects with power supply, whose output is a N source follower. In the Fig. 5, used transmission gate as the sampling switch between the integral unit and sampling unit instead of source follower, whose sample will not miss threshold voltage, voltage A can have a great dynamic range; an NMOS transistor was used as the clamping transistor, and source follower con-

778

sists of PMOS transistors, so 1/f noise lower in the circuit; in Ref. [12], the switch of complementary time sequence is achieved by a inverter, and the inverter is in the circuit of CDS. The inverter was used in the time sequence circuit in this design instead of that in CDS to save the layout area in micro-array; the clamping pulse multiplexes with the integral pulse, so as to cut out the digital clock circuit.

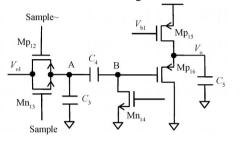


Fig. 5 Circuit diagram of the correlated double sample unit

Set Rst to high level and turn on Mn_{14} . When integral signal achieved, the signal Sample turns off the transmission gate at the moment T_1 . And then, the voltages of capacitor C_4 are:

$$V_1(T_1) = V_{ref} + V_{Gat} + V_{noise}$$
(7)

$$V_2(T_1) = 0$$
 (8)

At the moment T_2 , Rst is in low level, Mn_{14} is turned off. Sample turns on the transmission gate, the reset signal Rst reset the integral capacitor to V_{dd} , voltage $V_2(T_2)$ is send to P source follower unit, at the moment,

$$V_1(T_2) = V_{dd} + V_{ref} + V_{noise}$$
 (9)

According to the principle of charge conservation, the charge of the coupling capacity C_4 could not change abruptly, so:

$$C_{S}(V_{1}(T_{1}) - V_{2}(T_{1})) = C_{S}(V_{1}(T_{2}) - V_{2}(T_{2}))$$
(10)
The output signal $V_{2}(T_{2})$ of CDS is:

 $V_{2}(T_{2}) = V_{1}(T_{2}) - V_{1}(T_{1}) + V_{2}(T_{1}) = (V_{dd} + V_{ref} + V_{noise}) - (V_{ref} + V_{Cint} + V_{noise}) = V_{dd} - V_{Gint}$ (11)

The equation shows that the noise signal V_{noise} is neutralized by CDS circuit, the output signal V_2 is just that V_{dd} subtracts integral signal V_{Cint} . Thus CDS circuit could reduce the noise of ROIC effectively.

Furthermore, this CDS circuit has the advantage of simple structure; fewer transistor and low power consumption, etc.

3 Simulation Results

The ROIC design based on 0. 6 μ m CMOS technical BSIM3V3 model, which used Spectre emulator of Cadence to simulate. The circuit used single 5 V source to supply power, the integral capac-

itance C_2 is 2 pF, the constant capacitance C_3 is 2 pF, and the CDS holding capacitance C_4 is 0.8 pF. The timing of circuit is shown as Fig. 6, the integral time is 350 μ s, and the sampling time is 340 μ s.

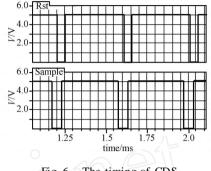
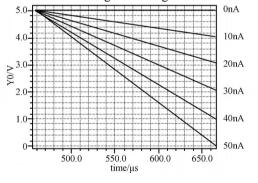
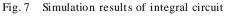


Fig. 6 The timing of CDS

The output current of biosensor is $0 \sim 50$ nA, and 10 nA per step. The parameter sweep of integral voltage signal of integral capacitor C₂ is shown in Fig. 7, in which results show a good linearity, and the output voltage signal of integral capacitor has a great dynamic range $(0 \sim 5 \text{ V})$; in the Ref. [13], the output wave of simulation have no uniformly-spaced effect, no obvious effect. The simulation results of CDS circuit of Fig. 5 is shown in Fig. 8, the output is square wave, and the output changed almost synchronizes to the input signals. This shows that the CDS holding circuit has a good responsiveness to integral voltage.





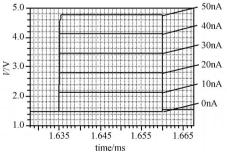


Fig. 8. Simulation results of CDS

The table 1 showed a relation between output and input of tradition sampling circuit and CDS circuit.

780

Table1 The relation between output and input of tradition sampling circuit and CDS circuit

$V_{o}\left(V ight)$	I(nA)					
	0	10	20	30	40	50
Tradition	1.296	1.950	2.636	3.302	3.956	4.613
CDS	3.743	3.094	2.389	1.705	1.050	0.458

The curvilinear equation between input and output of table 1 is analyzed by cubic polynomial fitting method using Matlab:

 $V_{O1} = 0 \cdot I^3 - 0.0003 \cdot I^2 - 0.0629 \cdot I + 3.7449$ (12) $V_{O2} = 0 \cdot I^3 + 0.0001 \cdot I^2 + 0.0649 \cdot I + 1.4755$ (13) where *I* is the output current of biosensor, V_{O1} and V_{O2} are output voltage of tradition sampling circuit and CDS circuit of ROIC. From the above equation, it is easy to know that the CDS fitted curve is more likely a straight line, and the output transfer voltage of micro biosensor ROIC presents a good linear relationship at the range of 0 to 50 nA of biological current, a wide dynamic response range and an output swing of greater than 3 V are also obtained.

4 Conclusion

Based on 0.6 µm CMOS technique, designed a new ROIC for micro biosensor, and analyzed its every module. In order to suppress the noise of micro biosensor in CMOS ROIC and improve the quality of biological detection, a novel CDS circuit was proposed. The simulation results by Spectre show that the circuit can reduce noise as normal CDS circuit. And the CDS circuit also has many other advantages such as simple structure, fewer transistors etc. It can be used for micro biosensor and will have a good utility value.

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