An Accurate CMOS Temperature Sensor with a CDS Circuit*

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Abstract: This paper presents a novel accurate CMOS temperature sensor with a correlated double sampling (CDS) circuit designed, and simulated for thermal testing and monitoring chips in CMOS technologies. In this design, a nine-MOS-transistor temperature sensor's output current, which includes temperature characteristic integrated by a capacitor, the integral voltage signal is sent to a CDS circuit to eliminate kTC noise and reduce $1/f$ noise of the circuit. The new temperature sensor is compatible with standard CMOS technologies, and the simulation results show its good performances.

Key words: CMOS temperature sensor; current integration circuit; CDS

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一种采用 CDS 电路的高精度 CMOS 温度传感器*

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摘 要: 采用相关双采(CDS)电路, 设计了一种新颖的高精度温度传感器, 该温度传感器可用于 CMOS 集成电路的过温检测。传感器的温度感应部分仅采用 9 个 MOS 管, 其输出的包含温度信息的电流信号通过一个电容进行积分, 随后采用 CDS 电路对积分信号进行消除 kTC 噪声和降低 $1/f$ 噪声处理, 并同时进行采样处理, 得到与温度成正比的电压信号。该新型温度传感器与标准 CMOS 工艺兼容, 且仿真结果表明其具有较高的性能。

关键词: CMOS 温度传感器; 电流积分电路; CDS

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A temperature sensor is an essential unit in many integrated circuits (ICs), especially in power devices and power or thermal management chips. A large variety of temperature sensors have been developed to match these technical requirements. In the last couple of years CMOS temperature sensors have become increasingly popular because of rapid steady growth of IC industry and the necessity of effective thermal management in the power hungry and management circuits[1]. The basic and the most popular temperature sensor is the bipolar junction transistor (BJT) which can be used as a temperature sensor when operated in a diode configuration, and can be realized in most of the CMOS processes[2-5].

In the BJT solution, the base-emitter junction of a substrate PNP transistor is usually used as a conventional thermal diode whose collector is connected to the ground in CMOS processes. The base-emitter voltage V_{be} of a bipolar transistor decreases almost linearly with temperature. The temperature coefficient is approximately 2 mV/℃[1]. Figure 1 shows the conventional structure of integrated CMOS temperature sensors by using PNP transistors as thermal diodes, and the output voltage V_{out} can be calculated as follows:

$$V_{out} = V_{be2} + \frac{KT}{q}\ln n\left(1+\frac{R_2}{R_3}\right) \quad (1)$$

Where K is Boltzmann's constant, T is the absolute temperature in Kelvin, q is the elementary electric charge and n is the emitter current density ratio of Q_2 and Q_1. Obviously, there is a linear relationship between the obtained voltage V_{out} and the temperature T by choosing appropriate values of n, R_2 and R_3.

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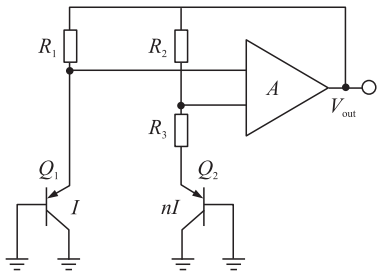

Fig. 1 Conventional Structure of Integrated CMOS Temperature Sensor

However, in this structure, the offset voltage of amplifier A will cause large errors.

As for temperature sensors, the quality of the lateral bipolar transistor depends heavily. In many processes, especially when no attention has been paid to optimize this device, the current gain of this transistor is very low (< 5) and the leakage current toward the substrate (via the parasitic vertical bipolar) is difficult to control; and for the vertical bipolar substrate transistor in the temperature sensors, the quality of this transistor is comparable to transistors in standard bipolar processes. However the main problem is the lack of a free collector terminal, which is inherently connected to the substrate[6-7].

Recent researches showed that it is possible to make temperature sensors using CMOS transistors operating in weak inversion[8-10]. And this paper presents a novel in-chip temperature sensor solution with CMOS transistors. A correlated double sampling (CDS) circuit is designed which can eliminate kTC noise and reduce $1/f$ noise of the sensor.

1 Circuit Design and analysys

1.1 Nine-Transistor Temperature Sensor

The new nine-transistor temperature sensor is shown, exclusive of the CDS circuit, is shown in Fig. 2. Mp1 ~ Mp4 and Mn1 ~ Mn5 constitute a nine-transistor temperature sensor, and the four P channel MOS transistors Mp1 ~ Mp4 constitute a cascade current mirror. The current of N channel MOS transistors Mn1 is mirrored to transistors Mn2 and Mn3. This temperature sensor utilizes the temperature dependence of two parameters of the MOS transistor, namely, the threshold voltage V_{TH} and the gain factor β. These dependencies are on the order of[8-9]

$$\partial V_{TH}/\partial T \approx -1.8\ \text{mV/K} \tag{2}$$

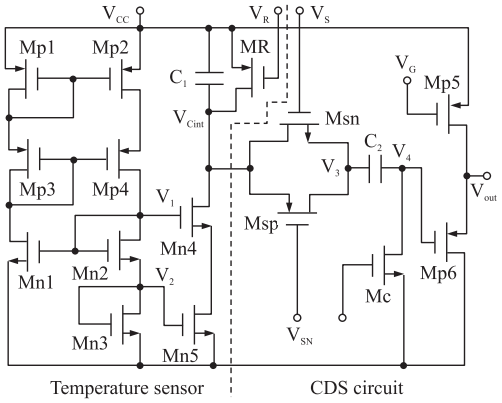

Fig. 2 Schematic of Proposed Temperature Sensor

$$\frac{1}{\beta}\cdot\frac{\partial\beta}{\partial T}\approx -0.5\%/\text{K} \tag{3}$$

$$\beta=\mu C_{ox}(W/L) \tag{4}$$

Where μ is carrier mobility (for PMOS the carrier is hole $\mu=\mu_p$ and for NMOS the carrier is electron $\mu=\mu_n$), C_{ox} is the gate oxide capacitance per unit area, W is the transistor width, and L denotes the transistor effective channel length.

The output voltage of node V_1 and V_2 can be expressed as follows:

$$V_1=V_{TH}\left(1+\frac{\lambda_{p12}}{\lambda_{p12}-\lambda_{n13}-\lambda_{n14}}\right) \tag{5}$$

$$V_2=V_{TH}\left(1+\frac{\lambda_{n13}}{\lambda_{p25}-\lambda_{n13}-\lambda_{n14}}\right) \tag{6}$$

Where λ_{pij} and λ_{nij} are determined by the ratio between the gate sizes of the transistor pair of PMOS and NMOS, respectively.

$$\lambda_{pij}=\sqrt{\frac{W_{pi}/L_{pi}}{W_{pj}/L_{pj}}};\lambda_{nij}=\sqrt{\frac{W_{ni}/L_{ni}}{W_{nj}/L_{nj}}} \tag{7}$$

The voltage V_1 controls the gate of the transistor Mn5 yielding a drain current[12-13] of

$$I_1=\beta_{n5}\cdot V_{TH}^2\cdot\left(\frac{\lambda_{n13}}{\lambda_{p25}-\lambda_{n13}-\lambda_{n14}}\right)^2=\beta_{n5}\cdot V_{TH}\cdot\text{const} \tag{8}$$

$$\beta_{n5}=\mu_n C_{ox}(W_{n5}/L_{n5}) \tag{9}$$

The characteristic of equations (8) and (9) show that the output current is proportional to the temperature. The I_1 current of the nine-MOS-transistor analogue sensor discharges the capacitor C_1. So the voltage drop V_C on the capacitor C_1 and the voltage of node V_{Cint} yield by I_1 are follows, respectively:

$$V_C=\int_0^t I_1\,\mathrm{d}t/C_1 \tag{10}$$

$$V_{Cint}=V_{CC}-V_C=V_{CC}-\int_0^t I_1\,\mathrm{d}t/C_1 \tag{11}$$

Then, the voltage single is send to the CDS circuit.

1.2 CDS Circuit

CDS is a widespread noise reduction method for discrete-time output signals[11]. Schematic view of CDS is shown in Fig. 3[14]. At time T_1, by activating the switch S_1, the first sample (sample1) is taken and the sampled signal is stored on the sampling capacitor C_{S1}. And, at time T_2, switch S_2 is activated and a new signal (sample2) is sampled and stored on capacitor C_{S2}.

Sample1 retains information about $1/f$ noise and kTC noise. Sample2 contains both the available signal, and $1/f$ noise, kTC noise. Then the differential amplifier subtracts these two sampled signals eliminating common noise components from the available information signal.

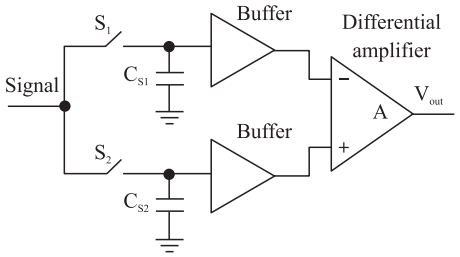

Fig. 3　Schematic View of CDS

The proposed CDS circuit is shown in Fig. 2. The NMOS transistor Msn and the PMOS Msp constitute a CMOS transmission gate, C_{S2} is a CDS capacitor, NMOS Mc is a clamp transistor and PMOS Mp5 and Mp6 constitute a common-source amplifier. The CDS function is described below.

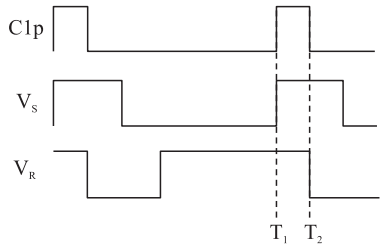

Fig. 4　Timing of CDS

Fig. 4 shows the timing of CDS circuit. At time T_1, the sample clock V_S and the clamping clock Clp are high and the clamp transistor Mc is ON. The first sampled voltage signal is charged on the CDS capacitor C_{S2} and the voltages of node V_3 and V_4 at time T_1 are:

$$V_3(T_1) = V_{\text{Cint}} + V_{\text{noise}} \tag{12}$$

$$V_4(T_1) = 0 \tag{13}$$

where V_{noise} is sum of $1/f$ noise and kTC noise of the circuit.

At time T_2 the clamp device Mc is turnnig OFF before the internal integration capacitor C_1 is reset. Then the second sampled voltage signal of node V_3 becomes:

$$V_3(T_2) = V_{\text{noise}} \tag{14}$$

since the charges on the ac coupling capacitor C_2 are the same at time T_1 and T_2. From (12) ~ (14), we have:

$$C_{S2}[V_3(T_1) - V_4(T_1)] = C_{S2}[V_3(T_2) - V_4(T_2)] \tag{15}$$

Thus, the output signal of node V_4 after the CDS is:

$$V_4(T_2) = (V_{\text{Cint}} + V_{\text{noise}}) - V_{\text{noise}} = V_{\text{Cint}} \tag{16}$$

Then the voltage signal $V_2(T_2)$ is sent to the common-source amplifier.

2 Simulation and analysys

The simulation results in 0.6 μm CMOS process of node V_{Cint} and V_{out} are shown in Fig. 5 and Fig. 6, respectively. The temperature is from 0 ℃ to 160 ℃ with delta = 20 ℃.

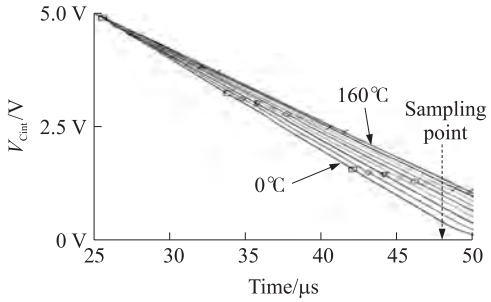

Fig. 5　Simulation Result of node V_{Cint}

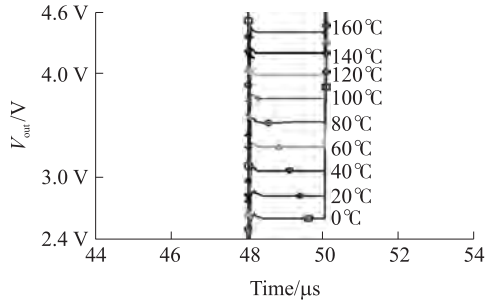

Fig. 6　Simulation Result of node V_{out}

Fig. 7 shows the characteristics of output voltage V_{out} with temperature T from simulation results with temperature from 0 ℃ to 160 ℃, delta = 20 ℃. Formula (17) is a fitting function of output voltage V_{out}

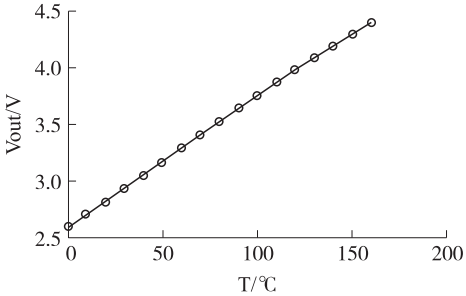

Fig. 7　Characteristics of V_{out} with Temperature

with temperature T. And it indicates that there is a good linear relationship between V_{out} and the temperature T in the range of 0 ℃ to 160 ℃.

$$V_{out} = -8.598\times10^{-8}T^3 + 1.622\times10^{-5}T^2 + 0.01086T + 2.594 \quad (17)$$

Table 1 shows the brief view of the proposed temperature sensor, and it has a wide temperature range, a high temperature coefficient and low power consumption. Another advantage of the sensor is it can be fabricated in CMOS process.

Table 1 Performance of the sensor

Supply voltage	Power consumption	Temperature coefficient	Temperature range	Process
5V	140 μW	11.25 mV/℃	0-160 ℃	CMOS

3 Conclusions

A novel accurate CMOS temperature is proposed in this paper. The CMOS temperature sensor consisted mainly of 2 parts: a nine-MOS-transistor temperature sensor and a CDS circuit. The MOS transistors can overcome bipolar transistor's shortcomings and the CDS circuit can eliminate kTC noise and reduce 1/f noise.

The CMOS temperature sensor is analyzed and verified by simulation. The simulation results show the sensor has a high temperature coefficient and the output voltage has a good linear relationship with the temperature. The proposed temperature sensor can be fabricated in standard CMOS process without using PNP bipolar transistors.

References:

[1] Florin Udrea, Sumita Santra, Julian W Gardner. CMOS Temperature Sensors-Concepts, State-of-the-Art and Prospects [C]// Semiconductor Conference, CAS 2008. International Issue Date: 13-15 Oct. 2008; 31-40.

[2] Omar Fathy, Ahmed Abdallah, Amr Wassal, et al. Counter Based CMOS Temperature Sensor for Low Frequency Applications[C]// Thermal Issues in Emerging Technologies Theory and Applications (ThETA), 2010 3rd International Conference, 2010: 103-109.

[3] André L Aita, Kofi A A Makinwa. Low-Power Operation of a Precision CMOS Temperature Sensor Based on Substrate PNPs [J]. Sensors, 2007: 856-859.

[4] 林摇荣, 蔡摇敏, 黄伟朝, 等. 新型低功耗 CMOS 片上温度传感器设计[J]. 传感技术学报, 2011, 24(7): 981-985.

[5] Bakker A, Huijsing J H. Micropower CMOS Temperaturesensor with Digital Output [J]. IEEE J Solid-State Circuits, 1996, 31(7): 933.

[6] Pertijs M, Niederkorn A, Ma X, et al. A CMOS Temperature Sensor with a 3σ in Accuracy of ±0.5 ℃ from -50 ℃ to 120 ℃. IEEE International Solid-State Circuits Conference (ISSCC), 2003: 1: 200.

[7] Bianchi R A, Karam J M, Courtois B, et al. CMOS-Compatible Temperature Sensor with Digital output for Wide Temperature Range Applications. Microelectronics Journal, 2000: 31: 803.

[8] Masahiro Sasaki, Makoto Ikeda. A Temperature Sensor with an Inaccuracy of -1 = +0.8 C using 90-nm 1-V CMOS for Online Thermal Monitoring of VLSI Circuits [J]. Semiconductor Manufacturing, IEEE Transactions, 2008, 21(2): 201-208.

[9] Vladimir SzCkely, Cs MBrta, Zs Kohki, et al. CMOS Sensors for on-Line Thermal Monitoring of VLSI Circuits[J]. Very Large Scale Integration(VLSI) Systems, IEEE Transactions, 1997, 5(3): 270-276.

[10] Chen Zhao, Jun He, Sheng-Huang Lee, et al. A Linear Differential Output of Threshold-Based CMOS Temperature Sensor with Enhanced Signal Range[C]//Circuits and Systems(MWSCAS), 2010 53rd IEEE International Midwest Symposium, 2010: 316-319.

[11] Chen Xu, Shen Chao, Mansun Chan. A New Correlated Double Sampling(CDS) Technique for Low Voltage Design Environment in Advanced CMOS Technology[J]. Solid-State Circuits Conference, ESSCIRC Proceedings of the 28th European, 2002, 9: 117-120.

[12] 曹新亮, 余宁梅, 卫秦啸. 集成 CMOS 温度传感器设计、实现和测试[J]. 传感技术学报, 2010, 23(1): 38-42.

[13] Vladimir SzCkely, Cs MBrta, Zs Kohki, et al. CMOS Sensors for on-Line Thermal Monitoring of VLSI Circuits[J]. Very Large Scale Integration(VLSI) Systems, 1997, 5(3): 270-276.

[14] Rankov A, Rodriguez-Villegas E, Lee M J. A Novel Correlated Double Sampling Poly-Si Circuit for Readout Systems in Large Area X-Ray Sensors[J]. Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium, 2005, 1: 728-731.

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