有晶化时间的高可控性和工艺过程的高稳定性，故而适合于工业化生产的要求。利用些技术，当温度为 590 ℃时，可将晶化时间缩短至 2 h 之内。用这种多晶硅薄膜为有源层，所得多晶硅 TFT 的场效应迁移率典型值为～55 $cm^2/V \cdot s$，亚阈值斜摆幅为 0.6 V/dec，开关电流比为～1×10^7，开启电压为－3 V。

关 键 词：金属诱导晶化；规则排列连续晶畴；薄膜晶体管；低温多晶硅

中国分类号：$TN321^+.5$ **文献标识码**：A

1 Introduction

Low temperature crystallization of amorphous silicon (a-Si) thin film has attracted extensive attention because of its potential applications to large area electronics on inexpensive glass substrates. Thin-film transistors (TFTs) manufactured on metal-induced unilateral crystallized (MIUC) polycrystalline silicon (poly-Si) have been testified high carrier mobility and good device uniformity. They can be used as active-matrices[1, 2] for flat-panel display and image sensor applications [3, 4].

However, MIUC-TFT [5] has such problem as of subsequent mask misalignment induced by glass substrate shrinking during the annealing process. Additionally, residual nickel in the poly-Si channel can affect the long term stability of the TFT. The electrical performance of MIUC TFT may shift and suffer from higher off-state leakage current and drain breakdown.

There have been several attempts to reduce the Ni content in MIC-based TFT. Disk-like poly-Si silicon has been obtained by Ni-mediated crystallization of a-Si with a silicon-nitride (SiN_x) cap layer [6]. In this process, Ni was sputtered onto the SiN_x/a-Si layer and then annealed at around 600 ℃. The cap SiN_x controlled the Ni content inside the MIC layer to within tolerable levels. However, that process is quite complicated. It is also expensive because of the vacuum process involved and the requirement to remove the cap layer afterwards.

In our previous research, we have demonstrated a solution-based MIC (SMIC) process for the fabrication of poly-Si TFT [7]. The poly-Si film with low Ni content and disk-like domains has been obtained by adjusting the Ni adsorption process in the solution. Compared to physical vapor deposition (PVD) method, the SMIC process is faster, simpler and inexpensive. The problem of subsequent mask misalignment induced by glass substrate shrinkage can be eliminated with these new technologies, but the random distribution of crystalline nuclei leads to longer annealing time, which is not desirable for large area glass substrate.

In this paper, a new scheme which can reduce residual nickel in poly-Si and precisely control the annealing process has been proposed. It can be realized with the combination of solution processing and the provision of the nucleation sites (NS) and the supplemental sites (SS). As a result, the crystallized poly-Si film has very low nickel concentration. The entire film is available for making high performance TFTs. Different shape domains can be acquired. Among the optimal designs, a honeycomb-like structure and a unidirectional structure are the most typical and practical.

In case of the repeatedly regular distribution of the nucleation sites and the supplemental sites, the domains of the same shape and size can be realized. This process is precisely controllable and the crystallization time can be reduced to about 2 h at 590 ℃. The fabricated P-Channel TFTs using the poly-Si films as active layer show high performance.

2 Defined-Grain Poly-Si Material

2.1 Preparation of defined-grain (DG) poly-Si

Eagle 2000™ glass covered with 300 nm PECVD silicon oxide was used as the initial substrate in these experiments. 50 nm a-Si was

deposited by low-pressure chemical vapor deposition (LPCVD). Nucleation sites (NS) and the supplemental sites (SS) were defined by photolithography. After removal of the native oxide on the a-Si surface, the samples were immersed in the $Ni(NO_3)_2/NH_4OH$ mixture solution for 12 min. The cross section schematic of the sample after immersion in solution is shown in Fig. 1. As seen from Fig. 1, only a little part of the a-Si was exposed to the solution, and most of it was covered with native oxide and the photoresist on it. After soaking in the mixture solution to obtain a certain quantity of the nickel as inducing metal, the photoresist was removed. Then the samples were annealed at 590 ℃ for 2 h in a controlled environment.

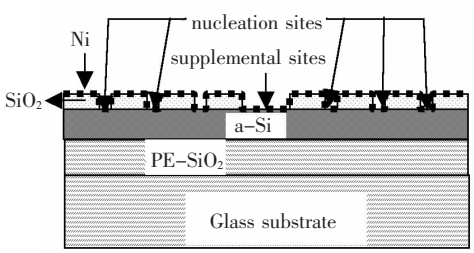

Fig. 1 Schematic of cross section of the sample after immersing in $Ni(NO_3)_2$/ NH_4OH mixture

2.2 DG poly-Si analysis

The key technology to get high quality defined-grain (DG) poly-Si is the combination of solution process and the provision of the nucleation sites (NS) and the supplemental sites (SS). The different arrangement of the NS and the SS can results in different shapes and sizes of grains. The optimal designs are honeycomb-like grain and unidirectional grains.

Fig. 2 are the layouts of the honeycomb-like grain poly-Si (HG-PS). The SS are defined in squares with size of 4 μm×4 μm and uniformly distributed around the NS. The distance between the SS is 8 μm. The hexagons NS sizes are 15 μm (a), 10 μm (b), 5 μm (c) and 4 μm (d). After forming the NS and SS formation, these samples were immersed in $Ni(NO_3)_2/NH_4OH$ mixture solution mentioned in 2.1 section. Then crystallization was carried out at 590 ℃ for 2 h in nitrogen ambient.

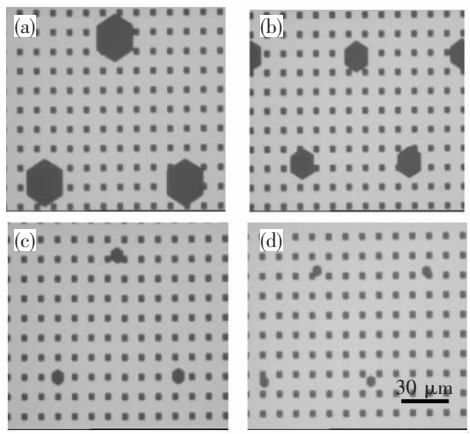

Fig. 2 Layout for forming honeycomb-like grain poly-Si. (a) 15 μm; (b) 10 μm; (c) 5 μm; (d) 4 μm.

Fig. 3 shows optical microscope photos of the HG-PS etched by tetra-methyl ammonium hydroxide (TMAH). As mentioned above, the SS are defined in squares in size of 4 μm×4 μm and uniformly distributed around the NS. When the size of hexagonal NS is 15 μm, there will be some floc-like grains in the center of the NS in the crystallized region. (See Fig. 3(a)). As the annealing time increases, the domain grew continuously around the centers of NS, at which $NiSi_2$ crystal nuclei are supposed to be formed at the beginning of thermal annealing. It may be because a fixed amount of Ni atoms is required to form a nucleus of $NiSi_2$ that can act as the seed

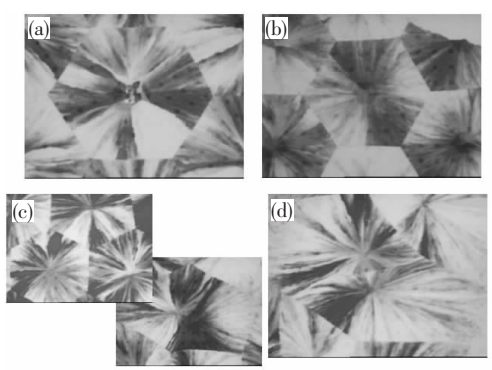

Fig. 3 Optical microscope images of the HG poly-Si film etched by TMAH. (a) 15 μm; (b) 10 μm; (c) 5 μm; (d) 4 μm.

for crystallization[6]. For a fixed immersion time in the $Ni(NO_3)_2/NH_4OH$ mixture solution, a larger NS area means more nickel is absorbed on the a-Si surface at a certain area.

When the size of the NS is 15 μm and immersion time is 12 min, much more nickel than the required amount for forming crystal nuclei is adsorbed. The superfluous nickel forms many floc-like grains in the center of the nucleation sites, as seen in Fig. 3(a). When the size of the hexagonal NS is 10 μm, perfect disk-like hexagonal domains surrounding the NS, are formed. (See Fig. 3 (b)). When size of the hexagonal NS reduced to 5 μm, perfect disk-like domains are formed too. But some of the domains do not encircle the NS, as seen in Fig. 3 (c). That means the localization of the NS is reduced when the area of the NS is smaller. Most of the domains distribute randomly when the size of the hexagonal NS reduced to 4 μm. (See Fig. 4 (d)). That is to say, when the side length of NS is 4 μm and soaking time is 12 min, the aggregated nickel at a NS is approximately as much as the nickel at a SS. So the localization function of the NS is disabled with the reducing of the area ratio of NS to SS.

Fig. 4 shows the layouts for forming the unidirectional grain poly-Si (UG-PS). The NS are rectangles, in which the length of the longer side is the same as the amorphous silicon substrate. The widths of the rectangles are 8 μm (a), 6 μm (b), 4 μm (c) and 2 μm (d). The distance between two neighboring NS is fixed at 60 μm. The SS are also defined in squares in size of 4 μm×4 μm. After forming the NS and SS, these samples were immersed into $Ni(NO_3)_2/NH_4OH$ mixture solution mentioned in 2.1 section for 12 min. The crystallization was carried out at 590 ℃ for 2 h in N_2 atmosphere.

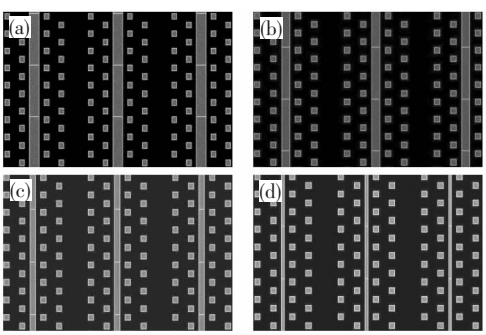

Fig. 4 Layout for forming unidirectional grain poly-Si. (a) 8 μm; (b) 6 μm; (c) 4 μm; (d) 2 μm.

Fig. 5 shows optical microscope photos of the unidirectional grain poly-Si (UG-PS) etched by TMAH. There are no floc-like grains when the width of the strip NS changes from 2～8 μm. When the widths of the strip NS are equal to or above 4 μm, MILC unidirectional grains can be obtained (See Fig. 5 (a-c)). The nucleus is formed in the NS strip at the early stages. Then during the annealing process, the grain extends in the semi-parallel direction, until fronts of the neighboring MILC domains collide and the grain boundaries formed in the center of two neighboring NS.

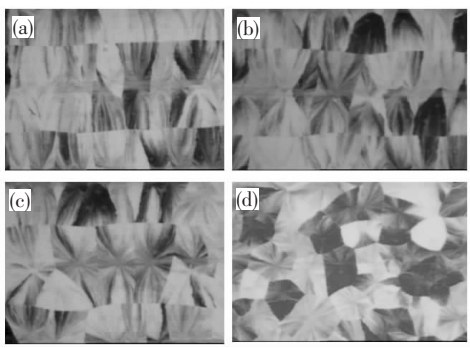

Fig. 5 Optical microscope images of the UG-PS etched by TMAH. (a) 8 μm; (b) 6 μm; (c) 4 μm; (d) 2 μm.

The poly-Si in the SS has the same orientation as the entire grain, which proves that there is not any crystalline nucleus formed there. Because the wider nucleation sites results in more nickel at a certain area, more nucleus can be formed with wider NS. The distance between two grains in the same NS is increasing with the reducing of the widths of the NS. That means the system is self-adjusted. The poly-Si consisting of disk-like domains can be easier obtained

compared to the hexagonal grain poly-Si. When the widths of the NS reduce to 2 μm, most of the domains are randomly distributed (See Fig. 5 (d)).

The smooth surface of the poly-Si is a critical factor for high performance and reliable TFT. The surface of the crystallized poly-Si is analyzed by atom force microscope (AFM). Fig. 6 shows AFM 3-D images of the defined-grain poly-Si inside and outside of NS or SS respectively. Inside means the film in that area has been exposed to the $Ni(NO_3)_2$/ NH_4OH mixture solution, while outside means that the film is protected by the photoresist and has not been exposed to the solution. The surface roughness of the inside and outside is found to be 0.364 nm and 0.189 nm, respectively. This results are much less than 13.1 nm, which is the roughness of ELA poly-Si[6].

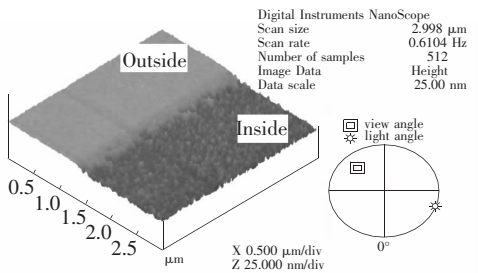

Fig. 6 AFM 3D image of the full crystallized DG-PS

3 DG Poly-Si TFT

These fully crystallized DG-PS films were patterned into active islands, and unwanted poly-Si was etched away using Freckle etchant. 50 nm low temperature oxide (LTO) was subsequently deposited by low pressure chemical vapor deposition (LPCVD) at 425 ℃ as the gate insulator after the native oxide was removed by 1% HF. Following the deposition of 300 nm metal which was patterned into gate electrodes, boron at a dose of $4\times10^{15}/cm^2$ was implanted into the source and drain region. A 500 nm LTO isolation layer was deposited and the dopants were activated at the same time. Contact holes were opened before 700 nm aluminum-1%Si was sputtered and patterned as contacts. Contact sintering was then performed in forming gas at 420 ℃ for 30 min. The schematic cross-section of a P-channel DG poly-Si TFT was shown in Fig. 7.

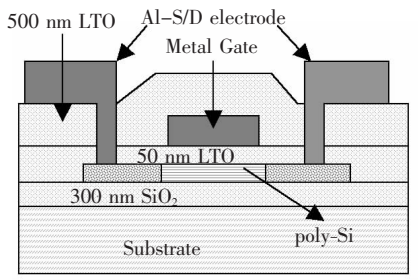

Fig. 7 Schematic cross-section of a P-channel defined-grain poly-Si TFT

Electrical characteristics of P-channel TFTs fabricated on 50 nm DG poly-Si were measured with HP4156 semiconductor parameter analyzer. Transfer characteristic curves were measured for TFTs with $W/L=30$ μm/10 μm. W and L denote the width and length of the transistor respectively. The threshold voltage (V_{th}) are defined as the V_g required to induce an I_d of $W/L\times10^{-7}$ A at $V_{ds}=-5$ V. The field-effect mobility (μ_{FE}) at low drain voltage is given by:

$$\mu_{FE}=\frac{Lg_m}{WC_{ox}V_{ds}}$$

where W and L are the channel width and length, g_m is the transconductance, C_{ox} is the gate insulator capacitance per unit area, V_{ds} is the voltage between drain and source. The reported field-effect mobility is the maximum value measured.

Fig. 8 shows the transfer characteristics of honeycomb-like grain (HG) and unidirectional grain (UG) poly-Si TFTs and their field effect mobility. The P-channel DG poly-Si TFTs exhibited a maximum field effect mobility (μ_{FE}) of ~55 $cm^2/V\cdot s$, a subthreshold swing (S) of ~0.6 V/dec and a threshold voltage (V_{th}) of −3 V. The ratio of on-state to off-state drain currents is $\sim1\times10^7$.

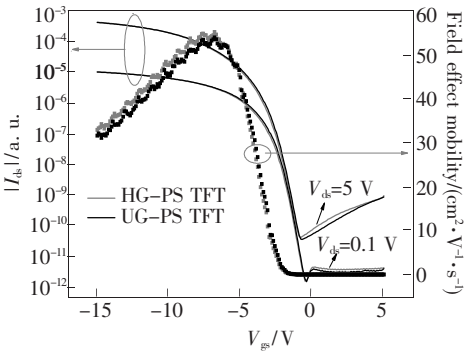

Fig. 8 Drain current and field-effect mobility *vs*. gate voltage of P-type TFTs fabricated with defined-grain poly-Si as active layer.

4 Conclusion

A new implementation scheme is presently proposed to control the grain boundaries and domains of low temperature poly-Si (LTPS) films. It can be realized by combination of the solution processing and the provision of the nucleation sites and the supplemental sites. With this new technology, different shapes of domains can be obtained due to the different distribution of the nucleation sites and supplemental sites. In this paper, a honeycomb-like grain and a unidirectional grain structure were introduced in detail. The crystallization time can be reduced to about 2 h at 590 ℃. The fully crystallized DG poly-Si film shows good surface roughness. The resulting P-channel TFTs using the DG poly-Si films as active layer show good performance.

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