半导体器件物理

The Physics of Semiconductor Devices

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Ch1 PN junction diode

- 平衡PN结定性分析
- 平衡PN结定量分析
- 理想PN结直流伏安特性
- 实际特性与理想模型的偏离
- PN junction AC characteristics ⇒
- PN junction transient behavior
- PN junction breakdown

Theoretic analysis

Conductance

Diffusion capacitance

Depletion capacitance

Equivalent circuit

1、 Theoretic analysis （8.2.2）

(1)、model

If the applied voltage is

$$V = V_0 + v(t) = V_0 + V_1 e^{j\omega t}$$

where V_0 is the DC voltage, and $V_0 >> kT/q$

V_1 is the amplitude of the AC signal，and $V_1 << kT/q$

ω is the frequency ， and $e^{j\omega t} = \cos\omega t + j\sin\omega t$

Then the current can be expressed as:

$$I = I_{DQ} + i = I_{DQ} + I_1 e^{j\omega t}$$

1、 Theoretic analysis （8.2.2）

Unlike the DC performance, in AC characterisics：

$$\frac{\Delta p}{\Delta t} \neq 0$$

For given V_1 ， and correspondring I_1 ， the AC conductance is

$$Y = \frac{I_1}{V_1}$$

(2)、小信号条件

我们下面所讨论的“小信号”模型需满足两个条件：

(1) $V_1 << kT/q$，（2） $\omega\ \tau<<1$。

1、 Theoretic analysis （8.2.2）

(3)、Conclusin

Small signal conductance

$$g_d = \frac{q}{kT} I_{DQ}$$

capacitance

$$C_d = \frac{q}{2kT}(\tau)(I_{DQ})$$

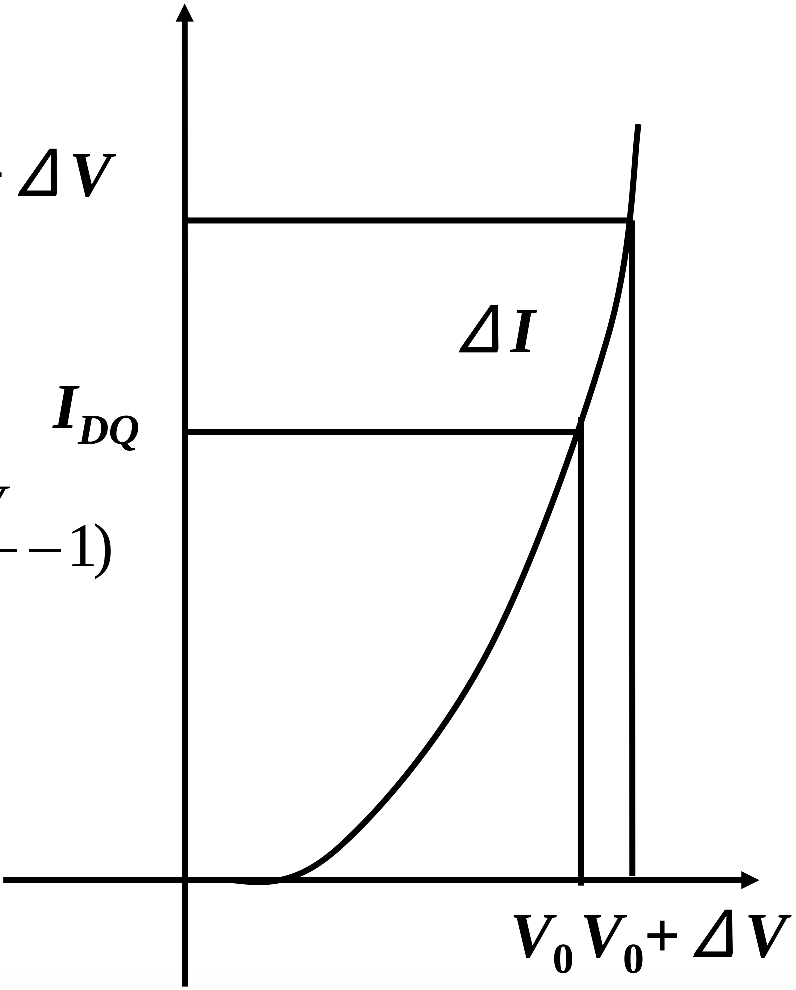
2、Conductance（8.2.1）

(1) the expression of the current increment

If the voltage increases from V_0 to $V_0 + \Delta V$

$$\Delta I = I_s \exp[\frac{q(V_0 + \Delta V)}{kT}] - I_s \exp\frac{qV_0}{kT}$$

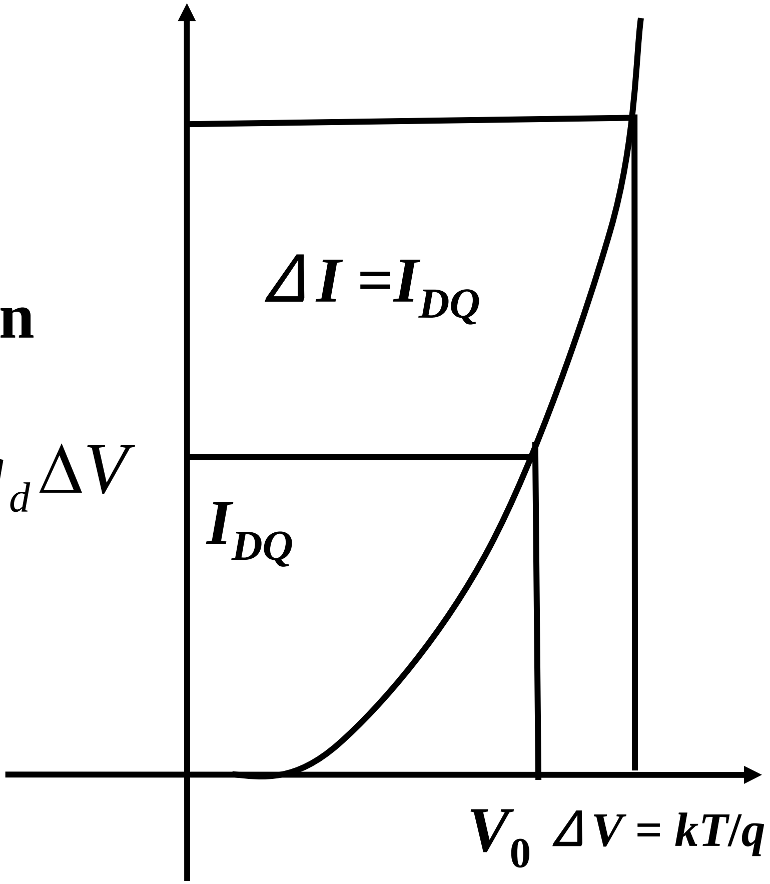
$$= I_s \exp\frac{qV_0}{kT}(\exp\frac{q\Delta V}{kT} - 1) = I_{DQ}(\exp\frac{q\Delta V}{kT} - 1)$$



注意：不管增量△V是多大，上式都成立。

2、Conductance（8.2.1）

(2) calculation of the conductance with the current increment



For small signal，$\Delta V \ll kT/q$，then

$$\Delta I = I_{DQ}(\exp\frac{q\Delta V}{kT} - 1) \approx I_{DQ}\frac{q\Delta V}{kT} = g_d \Delta V$$

$$g_d = \frac{\Delta I}{\Delta V} = I_{DQ}\frac{q}{kT}$$

注意：推导该表达式过程中采用了小信号条件△V＜＜kT/q

若 $\Delta V = kT/q$，如果用小信号结论计算的话，则 $\Delta I = I_{DQ}$。

2、Conductance（8.2.1）

(3) Calculation of the conductance through direct differential

At high forword current $$I = I_s \exp\frac{qV_a}{kT}$$

The conductance is

$$\left.\frac{dI}{dV_a}\right|_{V_a=V_0} = \left.(I_s \cdot \exp\frac{qV_a}{kT}) \cdot \frac{q}{kT}\right|_{V_a=V_0} = I_{DQ}\frac{q}{kT} = g_d$$

2、Conductance（8.2.1）

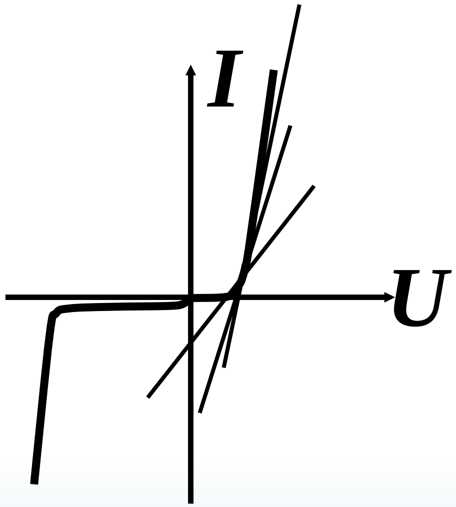
4、讨论

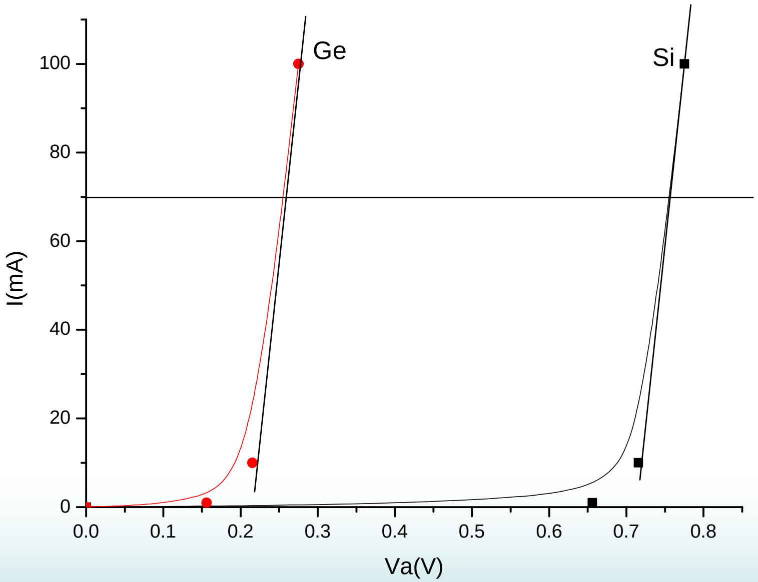
(1) $g_d=I_{DQ}q/kT$的几何解释：直流电流-电压曲线的斜率。

(2) 小信号电导只与直流工作点有关而与半导体材料无关

① 直流工作点电流增加，则交流小信号电导也随之线性增加。

② 不同材料的PN结，I_{DQ}相同处的I-V曲线切线相互平行。





3、Diffusion conductance

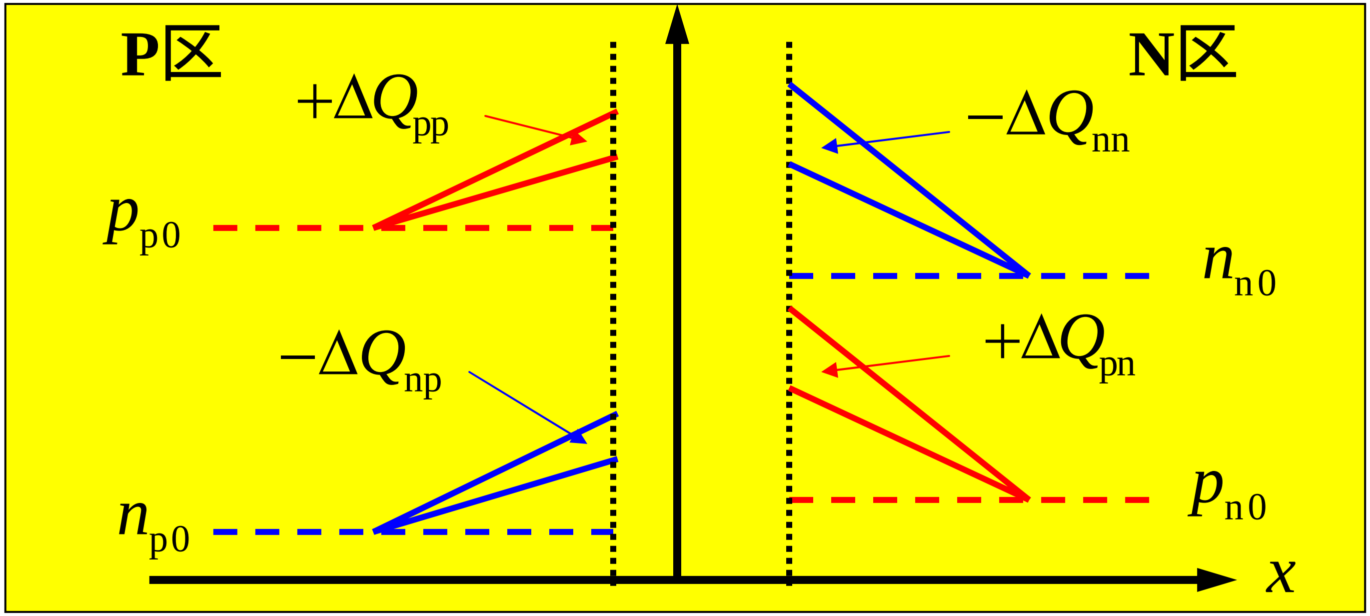
(1)、Conception

The electrostatic analysis of a p-n diode is of interest since it provides knowledge about the charge density and the electric field in the depletion region. It is also required to obtain the capacitance-voltage characteristics of the diode. A p-n diode contains two kinds of capacitance

- Depletion capacitance C_T
- Diffusion conductance C_D

3、Diffusion conductance

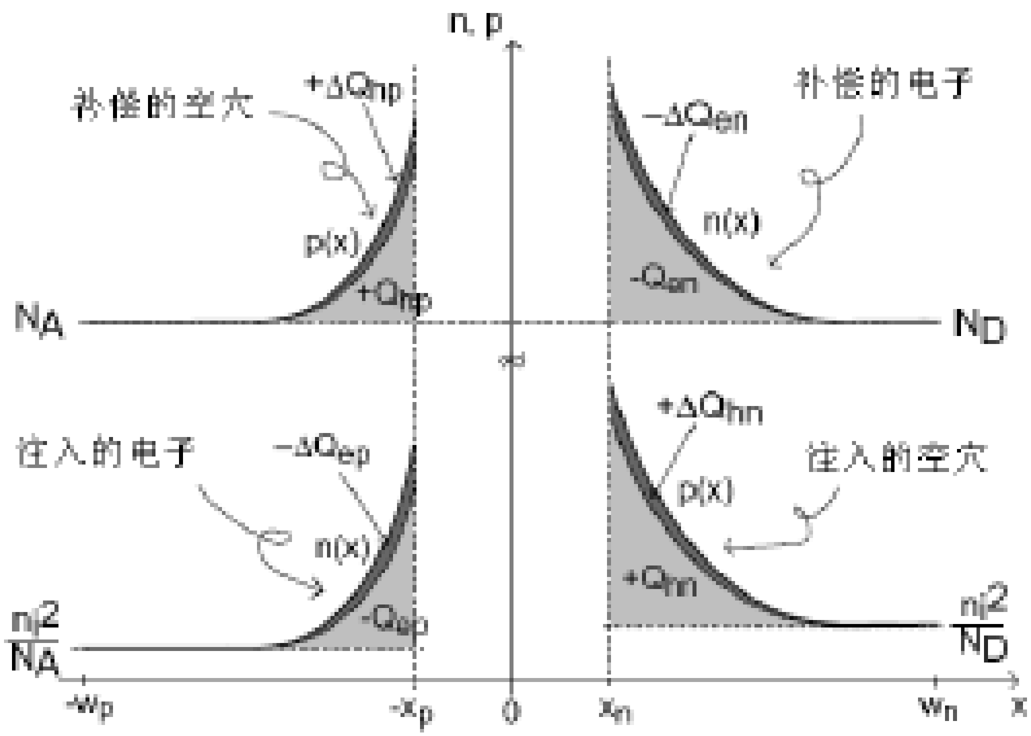
(1)、Conception



$$V_1 = \Delta V \rightarrow \begin{cases} \textbf{N region: } +\Delta Q_{pn} \textbf{ (simultaneously } -\Delta Q_{nn} \textbf{)} \\ \textbf{P region: } -\Delta Q_{np} \textbf{ (simultaneously } +\Delta Q_{pp} \textbf{)} \end{cases}$$

3、Diffusion conductance

(1)、Conception



3、Diffusion conductance

(2)、Calculation

The hole densities at the depletion region boundaries is：

$$p_n(x) - p_{n0} = p_{n0}\left[\exp(\frac{qV_a}{kT}) - 1\right]\exp(\frac{x_n - x}{L_p})$$

Charge per unit area

$$Q_p = q\int_{x_n}^{\infty}(p_n(x) - p_{n0})dx = qL_p p_{n0}\left[\exp(\frac{qV_a}{kT}) - 1\right]$$

At high forward voltage

$$Q_p = \frac{L_p^2}{D_p}J_p(x_n) = \tau_p J_p(x_n)$$

$$J_p(x_n) = \frac{qD_p p_{n0}}{L_p}\left[\exp\left(\frac{qV_a}{kT}\right) - 1\right]$$

3、Diffusion conductance

（1） N region diffusion capacitance

$$C_{dp}=\frac{dQ_p}{dV_a}=\frac{q^2}{kT}L_p p_{n0}\exp\left(\frac{qV_a}{kT}\right)=\frac{q}{kT}[J_p(x_n)\tau_p]$$

（2） P region diffusion capacitance

$$C_{dn}=\frac{dQ_n}{dV_a}=\frac{q^2}{kT}L_n n_{p0}\exp\left(\frac{qV_a}{kT}\right)=\frac{q}{kT}[J_n(x_p)\tau_n]$$

（3） total diffusion capacitance

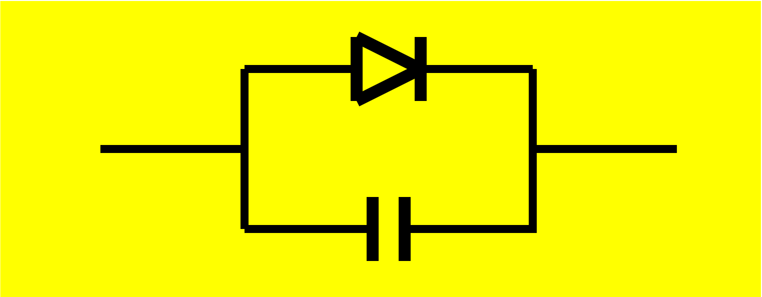
$$C_d=C_{dp}+C_{dn}=\frac{q}{kT}[J_p(x_n)\tau_p+J_n(x_p)\tau_n]$$

assuming $\tau_n=\tau_p=\tau$， then

$$C_d=(\frac{q}{kT}\cdot I_{DQ})\cdot\tau$$

4、Depletion layer capacitance

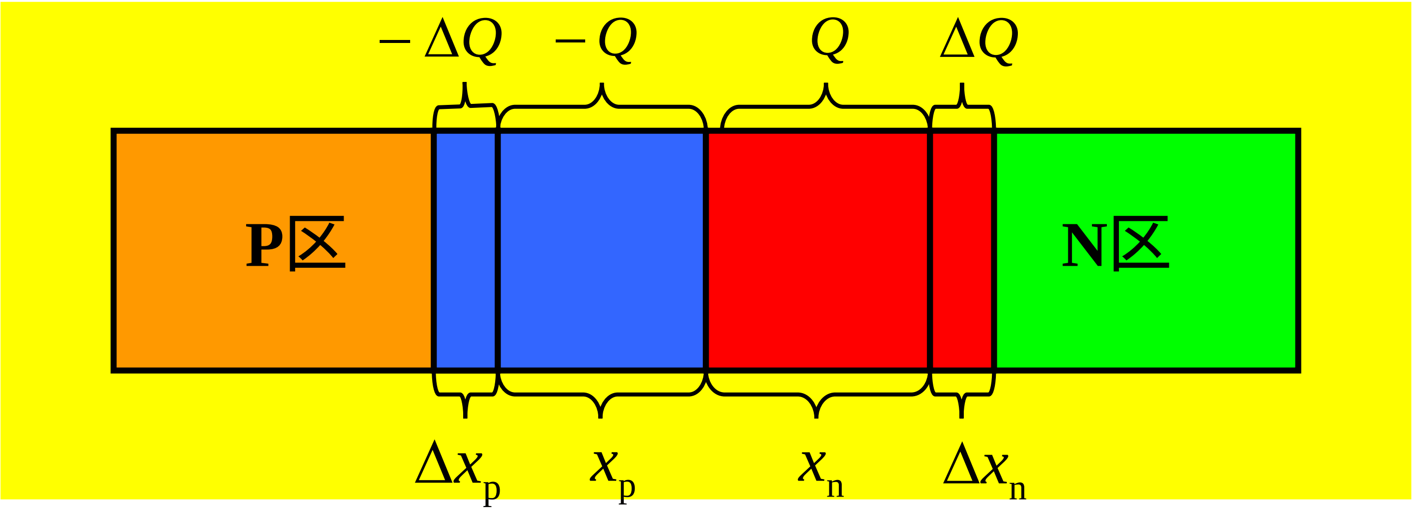
(1)、Conception



PN junction capacitance: Depletion capacitance C_T; Diffusion conductance C_D

4、Depletion layer capacitance

(1)、Conception



4、Depletion layer capacitance

(2)、Calculation

According to the comception of depletion layer capacitance

$$Q = A x_{\mathrm{n}} q N_{\mathrm{D}} = A\left(2\varepsilon_{\mathrm{s}} q N_0\right)^{\frac{1}{2}}\left(V_{\mathrm{bi}} - V\right)^{\frac{1}{2}}$$

$$x_{\mathrm{n}} = \left[\frac{2\varepsilon_{\mathrm{s}} N_{\mathrm{A}}}{q N_{\mathrm{D}}\left(N_{\mathrm{A}} + N_{\mathrm{D}}\right)}\left(V_{\mathrm{bi}} - V\right)\right]^{\frac{1}{2}}$$

$$C_{\mathrm{T}} = \left|\frac{\mathrm{d}Q}{\mathrm{d}V}\right| = A\left[\frac{\varepsilon_{\mathrm{s}} q N_0}{2\left(V_{\mathrm{bi}} - V\right)}\right]^{\frac{1}{2}}$$

where， $N_0 = \dfrac{N_{\mathrm{A}} N_{\mathrm{D}}}{N_{\mathrm{A}} + N_{\mathrm{D}}}$

4、Depletion layer capacitance

(2)、Calculation

the width of the depletion layer is

$$x_{\mathrm{d}} = x_{\mathrm{n}} + x_{\mathrm{p}} = \left[\frac{2\varepsilon_{\mathrm{s}}}{qN_0}\left(V_{\mathrm{bi}} - V\right)\right]^{\frac{1}{2}}$$

the depletion layer capacitance

$$C_{\mathrm{T}} = A\frac{\varepsilon_{\mathrm{s}}}{x_{\mathrm{d}}} = A\left[\frac{\varepsilon_{\mathrm{s}} qN_0}{2\left(V_{\mathrm{bi}} - V\right)}\right]^{\frac{1}{2}}$$

4、Depletion layer capacitance

(2)、Calculation

Practise expression（in CAD tools）

$$C_{\mathrm{T}} = A\sqrt{\frac{\varepsilon_{\mathrm{s}} q N_a N_d}{2(N_a + N_d)V_{\mathrm{bi}}}\frac{V_{bi}}{(V_{bi} - V_a)}} = C_{T0}\sqrt{\frac{V_{bi}}{(V_{bi} - V_a)}}$$

Common expression

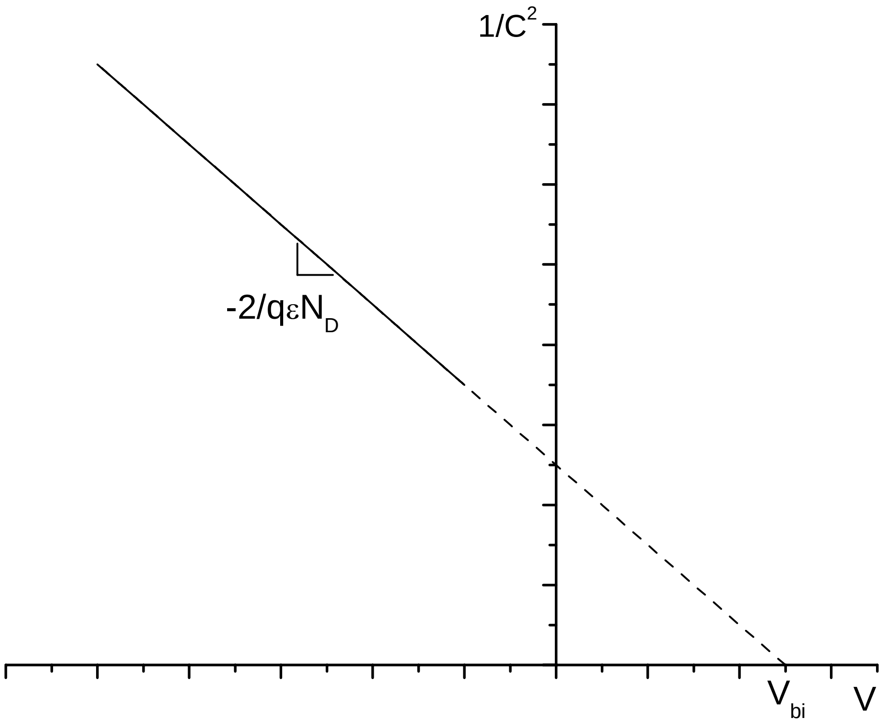
$$C_{\mathrm{T}} = C_{T0}\left(1 - \frac{V_a}{V_{bi}}\right)^{-m}$$

For one-side abrupt junction， m=1/2

For linearly graded junction，m=1/3

4、Depletion layer capacitance

(3)、Discussion



A capacitance versus voltage measurement can be used to obtain the built-in voltage and the doping density of a one-sided p-n diode. The capacitance-voltage characteristic and the corresponding $1/C^2$ curve are shown in the left figure.

4、Depletion layer capacitance

3、讨论

$$C_{\mathrm{T}} = A\frac{\varepsilon_{\mathrm{s}}}{x_{\mathrm{d}}}$$

势垒区中电离杂质电荷随外加电压的变化率；

正负电荷在空间上是分离的；

与直流偏压成幂函数关系；

正偏反偏下均存在，可作电容器使用；

要使C_{T}↓，应使A↓，x_{d}↑（N↓，反偏↑）。

$$C_{\mathrm{D}} = \frac{qI_{\mathrm{DQ}}\tau}{2kT}$$

中性区中非平衡载流子电荷随外加电压的变化率；

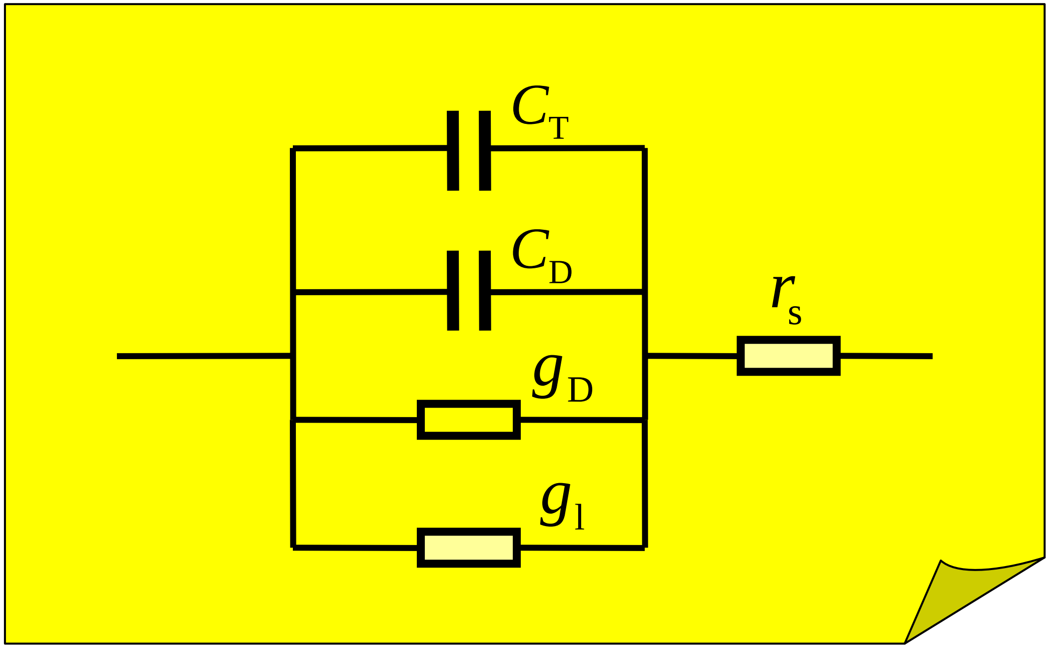
正负电荷在空间上是重叠的；

与直流电流成线性关系，与直流偏压成指数关系；

只存在于正偏下；

要使C_{D}↓，应使I_{F}↓（A↓，正偏↓），τ↓。

5、 Equivalent circuit



g_l is the drain conductance，r_s 为 is the resistance in series。

小结

- 势垒电容的物理含义与表达式
- 势垒电容测量的实际应用
- 势垒电容与扩散电容的对比
- 集成电路设计软件中势垒电容模型参数的含义和作用
- 交流小信号等效电路