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FOUR LEVEL SIMULATION OF MOSFET

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In this paper a software (MOSOFT) has been developed for 4-level simulation of MOSFETS. This software simulates the device characteristics up to micron channel length and includes long channel, short channel, subthreshold and field dependent mobility degradation models.

Keywords: MOSOFT; channel effect; VGB

I. INTRODUCTION

Nowadays, IC designers have the opportunity to set or tune or adjust devices to circuit needs by using circuit simulation softwares which save considerable time in testing, optimising and verifying the performance of circuits. MOSOFT is one such simulation software.

We briefly explain Subthreshold Region and Short Channel Effects below as these play an important role in MOSOFT – Simulation Software.

Subthreshold Region

When gate voltage is below threshold voltage, the corresponding region is called subthreshold region.

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Short Channel Effects

For a given channel doping concentration as the channel length is reduced, the depletion layer widths of the source and drain junctions become comparable to the channel length. Potential distribution in the channel now becomes Two-dimensional depending on both the transverse field (controlled by drain bias) and longitudinal field (controlled by gate bias).
This resuls in:

a) degradation of subthreshold behaviour;
b) dependence of threshold voltage on channel length and biasing voltage.
c) failure of current saturation due to punch through.

Short channel effects complicate device operations and degrade device performance and hence should be minimized.

A particular approach concentrates on decreasing device dimensions while maintaining long channel behaviour in the subthreshold region. It has been empirically found that the minimum channel length for which such long channel behaviour is maintained fits in the relations:

$$L_{\min} = 0.4[r\ t_{ox}(W_S + W_D)^2]^{1/3} \tag{1}$$

where

r : source and drain function
W_S : depletion width at source
W_D : depletion width at drain
t_{ox} : insular thickness

MOSOFT is developed on 4 levels which are briefly explained below:

Level 1 is used solely for implementation of long channel MOSFETs. It is based on the model proposed by shichmann and Hodges [...] and is usually not precise.
Level 2 gives a better model for large and short channel MOSFETs, It in based an the model proposed by Ihantola and Moll [1].

Level 3 uses a semiemperical model on a simplification, proposed by Dang [2], of the Ihantola and Moll model. The short channel effects are included semiempirically in the calculation of threshold voltage and mobility.

Level 4 is used specially for the simulation of subthreshold currents. It can be used for both long and short channel transistors. The former uses the Fichtner and Potzl model [3] while latter uses a 4 parameter fitting model of the subthreshold current suggested by Poon [4]. The fitting parameters can be found experimentally.

II. LEVEL 1 MODEL: THEORETICAL BACKGROUND

We consider here MOSFETs having *p*-type substrate and an *n*-type channel. The behaviour of MOSFETs with an *n*-type substrate is dual with the sign of the voltages end currents changed. The reference condition of the surface is when the semiconductor has the same carrier concentrations at the surface and at the substrate. This state is called the FLAT-BAND condition, The corresponding VGB needed to obtain this condition is the flat-band voltage VFB given by

$$V_{FB} = \Phi_{MS} - (Q_o/C_{OX}) \tag{2}$$

where Q_o is the charge at the oxide-silicon interface C_{OX} is the capacitance per unit area of the thin oxide layer.

For $V_{GB} = V_{FB}$, the carrier concentration is constant in the semiconductor and equals N_A. When $V_{GB} > V_{FB}$, the holes (majority carriers) are pushed away from the surface so that the negative charge of the fixed ions restores the balance with the gate charge. The carrier concentration near the surface is said to be depleted, The thickness of the depletion region X_B is given by

$$X_B = (2 \in_S / qN_A)^{1/2} \varnothing_s \tag{3}$$

where $\varnothing_S$ is the potential across the depleted region. If $\varnothing_S$ is small enough to neglect the minority carriers in the channel, we get

$$\varnothing_S = \{[\Upsilon^2 + 4(V_{GB} - V_{FB})^{1/2} - \Upsilon]^2/4\} \tag{4}$$

where

$$\Upsilon = ((2 \in_s qN_A)^{1/2}/C_{ox}). \tag{5}$$

These equations are valid as long as the carrier concentration remains negligible with respect to NA in the channel.

When $\emptyset_S$ is sufficiently high, the concentration of electrons at the surface can exceed that of the holes in the substrate. From Boltzmann's distribution this happens when

$$\emptyset_S = 2\,\emptyset_p \textit{ i.e.,} \text{ when } n = N_A = ni\exp(\emptyset_p q/KT) \tag{6}$$

or

$$\emptyset_p = (KT/q)\ \ln\ (N_A/n_i). \tag{7}$$

At $\emptyset_S = 2\emptyset_p$, this theory assumes that the surface condition changes from depletion to one of inversion.

Therefore, the condition $V_{GB} = V_{TH}$ is reached when $\emptyset_S = 2\emptyset_p$ Then

$$V_{TH} = V_{FB} + 2\emptyset_p + \Upsilon(2\emptyset_p - V_{BS})^{1/2} \tag{8}$$

where Υ is given by equation (5).

For $V_{GS} > V_{TH}$ by applying a positive voltage to the drain, the electrons in the channel flow by drift from surface to drain. We derive

$$I_{DS} = \mu\, C_{OX}(W/L_{eff})[(V_{GS} - V_{TH})V_{BS} - (V_{DS}2/2)]. \tag{9}$$

This is valid as long as a continuous channel exists between source and drain. However, if there is a point in the channel where the voltage between the channel and gate is equal to threshold voltage, the channel is only formed from $X = 0$ to X' where L' is the point where the channel voltage reaches saturation voltage V_D, sat.

For $V_{DS} > V_D$ sat the current I_{DS} is not a function of V_{DS} because the voltage at the end of the channel still remains equal to V_D, sat. Then

$$I_{DS} = \beta(V_{GS} - V_{TH})^2/2 \tag{10}$$

and

$$\beta = \mu\, C_{OX}(W/L_{eff}) = \kappa_p(W/L_{eff}) \tag{11}$$

Here κ_p is the transconductance parameter. This level is based on the gradual channel approximation *i.e.*, the traverse field is much larger than the longitudinal field.

MOSFET Implementation for Level 1

Linear Region

For $V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$:

$$I_{DS} = \kappa_p[W/(L - 2X_{jl})][V_{GS} - V_{TH} - V_{DS}/2] \quad (12)$$
$$V_{DS}(1 + \lambda V_{DS})$$

where X_{jl} is the lateral diffusion and

$$V_{TH} = V_{TO} + \Upsilon(2\emptyset_p - V_{BS})^{1/2} - (2\emptyset_p)^{1/2}] \quad (13)$$

V_{TO} is the threshold voltage for $V_{BS} = 0$.

Saturation Region

$$V_{GS} > V_{TH} \text{ and } V_{DS} > V_{GS} - V_{TH} :$$
$$I_{DS} = (KP/2)[W/(L - 2X_{jl})](V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (14)$$

where

W: width of channel

L: length of channel.

The amount by which the gate electrode overlaps the source and drain regions must be subtracted from the channel length. In Eq. (12) and (14), (L-2X_{ji}) stands for L_{eff}.

The term $(1 + \lambda V_{DS})$ introduced in the model is an empirical correction of the conductance. There are two parameters which characterize this model: V_{T0} and λ; both of which refer to the electrical behaviour of the MOSFET. The results of Level 1 model are shown as Figures 1–9.

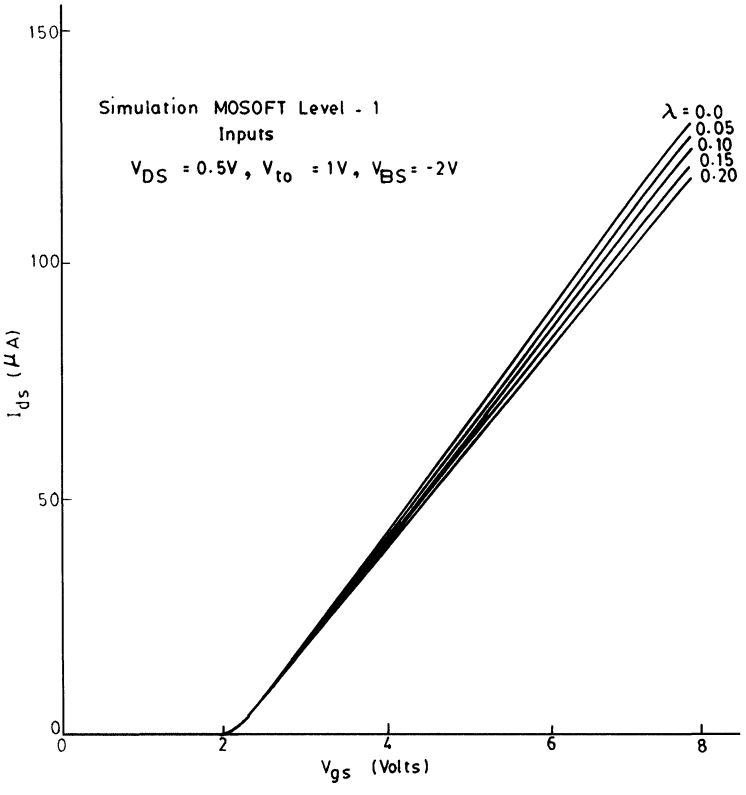

FIGURE 1 Graph drawn by the equations of MOSOFT for the values of the various parameters as indicated above.

III. LEVEL 2 MODEL: THEORETICAL BACKGROUND

The asumptions of this model are:

1) Gradual channel approximation,
2) Uniform doping throughout the P-region,
3) Constant mobility throughout the channel length,
4) Only drift transport occurs in the channel.

We get an expression for $V_{D'sat}$ as.

$$[V_{GS} - V_{FB} - 2\emptyset_p + (\Upsilon^2/2)\{1 - [1 + (4/\Upsilon^2)(V_{GS} - V_{FB} - 2\Upsilon\emptyset_p)]^{1/2}\} + \Upsilon(V_{SB} + 2\emptyset_p)^{1/2}] \quad (15)$$

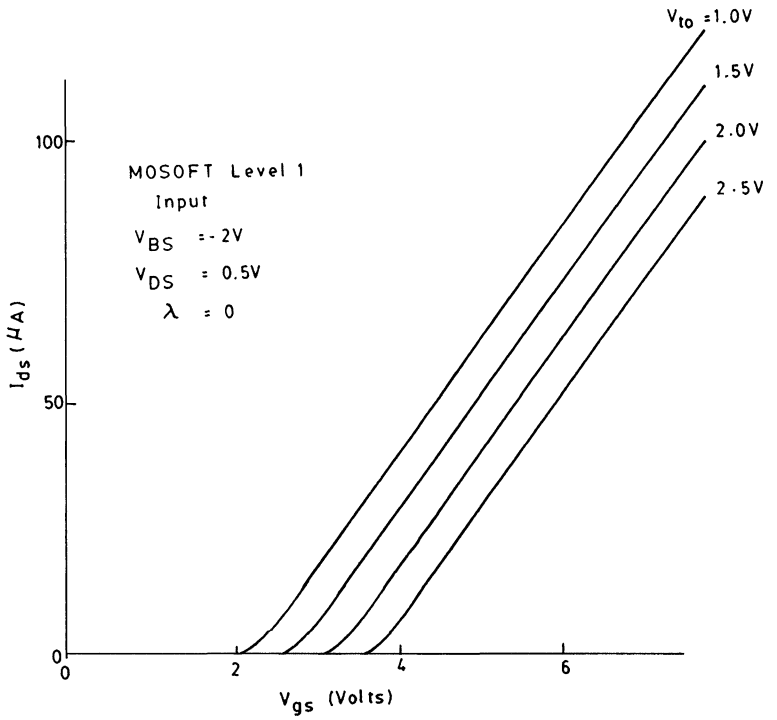

FIGURE 2 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated above.

MOSFET Implementation for Level 2

The threshold voltage can be calculated from the physical parameters by the equation:

$$V_{TO} = \emptyset_{MS} - (qN_{SS}/C_{OX}) + 2\emptyset_p + \Upsilon(2\emptyset_p)^{1/2} \tag{16}$$

where

$$\emptyset_{MS} = -T_{PG}(E_g/2) - KT/q) \ln (N_A/n_i) \tag{17}$$

T_{PG} represents the type of gate and takes a value of 0 for metal gate MOSFET.

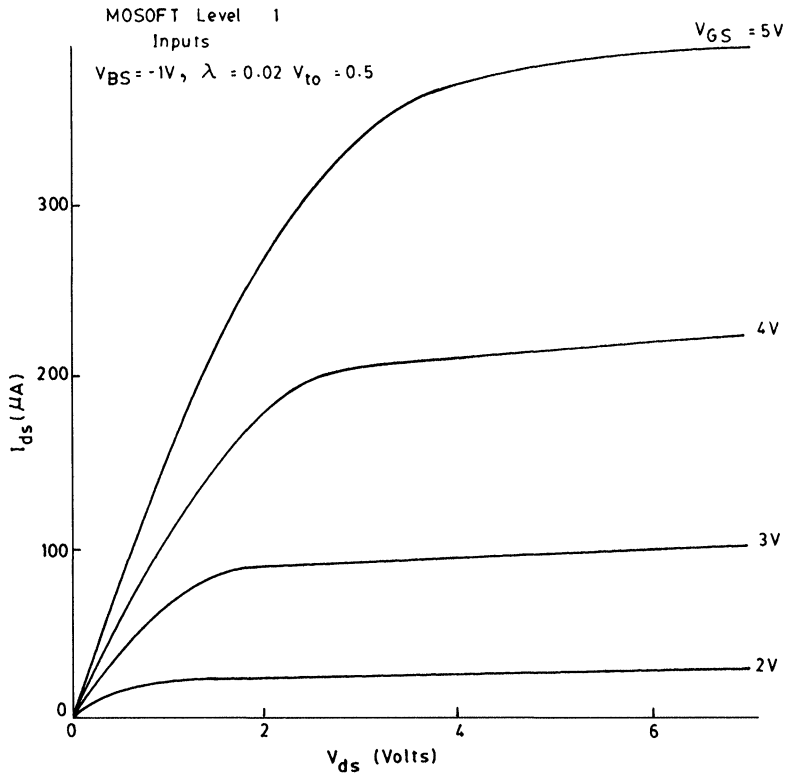

FIGURE 3 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

+ 1 or −1 for polysilicon gate electrode MOSFET,
−1 if polysilicon is doped of the same type as the substrate,
+ 1 if it is of the opposite type.

Linear Region

We have an expression for I_{DS} along with the correction term of the channel length modulation, as

$$[\kappa_p'/(1-\lambda V_{DS})][W/(L-2X_{jl})] \\ [(V_{GS}-V_{FB}-2\varnothing_p-V_{DS}/2)V_{DS}-(2/3)\Upsilon \\ \{(V_{DS}-V_{BS}+2\varnothing_p)^{1.5}-(2\varnothing_p-V_{BS})^{1.5}\}]. \tag{18}$$

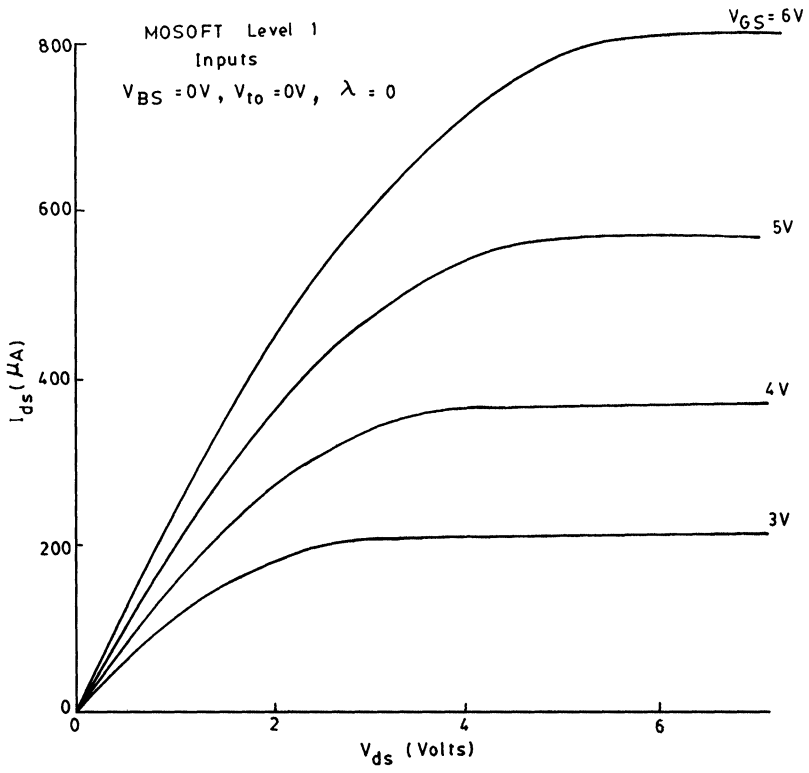

FIGURE 4 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

Saturation Region

$$I_{DS} = I_D, \text{sat}/(1 - \lambda V_{DS}) \tag{19}$$

$$V_D, \text{sat} = V_{GS} - V_{FB} - 2\emptyset_p + \Upsilon^2\left\{1 - [1 + (2/\Upsilon^2)(V_{GS} - V_{FB})]^{1/2}\right\} \tag{20}$$

1. The above equations do not agree well with experimental data. Variance of Mobility with gate electrode field: In the Level 2 model

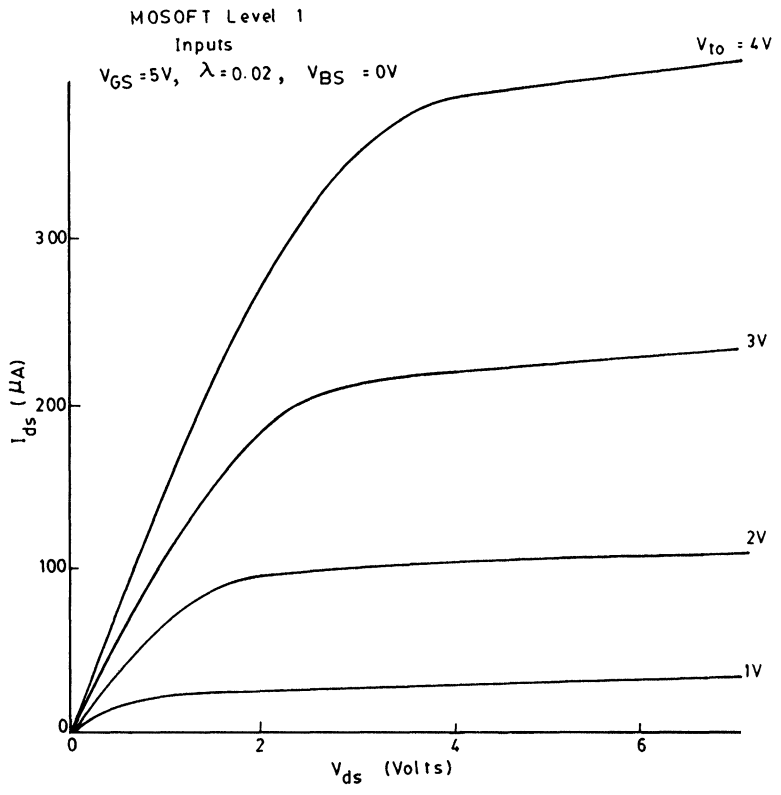

FIGURE 5 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

mobility was assumed constant. A variation of the parameter κ_p has been introduced in MOSOFT. The modified expression is:

$$\kappa_p' = \kappa_p\{(\in_S / C_{OX})[(U_C t_{OX})/(V_{GS} - V_{TH})]\} \tag{21}$$

U_C is the gate to channel critical field and the term $(V_{GS}\text{-}V_{TH})/t_{OX}$ represents the average electrical field perpendicular to the channel.

2. Variance of channel length in Saturation Region: We can use a physical model to calculate the channel length is saturation. We have:

$$\lambda = (L_{eff} - L')\, L_{eff} V_{DS} \tag{22}$$

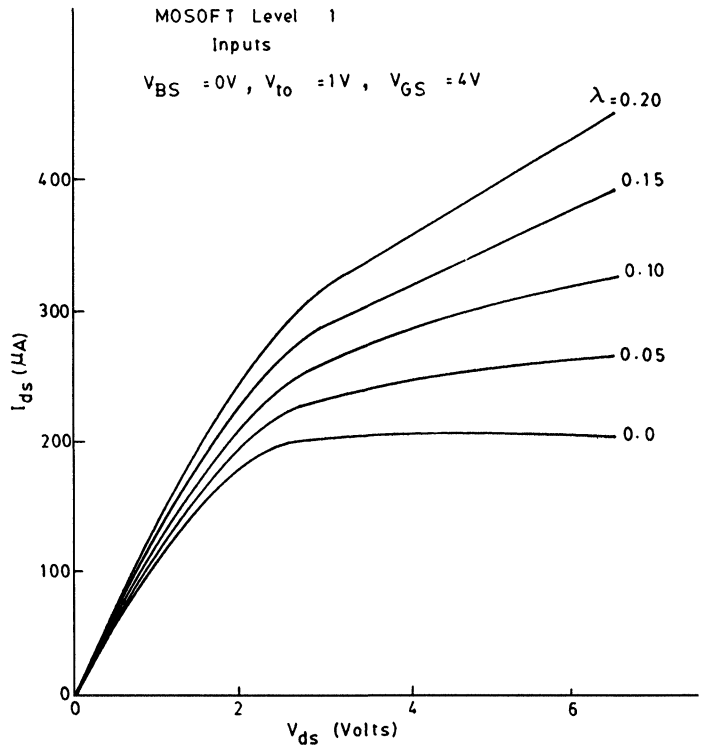

FIGURE 6 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

L_{eff}-L' is given by the expression

$$X_D\{(V_{\text{DS}} - V_D\text{sat}/4) + [1 + (V_{\text{DS}} - V_D\text{sat})^2/4]^{1/2}\} \tag{23}$$

and

$$X_D = (2 \in_S qN_A)^{1/2}. \tag{24}$$

3. Effect of channel length on threshold voltage:
The model was obtained from theory which did not take 2-dimensional effects into account. We correct this by modifying the value of Υ to Υ' which is defined as:

$$\Upsilon' = \Upsilon\{1 - (X_j/2L_{\text{eff}})[(1+2W_s/X_j)^{1/2} + (1+(2W_D)/X_j)^{1/2} - 2]\} \tag{25}$$

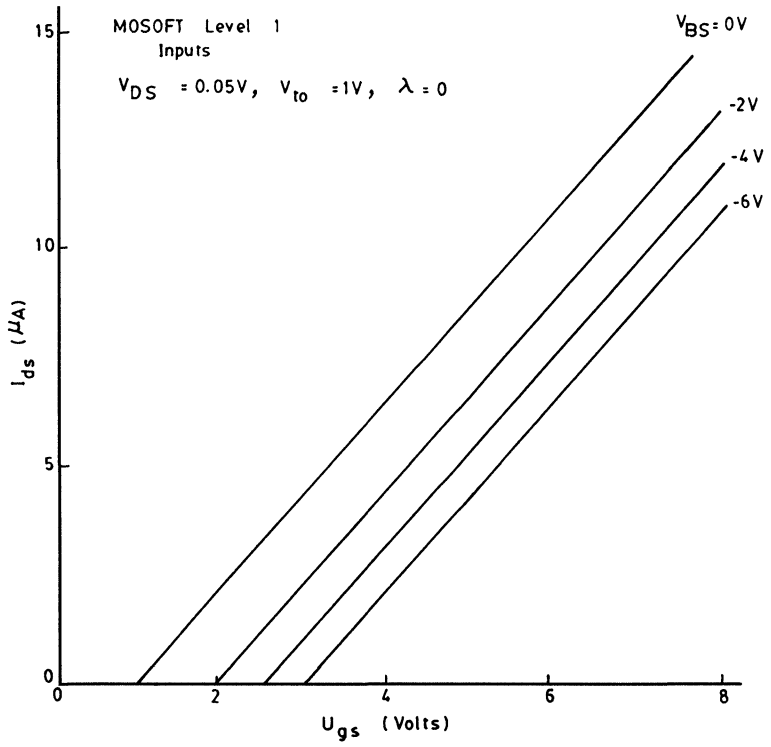

FIGURE 7 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

Here

$$W_S = X_D(2\emptyset_p - V_{BS})^{1/2} \tag{26}$$

$$W_D = X_D(2\emptyset_p - V_{BS} + V_{DS})^{1/2} \tag{27}$$

and X_D is given by Eq. (24)

4. Effect of Speed Limit of Carriers:
   This model is based on the hypothesis that charge in the channel is zero for $X = L'$ This is not true because a minimum concentration greater than zero exists in the channel due to the carriers that sustain the saturation current.

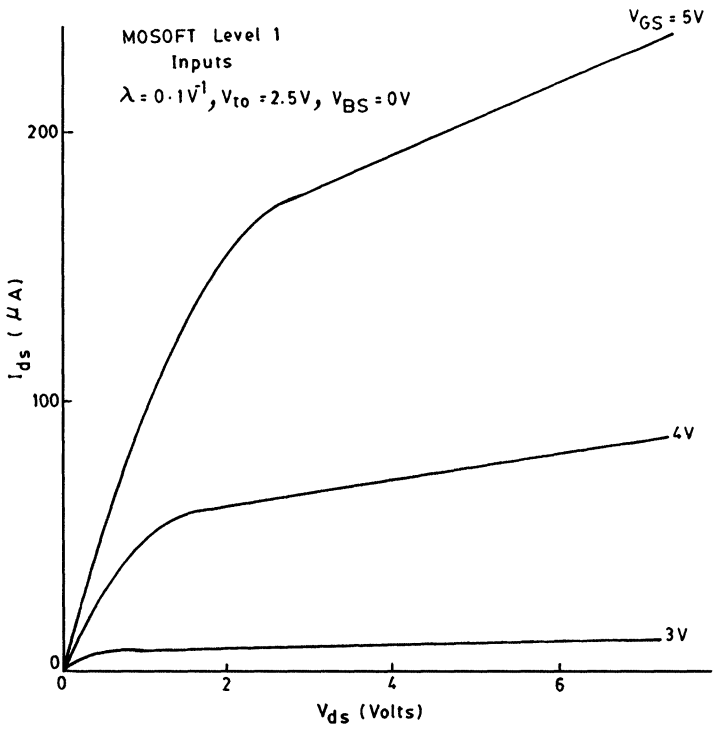

FIGURE 8 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

Also, the electric field between drain and channel and ($X = L'$) can drift the carriers at a maximum speed given by $V_{\max}$. Now:

$$QI' = (\mathrm{ID}, \mathrm{sat}/W V_{\max}) \tag{28}$$

and

$$L_{\mathrm{eff}} - L' = X_D[(X_D V_{\max}(2\mu)^2 + V_{\mathrm{DS}} - V_D, \mathrm{sat}]^{1/2} - X_D V_{\max}/2\mu). \tag{29}$$

We can more modify the value of N_A by a coefficient N_{eff} in the calculation of X_D then

$$X_D = (2 \in_S / qN_A N_{\mathrm{eff}})^{1/2} \tag{30}$$

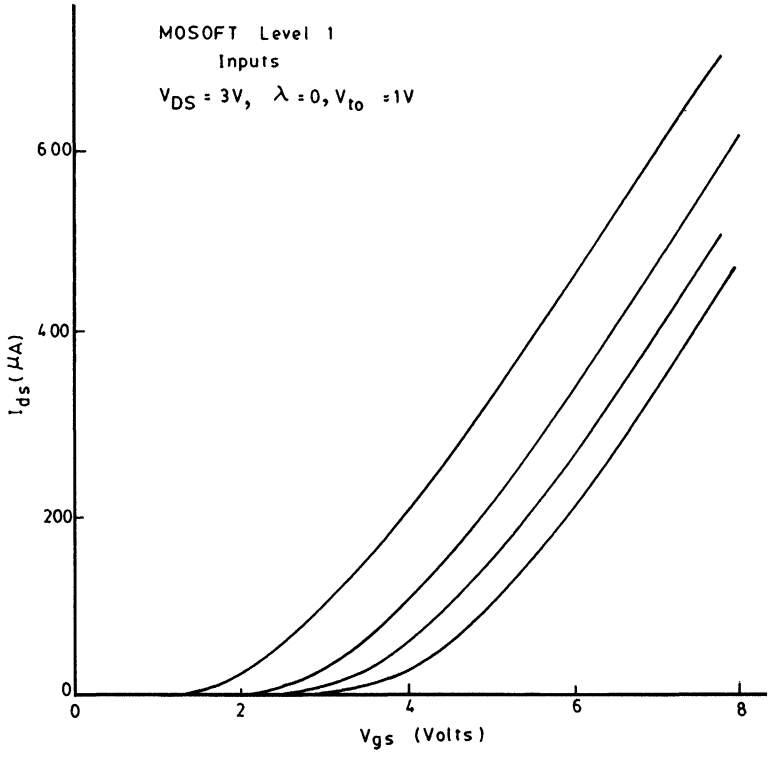

FIGURE 9 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

The model seen so far provides good results in the simulation of MOSFETs with a minimum channel length of 4–5 μm.

5. Effect of channel width on threshold voltage:
   In the MOSFETs with a small channel width W, the value of the threshold voltage V_{TH} is greater than that indicated by the previous theory. This effect is due to the 2-dimensional distribution of the Q_B at the edges of the channel. A modified equation is therefore

$$V_{\mathrm{TH}} = V_{\mathrm{FB}} + 2\emptyset_p + \Upsilon'(2\emptyset_p - V_{\mathrm{BS}})^{1/2} + (\in_S \delta\pi/4C_{\mathrm{OX}} W)(2\emptyset_p - V_{\mathrm{BS}}). \tag{31}$$

The results of MOSFET simulation for this level are shown below: (Figs. 10–13).

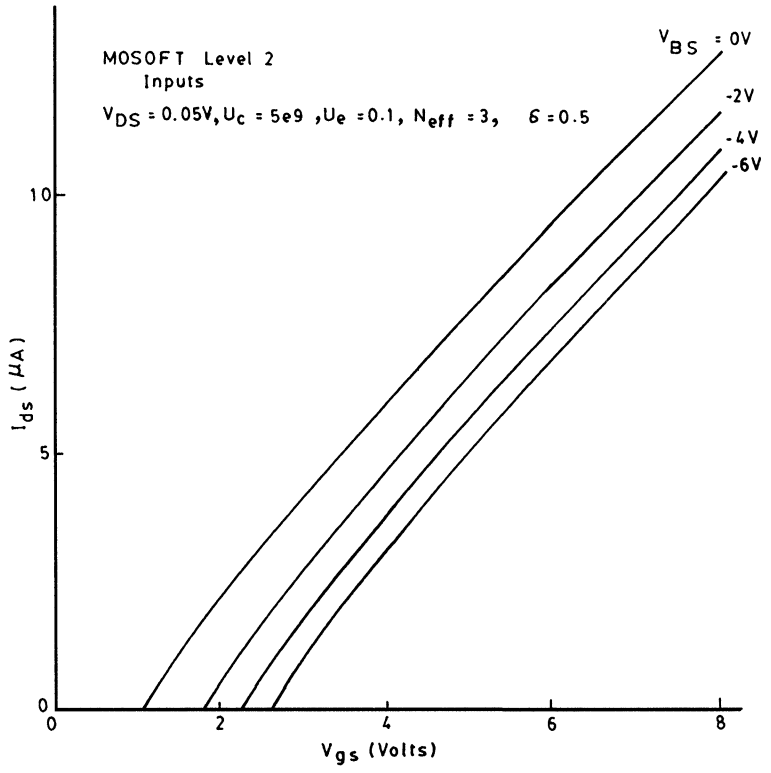

FIGURE 10 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

IV. LEVEL 3 MODEL: THEORETICAL BACKGROUND

The equations for this level are obtained in the same way as for level 2; however, a simplification of the current equation in the linear region is obtained with the Taylor series expansion of the deriving equation for I_D. We employ 3-term binomial series expansion for $(1 + \lambda)^n$ where λ is channel length modulation parameter defined as

$$\lambda = L'/LV_{DS}. \tag{32a}$$

Now

$$\lambda \ll 1; \text{ so that } (1 + \lambda)^{3/2} = 1 + (3/2)\lambda + (3/8)\lambda^2$$

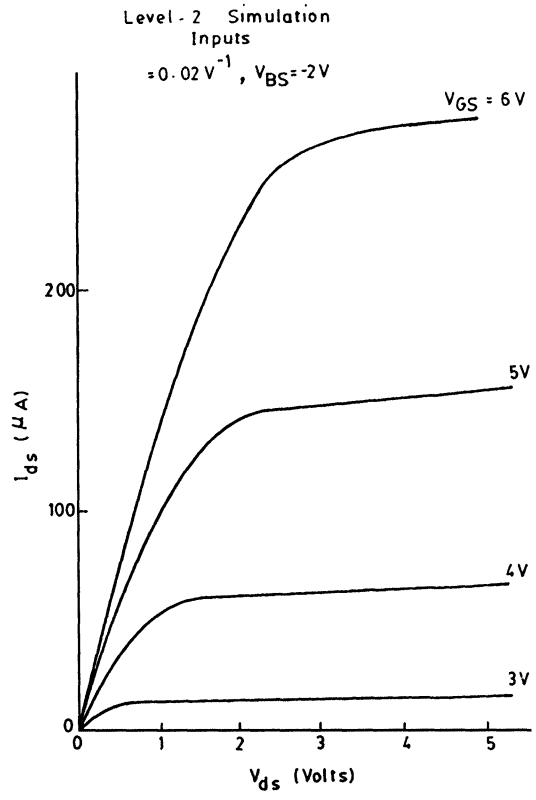

FIGURE 11 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

and we can write:

$$I_D = \mu C_{OX}(W/L)\{(V_{GS} - V_{FB} - 2\varnothing_p)V_{DS} - V_{DS}^2/2 - (2/3)(2 \in_S qN_A)^{1/2}/C_{OX}(2\varnothing_p)^{3/2} [(3/2)(V_{DS}/2\varnothing_p) - (3/8)(V_{DS}/2\varnothing_p)^2]\} \quad (32b)$$

or

$$I_D = \mu C_{OX}(W/L)\{[V_{GS} - V_{FB} - 2\varnothing_p - (2 \in_S qN_A 2\varnothing_p)^{1/2}/C_{OX}]V_{DS} - [1/2 + (\in_S qN_A/\varnothing_p)^{1/2}/4C_{OX}]V_{DS}^2\}. \quad (33)$$

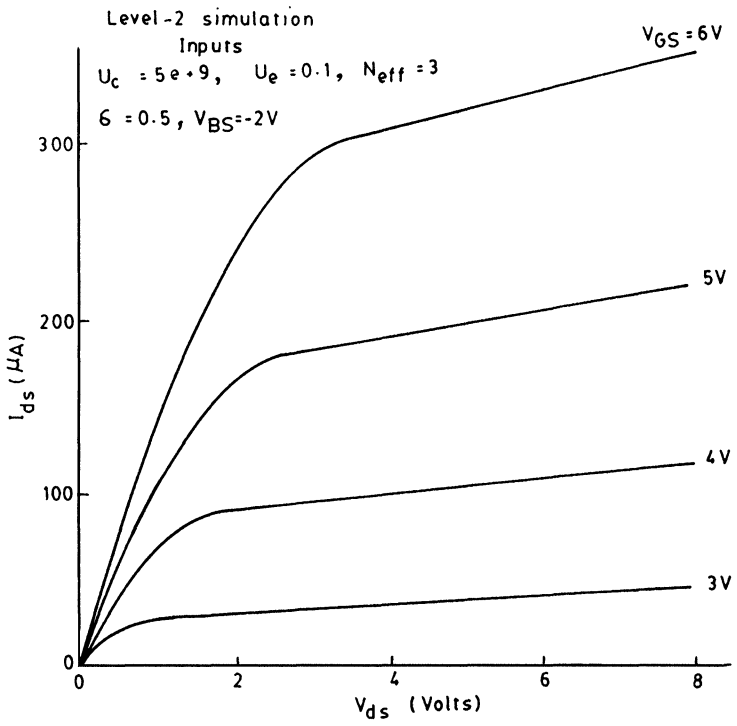

FIGURE 12 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

In view of Eq. (8) this can be rewritten as

$$I_B = \mu C_{OX}(W/L)\{(V_{GS} - V_{TH})V_{DS} - [1/2 + (\epsilon_S qN_A/\emptyset P)^{1/2}/4C_{OX}]V_{DS}^2\}. \tag{34}$$

MOSFET Implementation Level 3

The effect of gate voltage *is* dominant on the mobility. For this reason, it is sometimes said that μ_{eff} "depends an the gate field". It is more correct to say that μ_{eff} depends on the normal field, which in turn, depends on all terminal voltages. Thus the following form has been

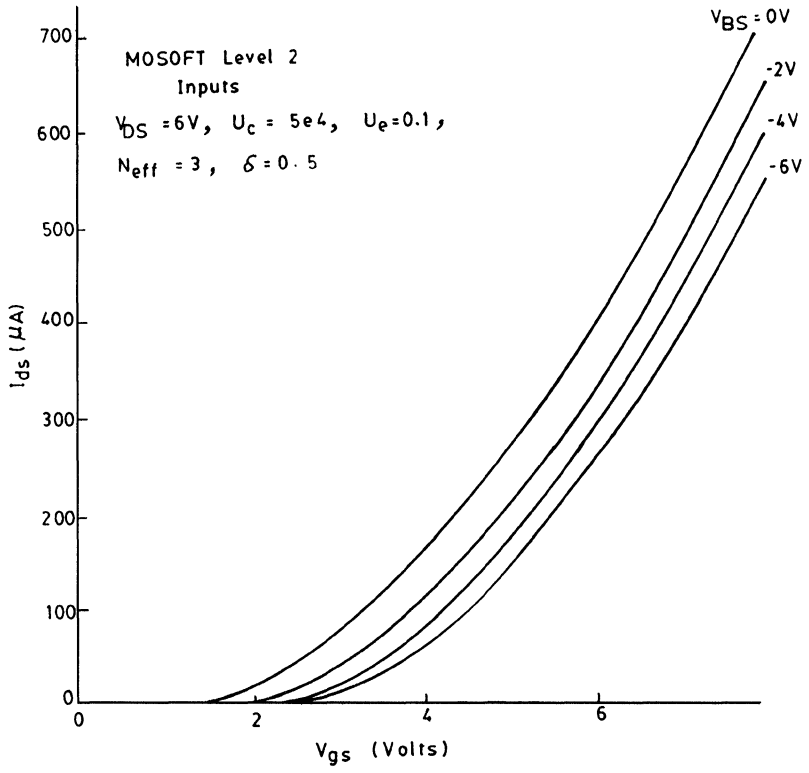

FIGURE 13 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

used for mobility

$$\mu_{\text{eff}} = \mu_o/[1 + \theta(Vgs - V_T V_{\text{SD}})\theta_B V_{\text{SB}}][1 + V_{\text{DS}}/L\varepsilon_O]. \quad (35)$$

Here V_T is the long channel threshold.

The values of μ_o, θ and θ_B used in the above equation may have to be chosen empirically. By comparison to minimise the error. A typical value of μ_o is 60 m^2/v ns for n-channel devices at room temperature θ is of the form β_0/t_{OX}, β_0 is typically 0.001–0.004 m/v and t_{OX} is the oxide thickness, θ_B is about a few hundred of $1v^{-1}$.

The critical electrical field Ec is given by

$$E_C = V_{\max}/\mu \quad (36)$$

which gives the value of E_C as 0.7–3 v/m for electrons, 2–10 v/m for holes.

In the Linear Region we have:

$$I_D = \mu_{\text{eff}}\, C_{\text{OX}}(W/L)[(V_{\text{GS}} - \hat{V}_T V_{\text{DS}}) + (1+\delta)V_{\text{DS}}^2/2]. \tag{37}$$

Saturation Region

We will now determine I_D in the saturation region. This requires some control. If V_T were independent of V'_{DS} as implicitly assumed earlier, we could use Eq. (19) where I'_D would be given by Eq. (37) after replacing V_{DS} by V'_{DS} and I_D by I'_D. In the resulting expression for I'_D, V_{DS} itself would not appear. This, of course, would be because the channel end, considered to be pinched off, would be assumed at a potential V'_{DS} with respect to the source, no matter what the actual value of V_{DS}. However, here we want to include the effect of V_{DS} on V_T. This effect is assumed unrelated to pinch off and is present whether V_{DS} is smaller or larger than V'_{DS} since even for $V_{\text{DS}} > V'_{\text{DS}}$ the channel once is directly influenced by the field lines even in saturation, V_T will continue to be an emanating from the nearby drain. Hence, function of V_{DS}, not V'_{DS}.

The saturation voltage can be expressed with equation simpler than that of the Level 2 Model: *i.e.*,

$$V_D, \text{sat} = V_a + V_b - (V_a^2 + V_b^2)^{1/2} \tag{38}$$

where V_a is the saturation voltage if E_C is not included in the inputs and V_b modifies Ion V_D, sat if it is included. These are expressed as:

$$V_a = (V_{\text{GS}} - V_{\text{TH}})/(1 + F_B) \tag{39}$$

$$V_b = L_{\text{eff}}\, E_C. \tag{40}$$

The equation of the Level 3 Model simulates the modulation of the channel length. On saturation [8] as:

$$L_{\text{eff}} - L = [(E_p X_D^2/2)^2 + K X_D^2 (V_{\text{DS}} - V_{\text{D,sat}})]^{1/2} - (E_p X_D^2/2) \tag{41}$$

where

$$E_p = (K_{\mathrm{ID,sat}})/G_{\mathrm{D\,sat}}\, L_{\mathrm{eff}}). \tag{42}$$

I_{Dsat} and $G_{\mathrm{D.sat}}$ represent the current and conductance respectively for $V_{\mathrm{DS}} = V_{D\mathrm{sat}}$-$K$ is an empirical fitting parameter.

The results for MOSFET Level 3 are shown below (Fig.14):

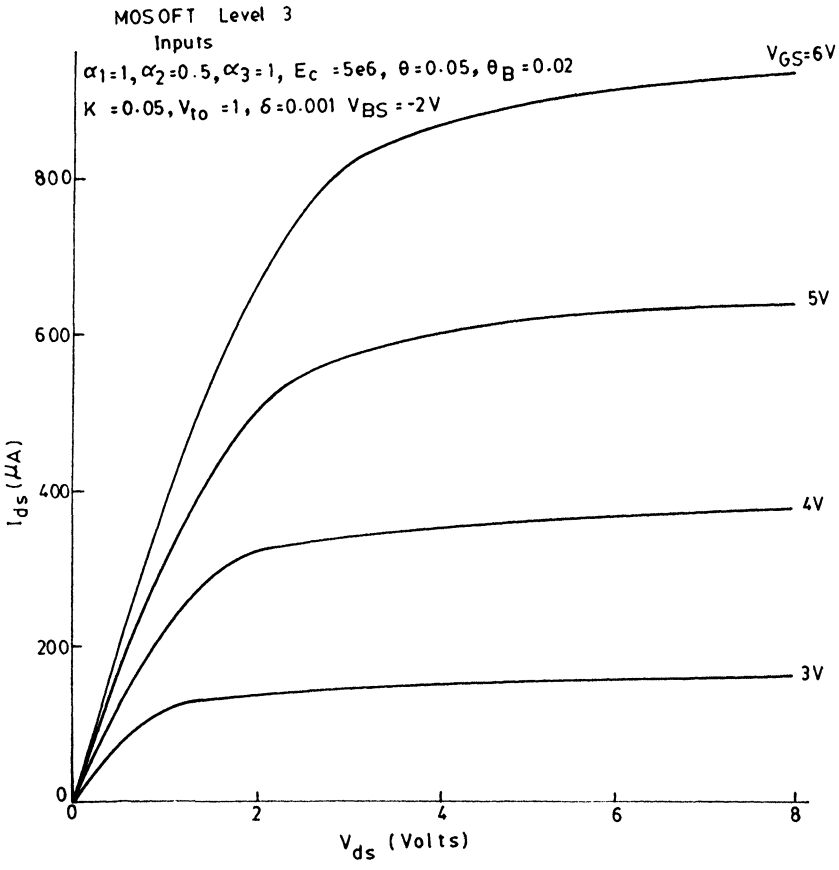

FIGURE 14

V. LEVEL 4 MODEL: THEORETICAL BACKGROUND

Level 4 is exclusively used for subthreshold currents. It has two models and the decision to use a particular model is decided by the empirical equation:

$$L_{\text{MIN}} = 0.4[\Upsilon_j d(W_s + W_D)^2]^{1/3} = 0.4\Upsilon^{1/3}. \tag{43}$$

Here

$$W_D = [(2 \in_S qN_A)(V_D + V_{\text{bi}} + V_{\text{BS}})]^{1/2} \tag{44}$$

$$W_S [(2 \in_S qN_A)(V_{\text{bi}} + V_{\text{BS}})]^{1/2}. \tag{45}$$

Fichtner and Potzl Model

This model calculates the subthreshold currents for long channel MOSFETs as a pure diffusion current. An expression for I_D is

$$WL_{\text{iq}}(D_{\text{ni}}/L)\exp[\beta(\varnothing_{\underline{S}} - 1.5\varnothing_{\underline{F}})]X[1 - \exp(\beta - V_{\text{DS}})]\ [\beta(\theta_S - V_{\text{SB}})]^{1/2} \tag{46}$$

where $\varnothing_s$ can be calculated from

$$V_{\text{GS}} - V_{\text{FB}} = \varnothing_S + [2q\,\theta_S N_A(\varnothing_S + V_{\text{SB}})]^{1/2}/C_{\text{OX}} \tag{47}$$

and

$$\varnothing_F = (KT/q)L_n(N_A/n_i). \tag{48}$$

Poon Mode

A 4-parameter fitting model of the subthreshold currents in short channel devices was suggested by Poon [4], in this the drain current is given by:

$$I_D = I_T[(1/m)(V_{\text{GS}} - V_T)q(KT)]X\{\exp[(1/m)(\mu_o q/kt) - 1]\} \tag{49}$$

where

$$\mu_o = P_3(V_{SB} + 2\varnothing_F)^{1/2}[(V_{SB} + 2\varnothing_F + V_{DS})1/2 - (V_{SB} + 2\varnothing_F)^{1/2}] \tag{50}$$

and

$$V_T = \mu_{TO} + [1 - (1.35 \times 10^{-6})/L][(2q \in_s N_A)^{1/2}/C_{OX}] \\ [(V_{SB} + 2\varnothing_F)^{1/2} - (2\varnothing_F)^{1/2}]. \tag{51}$$

Here I_T, m, P_3 and $_{TO}$ are fitting parameters which have to be determined by experiment or 2-dimensional numerical calculations. μ_o describes the drain voltage dependence of ubthreshold current.

MOSFET Implementation for Level 4

This level has 2 models - the long channel model and the short channel model. The long channel model uses flat data voltage and data as fitting parameters. The short channel model has 4 fitting parameters (I_T, m, P_3, m, μ_{TO}).

The results obtained by simulation were found to be in close agreement with those of the papers and are given below: (Figs. 15–16).

VI. GATE CAPACITANCE MODE

MOSFET uses a gate capacitance model smaller to that proposed by mayor. In this model the charge storage effect is represented by 3 non-linear capacitances C_{GB}, C_{GS} and C_{GD}. The equations are:

Accumulated Region

For $V_{GS} < V_{on} - 2\varnothing_p$:
where

$$V_{on} = V_{TH} + (hkt)/q \tag{52}$$

$$h = 1 + (qn_{FS} + C_d)/C_{OX} \tag{53}$$

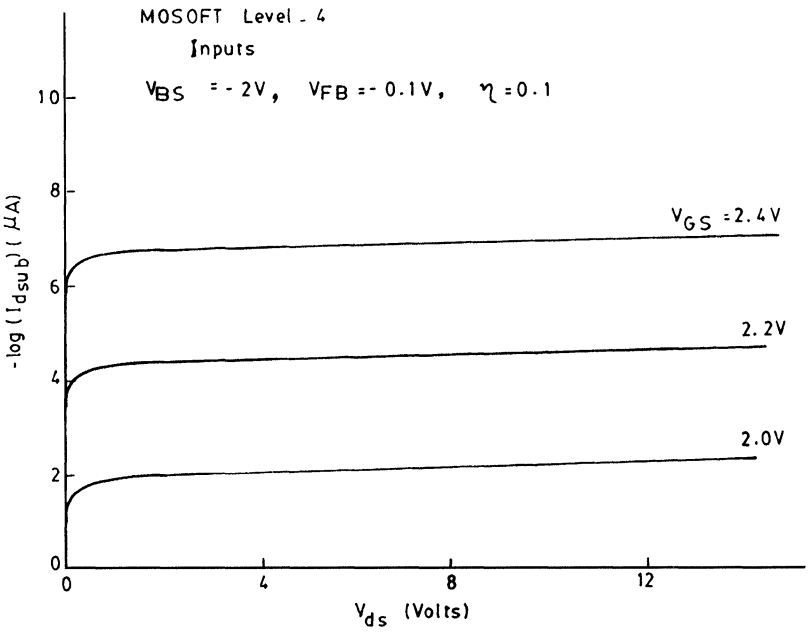

FIGURE 15 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

$$C_{GB} = \overline{C}_{OX} + C_{GBO}L_{eff} \tag{54}$$

$$C_{GS} = C_{GSO}W \tag{55}$$

$$C_{GD} = C_{GDO}W. \tag{56}$$

Depletion Region

For $V_{on}-2\emptyset_p < V_{GS} < V_{on}$:

$$\bar{C}_{GB} = \bar{C}_{OX}(V_{on} - V_{GS})/2\emptyset_p + C_{GBO}L_{eH} \tag{57}$$

$$C_{GS} = (2/3)\bar{C}_{OX}[(V_{on} - V_{GS})/2\emptyset_p + 1] + C_{GSO}W \tag{58}$$

$$C_{GD} = C_{GDO}W. \tag{59}$$

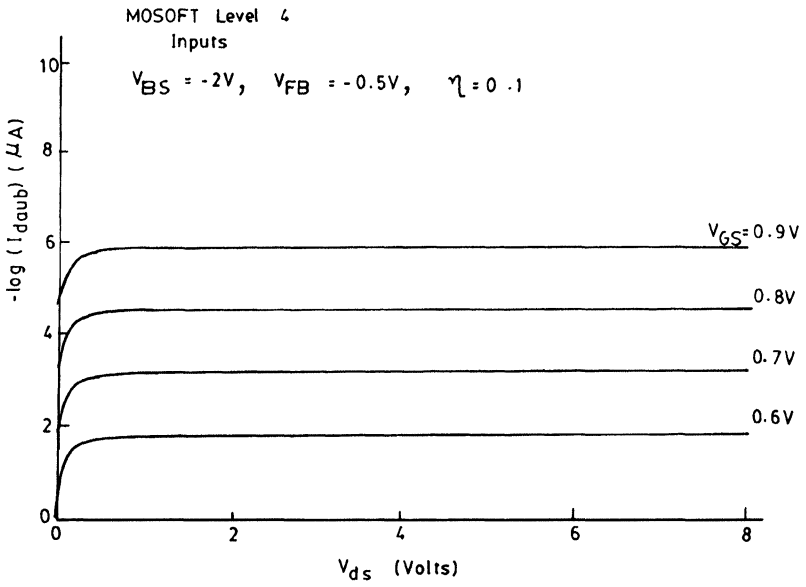

FIGURE 16 Graph drawn by using MOSOFT equations for the values of the various parameters as indicated.

Saturation Region

For $V_{on} < V_{GS} < V_{On}$

$$C_{GB} = C_{GBO}L_{EFF}; \tag{60}$$

$$C_{GS} = (2/3)C_{OX} + C_{GSO}W; \tag{61}$$

$$C_{GD} = C_{GDO}W. \tag{62}$$

Linear Region

For $V_{GS} > V_{On} + V_{DS}$

$$C_{GB} = C_{GBO}L_{EFF} \tag{63}$$

$$C_{GS} = \bar{C}_{OX}\{1-[V_{GS} - V_{DS} - V_{On})/(2(V_{GS} - V_{On}) - V_{DS})]^2 + C_{GSO}W\} \quad (64)$$

$$C_{GD} = \bar{C}_{OX}\{1 - [V_{GS} - V_{On})/(2(V_{GS} - V_{On}) - V_{DS})]^2\} + C_{GDO}W \quad (65)$$

In the above equation

$$\bar{C}_{OX} = C_{OX}WL_{eff} \quad (66)$$

V_{on} is calculated from Eq. (52) if N_{fs} is specified otherwise $V_{on} = V_{TH}$.

C_{GBO}, C_{GSO} and C_{GDO} are the overlap capacitances among the gate electrode and the other terminals outside the channel region.

VII. JUNCTION CAPACITANCE MODEL

The capacitance of the diffused regions of the source and drain is simulated with the *pn* junction model. A separate capacitance model is defined for the periphery of the junction; this is because the capacitance per unit area and its dependence on the reverse-bias voltage in the boundary region of the diffusion are different from those associated with the flat junction.

The total capacitance of a diffused region is calculated from the sum of an area and a perimeter capacitance:

$$C_{BS} = C_J A_S/(1 - V_{BS}/\phi_J)^{MJ} + C_{JSW}P_S/(1 - V_{BS}/\phi_s)^M_{JSW} \quad (67)$$

$$C_{BD} = C_J A_D/(1 - V_{BD}/\phi_J)^{MJ} + C_{JSW}P_D/(1 - V_{BD}/\phi_s)^M_{JSW} \quad (68)$$

where C_J and C_{Jsw} are capacitances at zero bias voltage, for square meter of area and for meter of perimeter respectively and *pj* is the junction potential that the physical parameters as

$$\phi_J = (Eg/2) + (K_T/Q) \ln (N_A/ni) \quad (69)$$

In Eq. (67) and (68), values of mj and M_{jsw} are 0.5 and 0.33 respectively.

VIII. PMOS TRANSISTORS IMPLEMENTATION

If the substrate is made of n-type material and the source/drain regions of P-type material, we have what is known as the p-channel MOS transistor or PMOS transistor.

The operation of the p-channel transistor is the 'dual' of the n-channel operation. The role of electrons played by holes and the role of ionised donor atoms.

$$\gamma = [F(N_D)^{1/2}]/C_{OX} = [F(N_D)^{1/2}]/C_{OX} \tag{70}$$

where N_D is the concentration of the donor atoms in the substrate.

In describing p-channel devices there are some rather obvious sign changes in the model equations, for example instead of Eq. (37) we will have

$$I_{DS} = -(W/L)\mu_{eff}\, C_{OX}[(V_{GS} - \hat{V}_T(V_{DS})V_{DS} - (1+\delta)V_{DS}^2/2] \tag{71}$$

and instead of Eq. (13) we will have

$$V_{TH} = V_{T0} - [(-2\Phi_P - V_{BS})^{1/2} - (-2\Phi_P)^{1/2}] \tag{72}$$

and instead of Eq. (16) we will have

$$V_{T0} = V_{FB} + 2\Phi_P - \gamma(-2\Phi_P)^{1/2} \tag{73}$$

The above are just a few examples to illustrate the difference.

The value of the effective mobility for p-channel devices at low gate voltages is smaller than that in p-channel devices by a factor of 2 to 4; a typical value is 25 m2/vns.

IX. ORIGINAL CONTRIBUTION TO MOSFET MODELLING

1. 4 level MOSFET simulation carried out step by step.
2. Results obtained are an extension of theory.

3. Each Model level is designed for a particular type of MOSFETs *i.e.*, Level 2 model is for large and short channel MOSFETs While Level 4 Model is for the simulation of subthreshold currents.

X. CONCLUSION

The Level 1 is not sufficiently precise because the theory is too approximated and the number of fitting parameters too small; its usefulness is in a quick and rough estimate of circuit performances.

The Level 2 Model can be used with differing complexity by adding the parameters relating to the effects needed to simulate with this model. But because of its inherent complexity a great amount of CPU time is required for the calculations.

The Level 3 model is better off than the Level 2 an the CPU time required for the model evaluation is much lesser. The only disadvantage is the complexity in the calculation of some of its parameters.

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