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A PHYSICAL MODEL FOR MOSFET DRAIN CURRENT IN NON-OHMIC REGIME USING OHMIC REGIME OPERATION

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In order to characterise the velocity saturation phenomena in short channel MOSFET's, a simple method is proposed in this work. It is based on the comparison between transistor behaviour in ohmic and saturation regime respectively. Therefore, the MOSFET characteristic $I_{d0}(V_d)$ avoiding velocity saturation phenomena, can be obtained from ohmic characteristic $I_d(V_g)$ and compared with the experimental characteristic $I_d(V_d)$.

Keywords: MOSFET; Velocity saturation; Pinch off; Conductance; Charge

1. INTRODUCTION

It's not obvious to consider drain current modelling $I_d(V_d)$, without taking into account the velocity saturation phenomena. In fact, it is physically difficult to access due to non linear dependence of drift velocity with lateral field F_y [1] in short channel devices. It is becoming so interest to dissociate physical parameters which are in the origin of velocity saturation and these which are not. In this previous work a new model of drain current $I_{do}(V_d)$ has been proposed. This method has allowed to avoid velocity saturation phenomena and more

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strongly to characterise the velocity saturation effect systematically by comparison between the model and a measured device out-put characteristics. It was shown that $I_{do}(V_d)$ is not other than out-put characteristic of long channel device.

2. MODEL

The operation mode in non ohmic regime consisted on applying an important voltage on the drain in addition to the applied gate voltage. The inversion layer which was evenly distributed in the channel should be more pinched close the drain. At the voltage value V_d equal to $V_{d\mathrm{sat}}$ the charge at the drain level becomes very weak (Pinch Off). For the drain voltage V_d exceeding $V_{d\mathrm{sat}}$ this charge doesn't vary practically. The transistor is saturated on the length ΔL [2]. In the case of short channel MOSFET, the drain current is limited by velocity saturation, and its saturation value depends on both $V_{d\mathrm{sat}}$ value and transistor velocity saturation [3].

2.1. $I_d - V_d$ Characteristic

The MOSFET operation in non ohmic regime can be shared in two principal zones:

2.1.1. Non-ohmic Regime ($V_d < V_{dsat}$)

The inversion charge at y space along the channel which is being in strong inversion is written as:

$$Q_i(y) = C_{ox}(V_g - V_t - V(y)) \tag{1}$$

Where C_{ox} is the oxide capacitance per unit area, V_g and V_t are, respectively, gate and threshold voltage and $V(y)$ is the voltage on the area at y space of the channel which is being in strong inversion. The current drain takes the following expression:

$$I_d(y) = WC_{ox}(V_g - V_t - V(y))v(y) \tag{2}$$

Where W is the channel width, $v(y)$ is the carriers velocity on the area. In this zone the channel is not pinched close the drain. For long

channel MOSFET's the carriers velocity is proportional to gradual voltage in the channel and the drain current follow the relation (3) in condition that effective mobility should be independent of V_d such as:

$$I_d = \mu_{\mathrm{eff}} \frac{W}{L} C_{ox} \left(V_g - V_t - \frac{V_d}{2} \right) V_d \tag{3}$$

This hypothesis is not always verified as the mobility varies *versus* the inversion charge existing in the channel. Moreover, the channel length reduction was accompanied by a degradation of MOSFET component properties [4]. Carriers velocity reduction for short channel MOSFETs is a direct consequence of channel reduction and its expression was given by Thornber model [5]. It depends, so, on lateral field F_y. Consequently, the expression (3) is correct if only both the attenuation coefficients and carriers velocity saturation are neglected.

2.1.2. Saturation Regime ($V_d > V_{dsat}$)

The channel is pinched close the drain and current can not increase *versus* drain voltage V_d. In this zone it is depending only on the applied gate voltage, the inversion charge becomes null at $V_{d\mathrm{sat}} = V_g - V_t$, the Eq. (3) is rearranged as:

$$I_d = I_{d\mathrm{sat}} = \frac{W}{2L} \cdot C_{ox} \mu_{\mathrm{eff}} (V_g - V_t)^2 \tag{4}$$

Therefore, the variation of pinched zone length in the case of short channel devices implies I_d variation with V_d. This leads to non neglected conductance G_d, which can be also modulated by thermal heating effects [7]. If, in the first time, we neglect velocity saturation phenomena, we can write the expression of carriers drift velocity in y channel point such as:

$$v(y) = \mu_{\mathrm{eff}} \frac{dV}{dy} \tag{5}$$

From relation (2) the drain current expression at every y channel point becomes:

$$I_{d0}(V_d) = \int_0^{V_d} \frac{W}{L} C_{ox} (V_g - V_t - V) \mu_{\mathrm{eff}}(V) dV \tag{6}$$

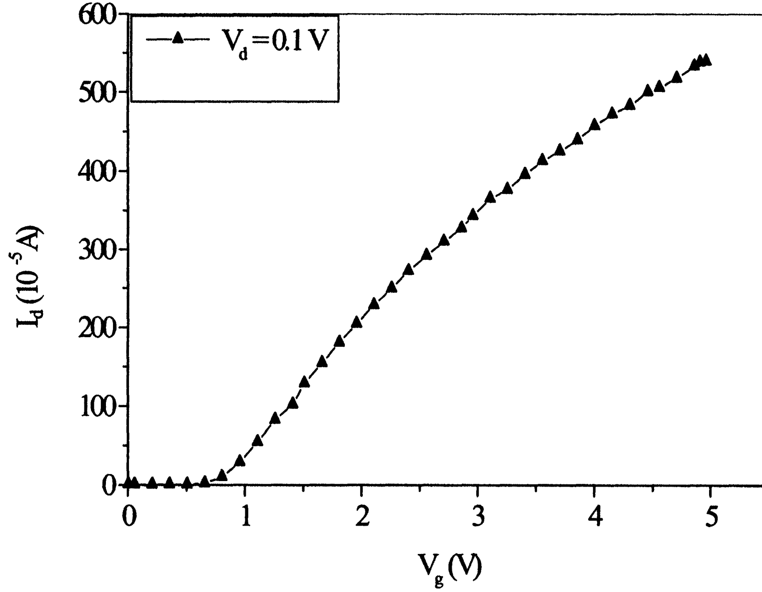

FIGURE 1 Drain current I_d *versus* gate voltage V_g.

It's observed so, that the expression inside the integral corresponds to dynamic conductance expression in ohmic regime and strong inversion (Fig. 1) which is given by:

$$G_d(V) = \frac{W}{L}\mu_{\text{eff}}C_{ox}(V_g - V_t - V) \tag{7}$$

Where V_g was exchanged by $V_g - V_t$, therefore, we can obtain the drain current characteristic of long channel transistor in saturation regime for gate voltage value V_{gi} by simply integrating. The G_d characteristic of ohmic regime between V_{gi} and 0. The expression of I_{d0} is given such as:

$$I_{d0}(V_d, V_{g_i}) = \int_{V_{g_i}-V_d}^{V_{g_i}} G_d(V)dV \tag{8}$$

3. RESULTS AND DISCUSSION

In order to validate experimentally these results we have used a conventional MOSFET where its main parameters are defined as:

thickness oxide $t_{ox} = 6.8\,\text{nm}$, aspect ratio $W/L = 25/0.85$, mobility at low field $\mu_0 = 0.0392\,\text{Cm}^2/\text{V} \cdot \text{s}$, substrate doping ranged between $10^{15} - 10^{16}\,\text{Cm}^{-3}$. Figure 1 shows the experimental drain current I_d *versus* gate voltage V_g. It is found that for V_d exceeding $V_{d\text{sat}}$ the drain current varies weakly against drain voltage V_d which implies a dynamic conductance $G_d(V)$ along the channel (Eq. (7)). The relation (8) is practically interest since it allows to access to transistor characteristics exempt velocity saturation phenomena which has been manifested in the experimental out-put characteristic $I_d(V_d)$ (Fig. 2). In the absence of velocity saturation, the behaviour of simulated drain current in non ohmic regime $I_{d0}(V_d)$, approaches a long channel device operation (Fig. 3). For short channel lengths, the drain current saturation is mainly due to carriers velocity saturation. In the obtained characteristic $I_{d0}(V_d, V_{gi})$, the limit of integration's are conserved when the drain voltage go up from 0 voltage to $V_{d\text{sat}}$ voltage, the inversion charge Q_i go down from $C_{ox}(V_{gi} - V_t)$ value to $C_{ox}(V_{gi} - V_t - V) \cong 0$ value corresponding to the same limits in $I_d(V_g)$ characteristic since gate voltage varies from V_{gi} down to 0 value, this supposes surly that $V_{d\text{sat}} \cong V_{gi} - V_t$, which is the case of long channel devices ($L > 5\,\mu\text{m}$)

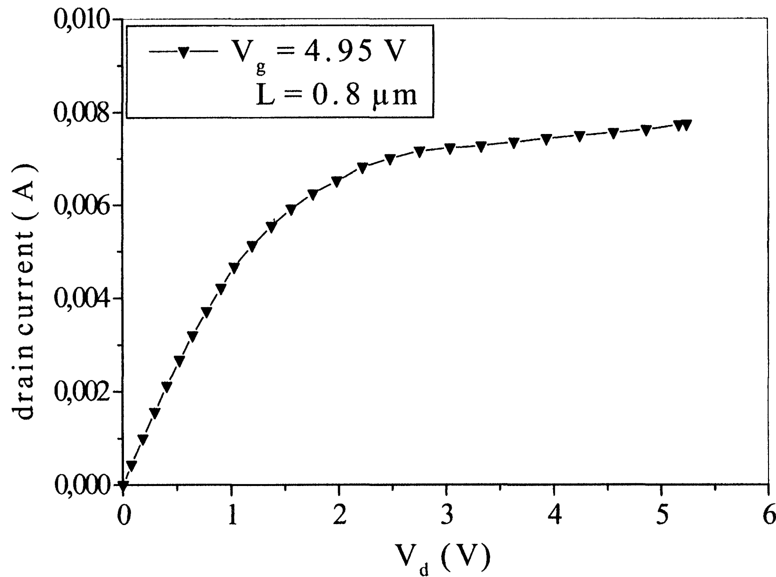

FIGURE 2 Experimental drain current I_d *versus* drain voltage V_d.

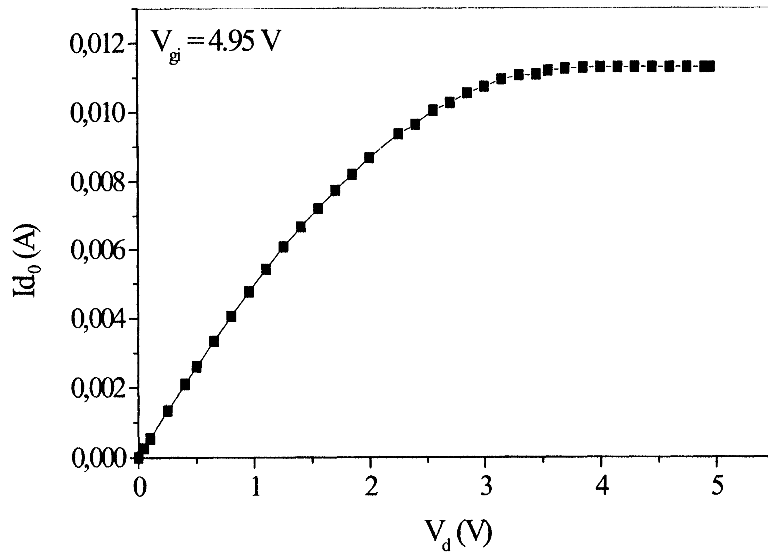

FIGURE 3 Drain current I_{d0} *versus* drain voltage V_d exempt velocity saturation.

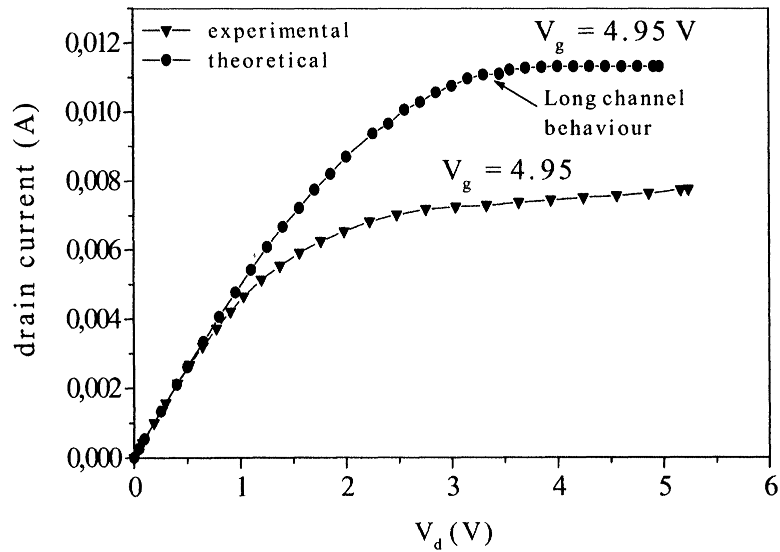

FIGURE 4 Comparison between experimental drain current I_d and drain current model I_{d0} *versus* drain voltage V_d.

without velocity saturation. (Fig. 4) shows a comparison with the drain current model $I_{d0}(V_d)$ without velocity saturation, and experimental data $I_d(V_d)$.

4. CONCLUSION

In this work we have presented a new method which used the integral of $I_d(V_g)$ characteristic in ohmic regime to reach non ohmic characteristic $I_d(V_d)$. This technique allowed to eliminate velocity saturation effects and improves powerful instrument to dissociate simultaneously the parameters related to velocity saturation phenomena and these which are not.

References

[1] Shiu-Wuu Lee and Tung-Yi Chan, *IEEE Trans. Electron Dev.*, Nov., 1990.
[2] Weber *et al.* (1984). *IEEE*, **EDL-5**, 518.
[3] Sodini, C. G., Ko, P. K. and Moll, J., *IEEE Trans. Electron Dev.*, Nov., 1990.
[4] Szelag, B., Balestra, F., Ghibaudo, G. *et al.*, *IEEE*, **EDL**, Dec., 1998.
[5] Thornber, K. K. (1980). *J. Appl. Phys.*, **51**, EDL-4, 2127.
[6] Jomaah, J., Balestra, F. and Ghibaudo, G., *IEEE International SOI Technology Conference*, PalmSprings, USA, Oct., 1993.
[7] Taur, Y., Hsu, C. H., Wu, B., Kiehl, R., Davari, B. and Shahidi, G. (1993). *Solid-State Electronics*, **36**(8), 1085–1087.