Active and Passive Elec. Comp., 2001, Vol. 24, pp. 187–199
Reprints available directly from the publisher
Photocopying permitted by license only

IMPACT OF THE STRESS ON THE SUB-MICRON N-METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR CHARACTERISTICS

R. MARRAKH and A. BOUHDADA*

Laboratoire de Physique des Matériaux et de Microélectronique-Université Hassan II Aïn Chok Faculté des Sciences, Km8, Route d'El Jadida, BP 5366 Maârif-Casablanca-Morocco

(Received 15 April 2001; In final form 15 May 2001)

In this paper, we present a drain current model for stressed short-channel MOSFET's. Stress conditions are chosen so that the interface states generated by hot-carriers are dominant. The defects generated during stress time are simulated by a spatio-temporal gaussian distribution. The parasitic source and drain resistances are included. We also investigate the impact of the interface charge density, generated during stress, on the transconductance. Simulation results show a significant degradation of the drain current versus stress time.

Keywords: Hot-carrier-injection; Stress time; Drain current; Transconductance; MOSFET

I. INTRODUCTION

The degradation of the NMOS transistors caused by hot carrier injection in the oxide and at the $Si-SiO_2$ interface constitutes a potential limit to device scaling. Indeed, the transistor miniaturization entails the presence of higher electric fields that provide enough energy to the channel electrons which may generate electron-hole pairs through impact ionization. These electrons and holes contribute to the gate and substrate current [1–5] and they may create damage in the oxide or in the interface near the drain junction [6–8]. Due to its

*Corresponding author. E-mail: bouhdada@facsc-achok.ac.ma

strong impacts on device and circuit reliability, the hot-carrier effect becomes an important research topic for submicrometer and deep submicrometer MOSFET devices. Understanding the physical phenomenon of the degradation process is required in order to find technological solutions to minimize the aging effect and device performance degradation.

In this work we devote our effort to develop a drain current model in relation with the defect density generated by the hot-carrier-injection during stress time. This defect density is modeled by a spatio-temporal distribution. The modeling of this defect density was developed in our previous work [9] by investigating the threshold voltage evolution according to stress time. Simulation results allow us to deduce the impact of the stress time on the I–V characteristic and on the transconductance.

II. DRAIN CURRENT MODELING

To consider the source and drain resistances, we treat the device as an intrinsic MOSFET in series with two ones (Fig. 1).

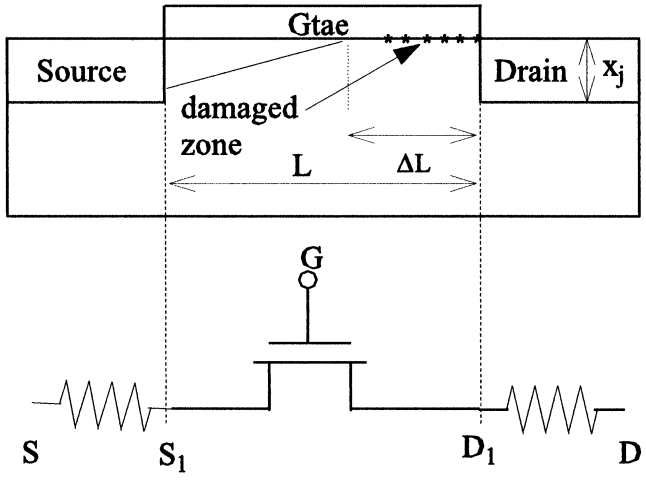

FIGURE 1 Schematic diagram and equivalent circuit of MOSFET.

The source drain voltage can be written as:

$$V_{DS} = V_{D_1 S_1} + (R_s + R_D) I_{DS} \tag{1}$$

The drain current expression in the linear region is given by:

$$I_{DS} = \mu_s W \vartheta C_{\text{ox}} [V_{GS} - V_{T_0} + \Delta V_T - F_B V(y)] \tag{2}$$

where μ_s, W, C_{ox} and V_{GS}, are respectively, the surface mobility, the channel width, the gate oxide capacitance per unit area and the gate bias.

ϑ is the carrier velocity which is expressed by:

$$\begin{cases} \vartheta = \dfrac{\mu_s E_y}{1 + E_y / E_{\text{sat}}} & E_y \leq E_{\text{sat}} \\ \vartheta = \vartheta_{\text{sat}} & E_y > E_{\text{sat}} \end{cases} \tag{3}$$

where $V(y)$ and E_y are the potential and the lateral electric field in the channel; ϑ_{sat} is the carrier saturation velocity. The parameters involved in Eqs. (2) an (3) are defined as:

$$\begin{cases} V_{T_0} = V_{FB} + 2\phi_f + \gamma \sqrt{2\phi_f + V_{SB}} \\ \mu_s = \dfrac{\mu_0}{[1 + \theta (V_{GS} - V_{T_0})]} \\ E_{\text{sat}} = \dfrac{2\vartheta_{\text{sat}}}{\mu_s} \\ F_B = \dfrac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} + 1 \\ \gamma = \sqrt{\dfrac{2q\varepsilon_s N_A}{C_{\text{ox}}}} \\ \Delta V_T = \dfrac{\varepsilon_S}{C_{\text{ox}}} \left(\dfrac{X_{\text{dep}}}{2} + \dfrac{X_{\text{dep}}^2 C_{\text{ox}}}{12 \varepsilon_S} \right) \dfrac{\partial^2 V(y)}{\partial y^2} \end{cases}$$

$V_{FB}, V_{SB}, \varepsilon_s$, and ϕ_f are the flat-band voltage, the substrate bias, the dielectric permittivity and the Fermi potential, respectively. μ_0 is the low field channel mobility and θ is the mobility degradation factor resulting from vertical electric field. X_{dep} is the depletion width.

ΔV_T is the threshold voltage reduction due to the lateral electric field. In the linear region ΔV_T is small and can be regarded as a constant since the lateral electric field is weak.

The defect density created during stress time leads to an increase of the threshold voltage and a reduction of the carrier mobility, namely:

$$V_{th} = V_{T_0} + q\frac{N_{it}(y, t_s)}{C_{ox}} \tag{4}$$

$$\mu_s - \frac{\mu_0}{[1 + \theta(V_{GS} - V_{T_0})][1 + \beta N_{it}(y, t_s)]} \tag{5}$$

θ and β are fitting constants.

$N_{it}(y, t_s)$ is the defect density created during stress, it is modeled [9] by:

$$N_{it}(y, t_s) = N_{it_{max}}(t) \exp\left(\frac{-(y - y_c)^2}{2\sigma(t_s)^2}\right)^n \tag{6}$$

where:

$$\begin{cases} N_{it_{max}}(t_s) = \dfrac{a}{S_e V_t} t_s^n \left(\dfrac{I_{DS}}{W}\right)^n \\ \sigma(t_s) = \sigma_0 + b\log(t_s) \end{cases} \tag{7}$$

W is the channel width, I_{DS} is the drain current. $S_e = 10^{-15}\,\text{cm}^2$ is the average capture cross section, $V_t = 10^7\,\text{cm/s}$ is the thermal velocity, the exponent n has been found to range between 0.5 and 0.75 [10,11]. In our simulation it is taken equal to 0.5. σ_0 is regarded as an effective impact ionization length [12].

Using Eqs. (1)–(6) drain current:

$$I_{DS} = W\mu_s C_{ox}[V_{GS} - V_{th} + \Delta V_T - F_B(V_{CS_1}(y) + R_s I_{DS})]E_y - \frac{I_{DS}}{E_{sat}}E_y \tag{8}$$

where:

$$V_{CS_1}(y) = V(y) - R_S I_{DS} \tag{9}$$

Integrating Eq. (8) from $y = 0$ to $y = L$ and assuming that $dV_{CS_1} \approx dV_{CS_1}/dydy \approx V_{D_1S_1}/L$, we obtain:

$$I_{DS} = \frac{\bar{\mu}_s W C_{ox}\left[V_{GS} - \overline{V_{th}} + \Delta V_T - \frac{F_B}{2} V_{D_1S_1}\right] V_{D_1S_1}}{L + \frac{V_{D_1S_1}}{\overline{E_{sat}}} + \bar{\mu}_s W C_{ox} R_S F_B V_{D_1S_1}} \tag{10}$$

where:

$$\begin{cases} \overline{V_{th}} = V_{T_0} - \dfrac{q\,\overline{N_{it}(y, t_s)}}{C_{ox}} \\ \overline{\mu_s} = \dfrac{\mu_0}{[1 + \theta(V_{GS} - V_{T_0})][1 + \beta\overline{N_{it}(y, t_s)}]} \\ \overline{E_{sat}} = \dfrac{2\vartheta_{sat}}{\overline{\mu_s}} \end{cases} \tag{11}$$

The spatial average of the defect density $\overline{N_{it}(y, t_s)}$ expressed as:

$$\overline{N_{it}(y, t_s)} = \sqrt{\frac{\pi}{2}}\,\frac{N_{it_{max}}(t_s)\sigma(t_s)}{L}\left[\operatorname{erf}\left(\frac{L - y_c}{\sqrt{2}\sigma(t_s)}\right) + \operatorname{erf}\left(\frac{y_c}{\sqrt{2}\sigma(t_s)}\right)\right] \tag{12}$$

where erf denotes the error function.

From Eq. (11) we can write $V_{D_1S_1}$ as:

$$V_{D_1S_1} = \frac{-V_2 - \sqrt{V_2^2 - 4V_1V_3}}{2V_1} \tag{13}$$

where V_1, V_2 and V_3 are given by the following expressions:

$$\begin{cases} V_1 = \dfrac{\bar{\mu}_s F_B W C_{ox}}{2} \\ V_2 = \dfrac{I_{DS}}{\overline{E_{sat}}} - \bar{\mu}_s W C_{ox}[V_{GS} - \overline{V_{th}} + \Delta V_T - F_B R_s I_{DS}] \\ V_3 = I_{DS} L \end{cases} \tag{14}$$

By substituting Eq. (14) in (1), the drain current in the linear region can be expressed as:

$$I_{DS} = \frac{-I_2 - \sqrt{I_2^2 - 4I_1 I_3}}{2I_1} \tag{16}$$

where:

$$\begin{cases} I_1 = V_1 (R_S + R_D)^2 - \left(\dfrac{1}{\overline{E_{sat}}} + \bar{\mu}_s W C_{ox} F_B R_s\right)(R_S + R_D) \\ I_2 = \left(\dfrac{1}{\overline{E_{sat}}} + \bar{\mu}_s W C_{ox} F_B R_s\right) V_{DS} - 2(R_S + R_D) V_1 V_{DS} \\ \qquad + \bar{\mu}_s W C_{ox} (R_S + R_D)[V_{GS} - \overline{V_{th}} + \Delta V_T] + L \\ I_3 = -\bar{\mu}_s W C_{ox}[V_{GS} - \overline{V_{th}} + \Delta V_T] V_{DS} + V_1 V_{DS}^2 \end{cases}$$

When V_{DS} increases, the carrier velocity reach the saturation for high V_{DS} values. The saturation channel voltage V_{dsat} is derived by letting Eq. (8) equal to the expression (10):

$$V_{dsat} = \frac{-Z_5 - \sqrt{Z_5^2 - 4Z_4 Z_6}}{2Z_4} \tag{17}$$

where:

$$\begin{cases} Z_1 = V_{GS} - (V_{T_0} - \Delta V_T) \\ Z_2 = 1 + WC_{\text{ox}}\vartheta_{\text{sat}}F_B R_S \\ Z_3 = 1 + WC_{\text{ox}}\overline{\mu_s}\overline{E_{\text{sat}}}F_B R_S \\ Z_4 = F_B(Z_2 - Z_3) \\ Z_5 = Z_3\left(Z_1 - q\dfrac{N_{it}(L,t_s)}{C_{\text{ox}}}\right)Z_1 - 2Z_2\left(Z_1 - q\dfrac{\overline{N_{it}(y,t_s)}}{C_{\text{ox}}}\right) - F_B L\overline{E_{\text{sat}}} \\ Z_6 = \left(Z_1 - q\dfrac{N_{it}(L,t_s)}{C_{\text{ox}}}\right)\overline{E_{\text{sat}}}L \end{cases} \tag{18}$$

The saturation current $L_{d\text{sat}}$ is determined while replacing $V_{D_1S_1}$ with $V_{d\text{sat}}$ in Eq. (10):

$$I_{d\text{sat}} = \frac{\bar{\mu}_s WC_{\text{ox}}\left[V_{GS} - \overline{V_{th}} + \Delta V_T - \dfrac{F_B}{2}V_{d\text{sat}}\right]V_{d\text{sat}}}{L + \dfrac{V_{d\text{sat}}}{\overline{E_{\text{sat}}}} + \bar{\mu}_s WC_{\text{ox}}R_S F_B V_{d\text{sat}}} \tag{19}$$

The saturation extrinsic drain voltage $V_{d\text{sat}}$ can be expressed as:

$$V_{d\text{sat}} = V_{d\text{sat}} + (R_s + R_d)I_{d\text{sat}} \tag{20}$$

In order to have a smooth transition between linear and saturation regions, an effective drain voltage was used [12]:

$$V_{DSE} = V_{d\text{sat}}\left(1 + \frac{\text{In}[1 + \exp(A(1 - V_{DS}/V_{d\text{sat}})]}{\text{In}[1 + \exp(A)]}\right) \tag{21}$$

A is a fitting parameter that is extracted from experimental data.

When V_{DS} becomes greater than $V_{d\text{sat}}$, the pinch-off region increases which results in a reduction of the channel length toward $L_{\text{eff}} = L - \Delta L$. To determine the modulated channel length, we

assume that the inversion charge is a constant in the saturation region. Hence, Eq. (8) can be written as:

$$\frac{\partial^2 V_{CS_1}}{\partial y^2} - k'^2 V_{CS_1} = k'^2 \left[(V_{DSE} - (R_s + R_d) I_{DS}) - \frac{\Delta V_T}{F_B} - q \frac{N_{it}(y, t_s) - N_{it}(L, t_s)}{C_{ox} F_B} \right] \quad (22)$$

where:

$$k'^2 = k^2 F_B$$

The boundary conditions at the pinch-off points are:

$$\begin{cases} V_{CS_1}(y = L_{eff}) = V_{DSE} - (R_s + R_d) I_{DS} \\ E(y = L_{eff}) = E_{sat}(1 + \beta N_{it}(L_{eff})) \end{cases} \quad (23)$$

Using Eq. (23), the resolution of Eq. (22) gives the channel potential in the saturation region:

$$V_{CS_1}(y) = (V_{DSE} - (R_s + R_d) I_{DS}) + \frac{E_{sat}}{k'}(1 + \beta N_{it}(L_{eff}))\sinh(k'(y - L_{eff})) + q \frac{\Delta V_T - N_{it}(y, t_s)}{C_{ox} F_B}(\cosh(k'(y - L_{eff})) - 1) + k' \int_{L_{eff}}^{y} q \frac{N_{it}(y', t_s)}{C_{ox} F_B} \sinh(k'(y - y'))dy' \quad (24)$$

Known that, $V_{CS_1}(y = L) = V_{DS} - (R_s + R_d) I_{DS}$, numerical resolution of Eq. (24) gives ΔL.

Replacing L by $L - \Delta L$ and V_{DS} by V_{DSE} in Eq. (16), provides the drain current.

III. SIMULATION RESULTS

The parameters of the transistor used in the simulation are given in Table I.

TABLE I

Parameters	Values
L	0.6 μm
W	40 μm
T_{ox}	14 nm
X_j	0.15 μm
N_A	$6.5\ 10^{16}\,cm^{-3}$
θ	$0.18\ V^{-1}$
β	$2.5\ 10^{-12}\,cm^2$
μ_0	$580\,cm^2/Vs$
ϑ_{sat}	$7.10^6\,cm/s$

III.1. Impact on $I_{DS} - V_{DS}$ Characteristic

Figure 2 represents the variation of the $I_{Ds} - V_{DS}$ characteristic for two gate bias (3 V and 5 V) before and after stress. The curves of this figure show that the drain current decreases when increasing stress time, which is due to the mobility degradation. In saturation mode part, the interface states are in velocity saturation region and can be depleted, therefore the effect of these interface state becomes insig-

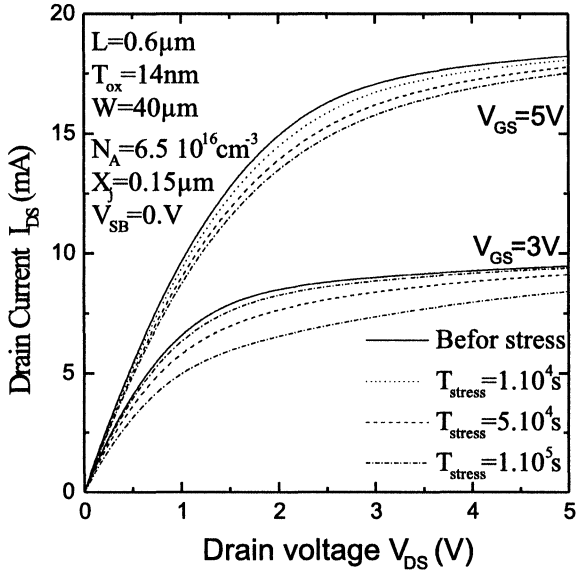

FIGURE 2 Variation of the $I_{DS} - V_{DS}$ characteristic versus stress time.

nificant. Moreover, after pinch-off, the channel current is governed by the inverted channel between the source and the drain pinch-off, so it becomes virtually independent of the region between the pinch-off point and drain junction. Since the defects are mostly located in this region near the drain, its influence upon the drain current becomes less in saturation.

Figure 3 shows the variation of the drain current drift versus stress time for different drain bias. The degradation of the drain current drift increases with stress time. Also notice that the degradation the delta decrease when the drain bias increase.

III.2. Impact on the Transconductance

The curves of Figure 4 show that the stress acts on the transconductance, which decreases with, the stress time. The degradation of the transconductance is due to the mobility reduction caused by the increase of the defect density during stress time. This transconductance degradation is reduced as the gate voltage increase. Indeed, when the

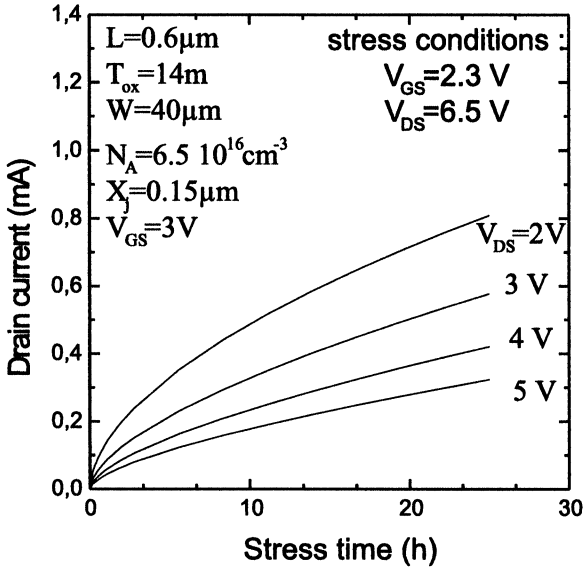

FIGURE 3 Evolution of the drain current drift with stress time for different drain bias.

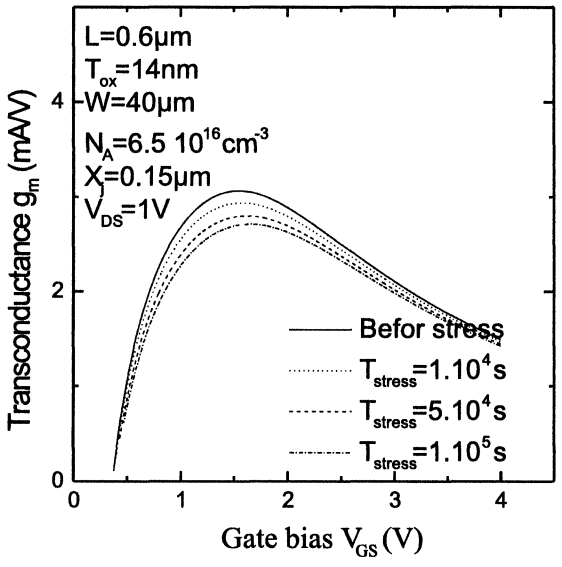

FIGURE 4 Transconductance variation during stress time.

gate voltage increase, the carrier density in the inversion layer increase and the effects of coulomb scattering are reduced by the screening effect. Thus, the degradation of transconductance is less significant. Exhibit ■

The evolution of the ratio, between the transconductance drift Δg_m and the transconductance initial value g_{m_0} (before stress), versus stress time is sketched on Figure 5. This figure show that the evolution of the $\Delta g_m/g_{m_0}$ is linear, in logarithmic scale, what is qualitatively agree with the results given in the literature [13–15].

IV. CONCLUSION

The modeling of the current drain in relation with interface defects created during stress time is very important. Since, it allows us to understand the aging phenomenon and the amount degradation of the performances of the devices. The simulations results show that the stress leads to the degradation of the I–V characteristic and the re-

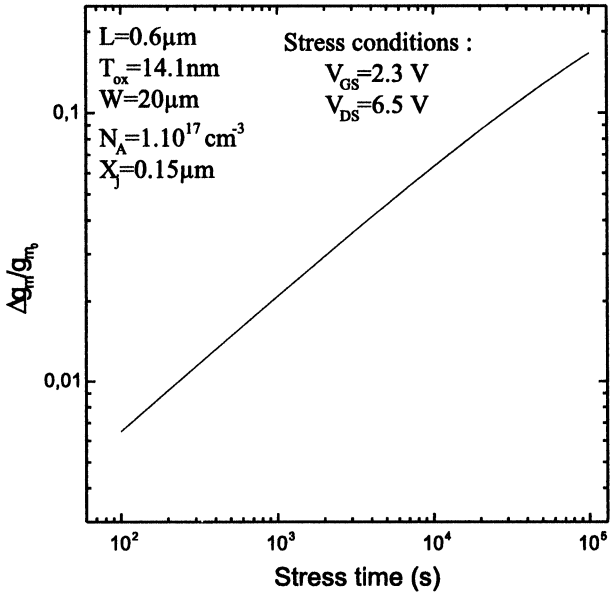

FIGURE 5 Impact of the stress on the transconductance drift.

duction of the transconductance. The model can be applied to the simulation of device behavior after stress in order to improve the circuit long-term reliability.

References

[1] J. J. Yang, S. S. S. Chung, P. C. Chou, C. H. Chen and M. S. Lin (1995) *IEEE Trans. Electron. Devices* **42**, 1113–1119.
[2] Y. B. Park and D. K. Schroder (1998) *IEEE Trans. Electron. Devices* **45**, 1361–1368.
[3] A. Bouhdada, S. Bakkali and A. Touhami (1997) *Microelectronics and Reliability Journal* **37**, 649–652.
[4] A. Bouhdada, S. Bakkali, A. Nouaçry and A. Touhami (1997) *Microelectronics Journal* **28**, 85–91.
[5] A. Bouhdada, A. Nouaçry, S. Bakkali, A. Touhami and R. Marrakh (1999) *Microelectronics Journal* **30**, 19–22.
[6] H. H. Li, Y. L. Chu and C. Y. Wu (1997) *IEEE Trans. Electron. Devices* **44**, 782–791.
[7] C. Chen and T. P. Ma (1998) *IEEE Trans. Electron. Devices* **45**, 512–520.
[8] D. S. Ang and C. H. Ling (1998) *IEEE Trans. Electron. Devices* **45**, 149–159.
[9] A. Bouhdada and R. Marrakh (2000) *Active and Passive Elec. Comp.* **00**, 1–8.
[10] J. Oualid, S. Burgnlard, E. Ciantar and R. Jérisian (1993) *Microelectronic Reliability* **33**, 1759–1777.

[11] T. Tsuchy and J. Frey (1985) *IEEE Electron Devices Lett.* **6**, 8–11.
[12] N. Arora (1992) *MOSFET Models for VLSI Circuit Simulation* (Springer-Verlag, Wien New York) pp. 167–225.
[13] Y. Leblebici and S. M. Kang (1993) *Hot Carrier Reliability of MOS VLSI Circuits* (Kluwer Academic Publishers) pp. 84–85.
[14] M. Song, K. P. MacWilliams and J. C. S. Woo (1997) *IEEE Trans. Electron. Dev.* **44**, 268–275.
[15] E. Takeda, C. Y. Yang and A. M. Hamada (1995) *Hot-carrier Effects in MOS Devices* (Academic Press, INC) pp. 78–79.