ANALYSIS OF TEMPERATURE AND DRAIN VOLTAGE DEPENDENCE OF SUBSTRATE CURRENT IN DEEP SUBMICROMETER MOSFET'S

Y. AMHOUCHE, A. EL ABBASSI, K. RAÏS* and R. RMAILY

*Laboratoire de Caractérisation des Composants à Semi-conducteurs,
Université Chouaib Doukkali B.P. 20, EL Jadida-Maroc*

In this paper, a detailed experimental study of channel length, drain voltage and temperature dependence of substrate current $Isub$ in submicrometer MOSFET's is presented. Impact ionization rate α is remarkably increased with decreasing channel length L and go up from 10^{-7} to $6, 7 \cdot 10^{-7}$ when L decrease from 2 to 0.1 µm, this behaviour found expression in a fast increase of the substrate current maximum $Isub_{max}$. Moreover it is observed that contrarily of long channels, low temperature operation is favourable to reduce hot carrier effects in submicrometer MOSFET's and may represent a promising alternative for the improvement of the performances of Si integrated circuits.

Keywords: Submicrometer MOSFET's; Impact ionization; Substrate current; Temperature; Channel length

1. INTRODUCTION

The scaling down of the MOSFET devices has allowed the increase of the integration density and of the speed of integrated circuits. However, the reduction device dimensions increase the longitudinal and transversal fields and induce secondary effects which leads to a performance degradation of the device and to less reliability [1,2].

One of these effects is the increase of impact ionisation with reducing channel length, since, in the submicrometer regime, hot carriers gen-

*Corresponding author.

eration is practically extended on all the channel area [3]. The saturated region length becomes comparable to the channel dimension and the channel pinch near drain is partial which will be interpreted in *Isub* (*Vg*) apparition, *Vg* being the gate voltage, by a slow decrease of the substrate current beyond the maximum $Isub_{max}$.

In this work, substrate current proprieties in very short channel MOSFET's in function of channel length, temperature and drain voltage are experimentally discussed. The study of impact ionization and the parameters *A* and *B* figuring in the substrate current law show that the reduction of channel length is unavoidably accompanied by the increase of $Isub_{max}$.

In the other hand, though the application of a substrate bias allowed in same cases the decrease of substrate current [4], it is shown that low temperature operation can be used, in function of the considered drain bias, as an other alternative to reduce hot carrier effects.

2. THEORETICAL DETAILS

According to the lucky electron model [5], impact ionization rate is given by

$$\alpha = C \cdot (Vd - Vd_{\text{sat}}) \cdot \exp\left[-\frac{B}{(Vd - Vd_{\text{sat}})}\right] \qquad (1)$$

where *C* is an empirical constant, Vd_{sat} is the drain saturation voltage and *Vd* represent the drain voltage. *B* is an empirical constant related to the impact ionization law coefficient *bi* as:

$$B = l \cdot bi = \frac{l \cdot \phi}{\lambda \cdot q} \qquad (2)$$

where ϕ, *l*, *q* and λ are the critical energy for impact ionization, the characteristic length of the saturated region, the electronic charge, and the hot electron mean free path respectively. For $L < 1.5\,\mu\text{m}$, *l* can be expressed by [6]:

$$l = 1,7 \cdot 10^{-2} \cdot t_{ox}^{1/8} \cdot x_j^{1/3} \cdot L^{1/5} \qquad (3)$$

where t_{ox} and x_j are the gate oxide thickness and the junction depth respectively. In addition, the substrate current can be derived as:

$$Isub = \alpha \cdot Id = C \cdot Id \cdot (Vd - Vd_{\text{sat}}) \cdot \exp\left[-\frac{B}{(Vd - Vd_{\text{sat}})}\right] \quad (4)$$

Id being the drain current. Therefore a satisfactory modelling of the substrate to drain current ratio can be obtained over whole temperature range 20–300 K by using the simple substrate current law [7,8]

$$Isub = \alpha \cdot Id = A \cdot Id \cdot \exp\left[-\frac{B}{(Vd - Vd_{\text{sat}})}\right] \quad (5)$$

where A is an empirical constant. The Eqs. (3, 4, 5) show that the essential parameters determining hot carrier generation in the saturation regime are drain saturation voltage and characteristic length of the velocity saturated region and all bias conditions and devices parameters are included in Vd_{sat} and l.

3. RESULTS AND DISCUSSION

The parameters of the devices investigated are: gate oxide thickness 5 nm, channel width 4 μm, channel length 0.1–10 μm and channel doping $\approx 10^{16}/\text{cm}^3$.

a) Channel length reduction effect

The constants A and B have been extracted from the y axis intercept and slope of the plots $Isub/Id$ versus $1/(Vd - Vd_{\text{sat}})$ respectively. Figures 1 and 2 displays the evolution with channel length of these parameters at $T = 300$ K and $Vd = 2.5$ V. For $L > 1.5$ μm, B is constant (32 V) which is in good agreement with the theoretical law given by [9]. On the other hand, for $L < 1.5$ μm. The coefficient B decrease remarkably as expected by Eq. (3), the coefficient A follows the same evolution versus channel length than B and varies from 12 for $L > 1.5$ μm down to 8 for $L = 0.3$ μm. This behaviour can be explained by a channel length dependence of the parameter A as soon as the effective ionization length becomes function of channel length which is the case for submicrometer MOSFET's. The study of channel length dependence of impact ionization (Fig. 3) show an abrupt augmentation of α with decreasing L which go up from 10^{-9} to $6, 7 \cdot 10^{-9}$ when
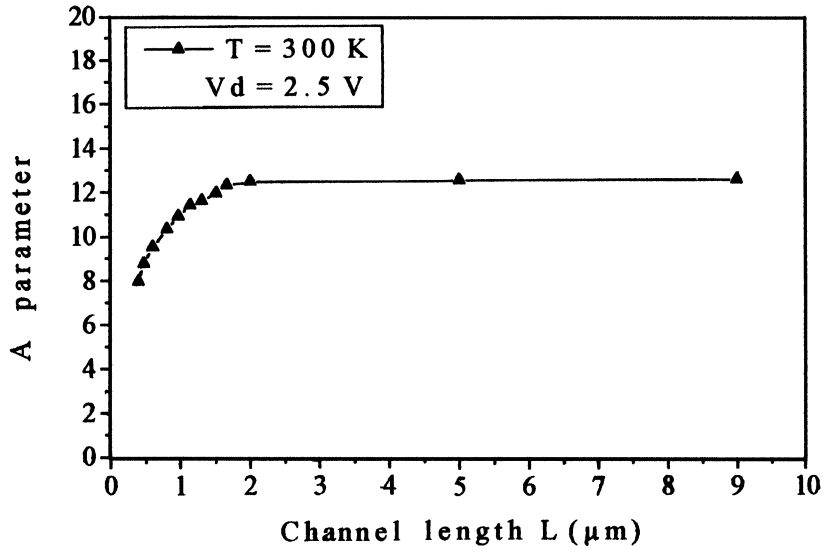
FIGURE 1   *A* parameter versus channel length at $T = 300$ K and $Vd = 2.5$ V.
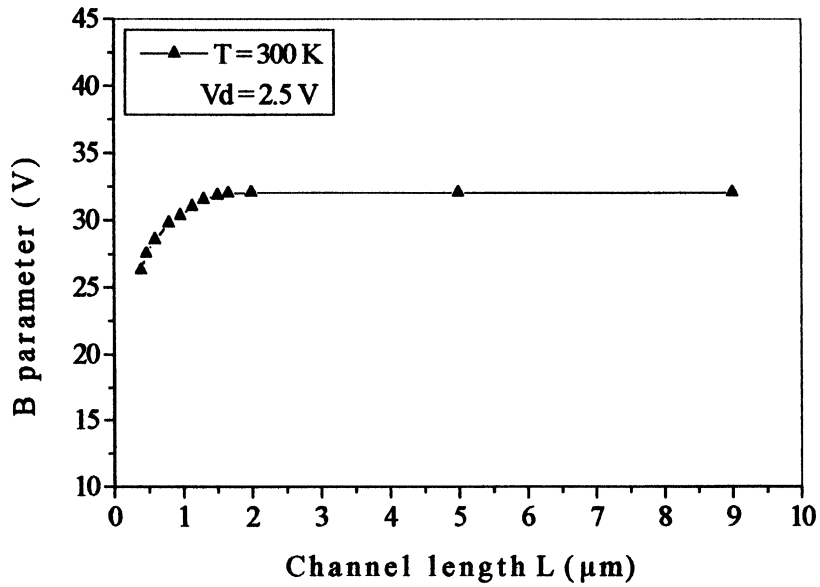
FIGURE 2   *B* parameter versus channel length at $T = 300$ K and $Vd = 2.5$ V.

L varies from 2 down to 0.1 μm. The increase of α becomes very strong from $L = 0.4$ μm. In Figure 4 is shown $Isub_{max}$ variation with channel length for $Vd = 2.5$ V and $T = 300$ K, $Isub_{max}$ is exponentially increased with L which explain that hot carrier effects are very dominants in very short channel lengths.

b) Temperature and drain bias effect.

If low temperature operation increase the substrate current maximum in long channel MOSFET's [10], a decrease of $Isub_{max}$ is shown for very short channel MOSFET's in the considered bias conditions. In Figure 5 is displaying the evolution of $Isub_{max}$ with temperature for $L = 0.3$ μm channel length and for different drain bias. For $Vd = 1.9$ V, $Isub_{max}$ increase from 30 nA up to 40 nA when T varies between 25 and 300 K. For $T < 25$ K, an unexpected increase of $Isub_{max}$ is observed. This behaviour is probably to a very large increase of effective mobility and as result of drain current and $Isub_{max}$. In Figures 6 and 7 respectively is shown the evolution of the coefficients A and B versus
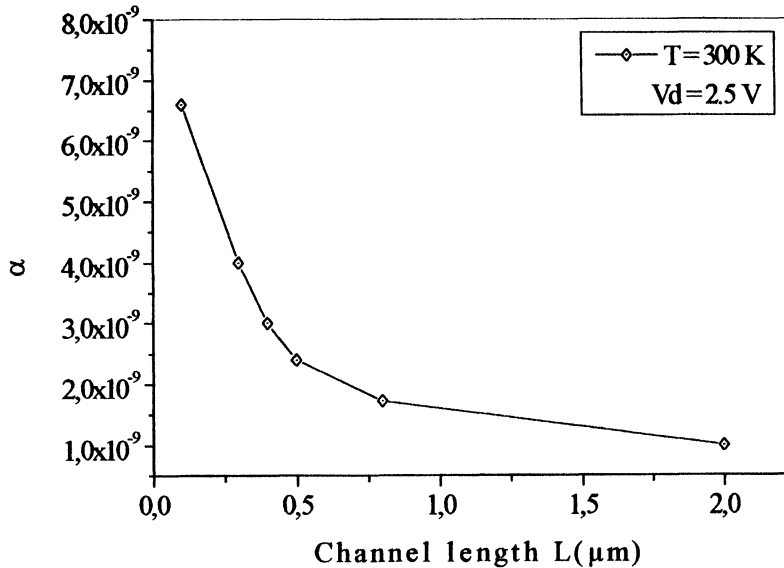

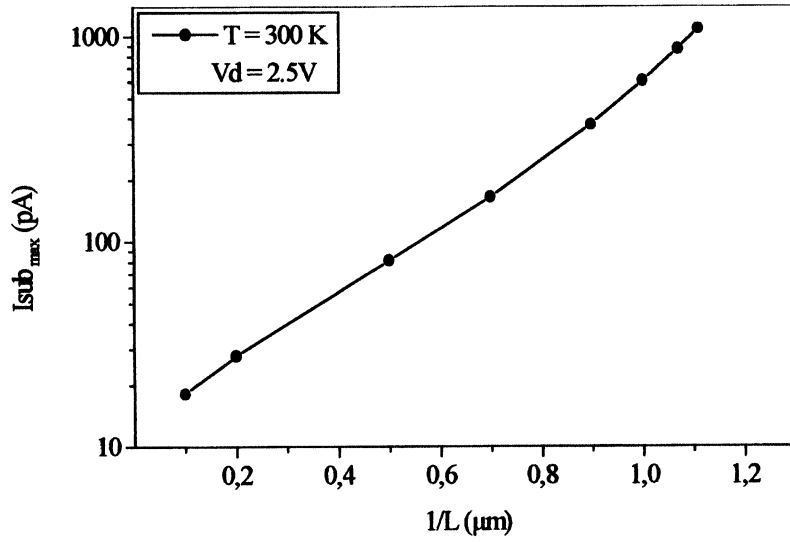FIGURE 3   Impact ionization rate against channel length characteristic at $T = 300$ and $Vd = 2.5$ V.

FIGURE 4   *Isub*$_{max}$ versus $1/L$ characteristic at $T = 300\,$K and $Vd = 2.5\,$V.

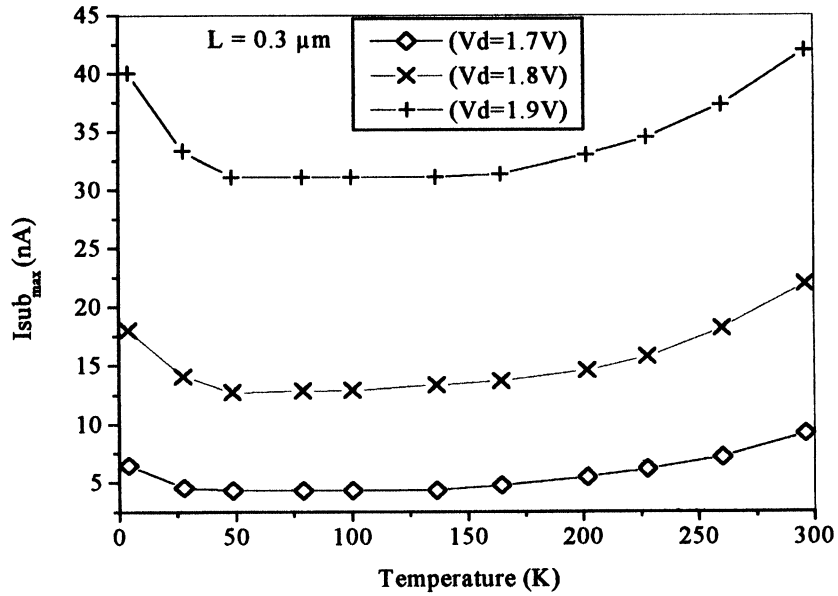FIGURE 5   *Isub*$_{max}(T)$ characteristic for $0.3\,\mu$m channel length and different drain voltages.

temperature for $L = 0.3\,\mu m$ channel length. The coefficient B is almost constant (25 V) but takes a value smaller than that founded for long channel transistors while A is an increasing function of temperature contrarily to long channel case.

In order to show simultaneously the drain bias and temperature effect, we have defined $\Delta Isub_{max}$ as follows:

$$\Delta Isub_{max}(T) = \frac{Isub_{max}(T)}{Isub_{max}(300\,K)} \qquad (6)$$

The Figure 8 represent the evolution of $\Delta Isub_{max}$ versus drain voltage for $L = 0.12\,\mu m$ channel length and shows clearly the cross-over voltage Vd_c which define the $Isub_{max}$ variation modes with temperature [11]. As seen in this figure, $\Delta Isub_{max}$ evolution against drain voltage can be divided into two principal regions. Indeed, for $Vd < Vd_c$, $Isub_{max}$ is an increasing function of Temperature while for $Vd > Vd_c$, hot carriers effects increase with decreasing temperature, for $Vd = Vd_c$, $Isub_{max}$ is not sensitive to temperature. The cross-over phenomena is generally governed by the temperature dependence degree of effective mobility and impact ionisation rate. The knowledge of this voltage
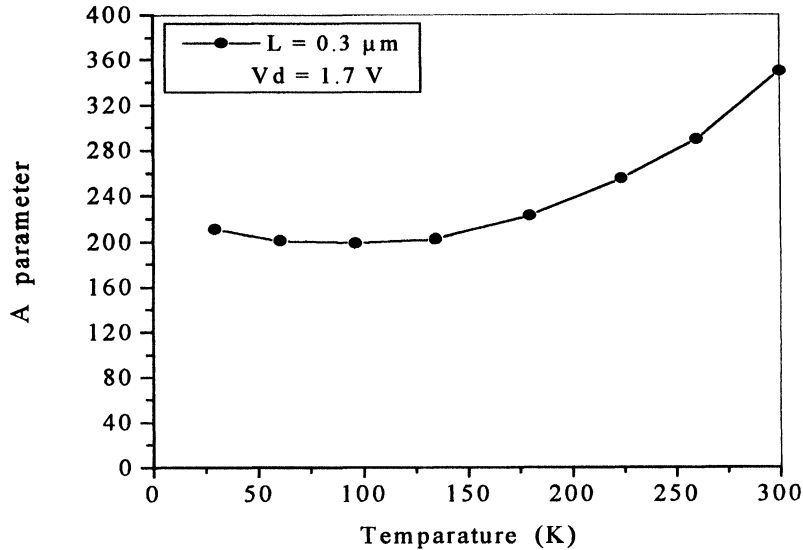

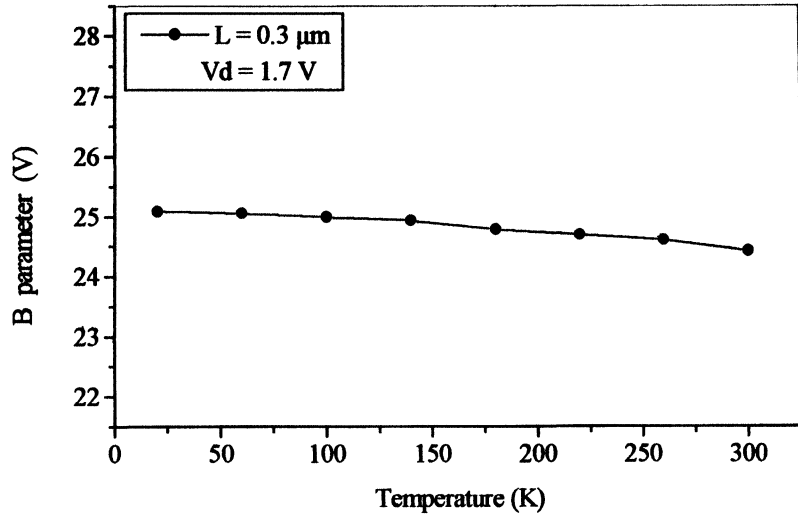FIGURE 6 B parameter evolution with temperature for $0.3\,\mu m$ channel length and $1.7\,V$ drain voltage.

FIGURE 7   *A* parameter evolution with temperature for 0.3 µm channel length and 1.7 V drain voltage.
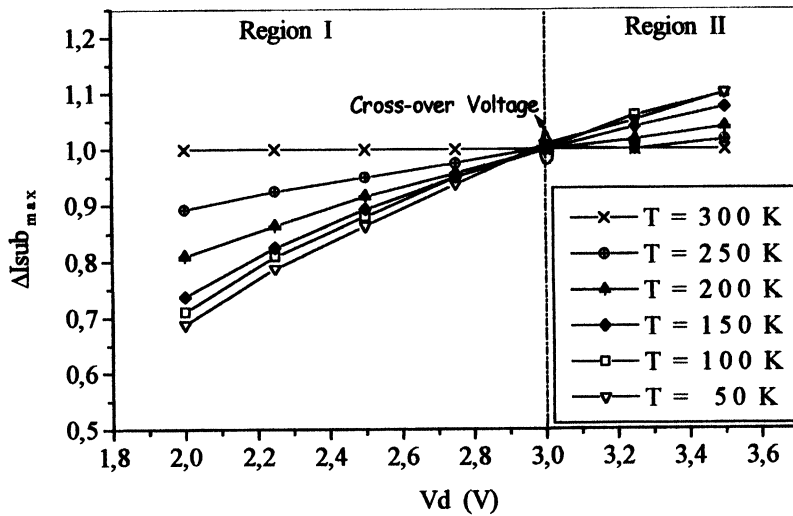

FIGURE 8   Observation of the cross-over voltage from the relative variation of *Isub*$_{max}$ against drain voltage for different temperatures. ($L = 0.12$ µm).

appears very useful for determining the influence of drain bias on the substrate current against temperature evolution and give a good idea on the choice of the best drain voltage with which $Isub_{max}$ can be minimised. Generally, the rated voltages of submicrometer MOSFET's are lesser than Vd_c (3 V in our case), this fact allowed to consider that low temperature operation is favourable to reduce hot carrier effects.

4. CONCLUSION

In this work, temperature and channel length dependence of substrate current in Submicrometer MOSFET's has been investigated. It has been shown that impact ionization is rapidly increased with reducing channel length. On the other hand the exponent factor B has been found to be almost constant with temperature. Moreover, it has been observed that the maximum substrate current increase with increasing temperature which allowed to consider low temperature operation as an other way to reduce hot carrier effects in submicrometer MOSFET's.

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