Research Article

Electronically Tunable Dual-Input Integrator Employing a Single CDBA and a Multiplier: Voltage Controlled Quadrature Oscillator Design

R. Nandi,[1] Mousiki Kar,[2] and Sagarika Das[3]

[1] *Department of Electronics & Telecommunication Engineering, Jadavpur University, Kolkata-700032, India*
[2] *Department of Electronics & Communication Engineering, Heritage Institute of Technology, Kolkata-700107, India*
[3] *Department of Electronics & Communication Engineering, B.P. Poddar Institute of Management & Technology, Kolkata-700052, India*

Correspondence should be addressed to R. Nandi, robnon@ieee.org

A new dual-input differential input active integrator using a current differencing buffered amplifier (CDBA) is proposed. A multiplier element is appropriately used in the circuit whose control voltage (V_c) tunes the integrator time constant (τ) electronically. The design of a voltage controlled quadrature oscillator (VCQO) based on the proposed integrator had been satisfactorily implemented. A new type of measurement for the tuning error of the oscillator based on the Nyquist plot is presented that shows an error of only 2% at $fo \approx 1$ MHz with Total Harmonic Distortion (THD) less than 3%.

1. Introduction

With the advent of the CDBA building block [1, 2], various analog signal processing/conditioning circuit realisation schemes using this element appeared in the recent literature [2–6]. The CDBA offers several advantageous features viz., high slew rate, improved bandwidth, and accurate port tracking characteristics when configured with a pair of matched current feedback amplifier (AD-844-CFA) devices [3, 4] which leads to extremely low active circuit sensitivity. We propose here a new electronically tunable differential integrator using a CDBA; the control voltage (V_c) of a multiplier element, incorporated suitably in the circuit, tunes τ electronically.

The ICL-8013 device is a four-quadrant analog multiplier whose output is proportional to the electronic product of two input voltage signals with a transmission constant $k$volt^{-1} [7, 8]. The high accuracy ($\pm 1\%$), relatively wide bandwidth (B = 1 MHz), and improved versatility make it quite suitable for analog signal conditioning and active filter design applications.

Albeit various CDBA-based active filters/oscillators [3–6] are now available, the feature of electronic tuning in the CDBA active function circuit had not yet been reported. The design of a voltage controlled quadrature oscillator (VCQO) had then been implemented using the double integrator loop. The proposed functions had been verified by PSPICE macromodel simulation of the AD-844 based CDBA and by hardware circuit tests.

2. Analysis

The proposed circuit is shown in Figure 1. The nodal equations characterizing an ideal CDBA element are $i_z = i_p - i_n$, $V_0 = v_z$, $v_p = 0 = v_n$ [1]. Analysis with these port relations for the CDBA [1–4] and writing the multiplier [7, 8] output $= kV_oV_c$ where $k \equiv$ multiplier constant = 0.1 per volt [9] yield

$$(V_1 y_1 - V_2 y_2) = V_0 [y_4 + g_z - y_3 + s\{C_z + C(1 - kV_C)\}] \tag{1}$$
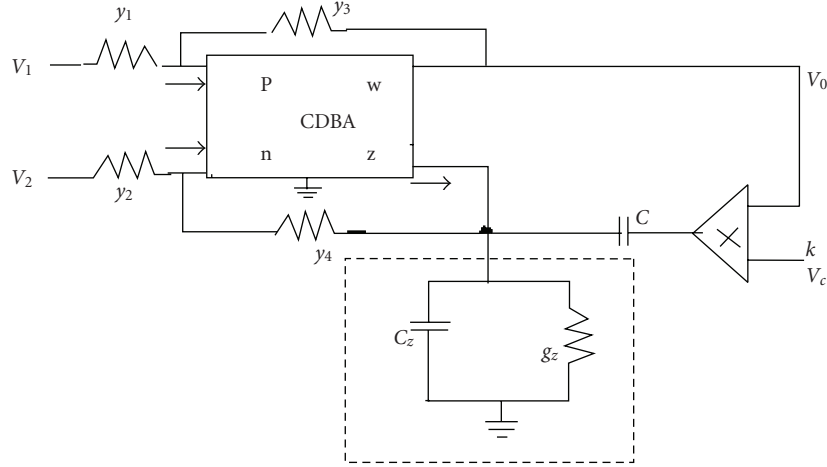
FIGURE 1: Voltage (V_c) tunable differential integrator using CDBA-multiplier composite block.

TABLE 1: S_f values for some recent CDBA-based quadrature-oscillators.

Ref.	Electronic tunability	fo-tuning range (MHz) reported	S_f
[3]	No	0.02	$\approx 2n(1-\varepsilon) \approx 2n$
[4]	No	0.01	$2/(1+2\varepsilon) \approx 2$
[6]	No	0.02	$n(2-3\varepsilon) \approx 2n$
Proposed	Yes	1.02	$2n(2-3\varepsilon) \approx 4n \gg 1$

where $Y_z = (g_z + sC_z)$ denotes the shunt parasitic transadmittance at z node of the CDBA; as per datasheet [10] $g_z = 0.2\,\mu$ mho and 5 pf $\leq C_z \leq$ 8 pF.

We therefore get the realisability conditions for a true differential integrator, putting $y_i = 1/R_i$; $i = 1$ to 4, as

$$R_2 = R_1$$
$$\frac{R_4}{R_3} = \frac{2}{\{1 - (R_3/r_z)\}} \approx 2 \quad (2)$$

here we assumed $R_3/r_z \ll 1$. With (2) in (1), an ideal dual-input integrator function is obtained as

$$\frac{V_0}{(V_1 - V_2)} \equiv F(s) = \frac{1}{s\tau} \quad (3)$$

where $\tau = RC(1 + m - kVc)$; if $m = C_z/C \ll 1$, then $\tau = RC_0$ with $C_0 \approx (1 - kVc)C$. Hence the time constant (τ) is electronically tunable for the range $0 \leq Vc \leq 10$ V d.c.

With a nonideal CDBA device, these design equations would alter. The device imperfections may be expressed in terms of some port mismatch ratios [2–4] given by the relations

$$i_z = \alpha_p i_p - \alpha_n i_n, \quad V_0 = \delta v_z. \quad (4)$$

The p and n terminals of the CDBA however are internally grounded; hence $v_p = 0 = v_n$. In the literature, the mismatch ratios are postulated in terms of some low-magnitude error [2–6] quantities $|\varepsilon| \ll 1$, given by $\alpha_p = 1 - \varepsilon_1$, $\alpha_n = 1 - \varepsilon_2$, and $\delta = 1 - \varepsilon_o$; for an ideal device the errors vanish.

By Reanalysis assuming finite ε quantities, we get a modified transfer equation

$$\left(V_1 y_1 \alpha_p - V_2 y_2 \alpha_n\right)\delta = V_0\Big[(1 + \alpha_n)y_4 + g_z - \delta\alpha_p y_3$$
$$+ s\{C_z + C(1 - kV_C\delta)\}\Big]. \quad (5)$$

The realisability conditions for a true differential integrator now modify to

$$\frac{R_2}{R_1} = 1 + \Delta\varepsilon; \quad \varepsilon_1 - \varepsilon_2 = \Delta\varepsilon \ll 1$$
$$\frac{R_4}{R_3} = \frac{[2 - \varepsilon_o - \varepsilon_2]}{[1 - (R_3/r_z) - (\varepsilon_0 + \varepsilon_1)]} \approx 2 + \varepsilon_t. \quad (6)$$

Here we neglect the error products since $\varepsilon \ll 1$; thus $\varepsilon_t = \varepsilon_0 + 2\varepsilon_1 - \varepsilon_2$.

The active τ-sensitivity may be estimated after writing $\varepsilon_{0,1,2} = \varepsilon$ for simplicity, which gives $s^\tau \approx 2\varepsilon/(1+2\varepsilon) \ll 1$ since $0.01 \leq |\varepsilon| \leq 0.03$ [4, 11, 12]. Effect of the multiplier device nonideality may be derived by expressing $k = (1 - \varepsilon_m)$ volt^{-1} so that we can effectively write $kV_c = (1 - \varepsilon_m)$ for sensitivity calculation, which yields $|S^\tau \varepsilon_m| \approx \varepsilon_m/(1 - \varepsilon_m) \ll 1$.

In this analysis, we neglected the parasitic series resistance ($r_p \approx 30$ ohm) [12] of the CDBA and noted that the n-node parasitics are bypassed to ground since $V_p = 0 = V_n$. The integrator quality factor (Q) may be evaluated after writing $F(\omega) = (p + jq)$ and then deriving $Q = q/p$, given by
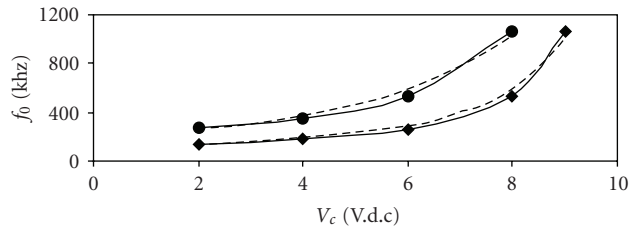
$$Q = \frac{(\omega C'_o R_4)}{2 + \varepsilon_t - (R_4/R_3)} \quad (7)$$

TABLE 2: Tuning error and THD measured at three different tuning frequencies.

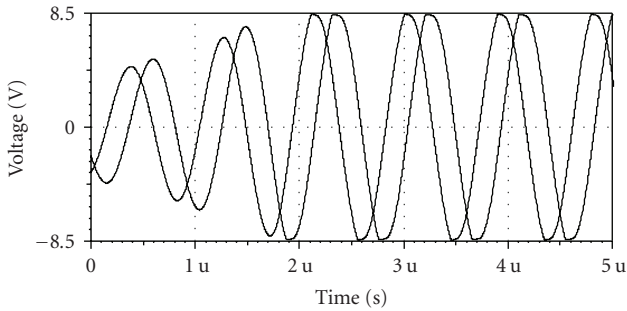| Curve	Tuned frequency f_0 (MHz)	$f\vert_{\theta=0°}$ (MHz)	Δf (MHz)	Tuning error (%)	THD (%)
A	1.00	1.020	0.020	2.00	2.1
B	0.72	0.727	0.007	0.97	1.8
C	0.50	0.498	0.002	0.40	1.5
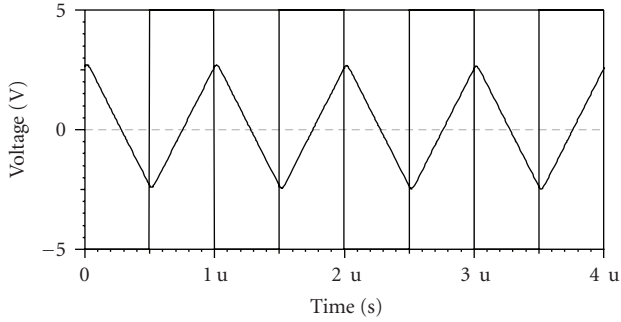
(a) Integrator response with square wave excitation of $V_1 = -V_2 = 2.5\,V$(peak) at 1 MHz using $R_1 = R_2 = R = 10\,K.ohm$, $R_4 = 60\,K.ohm$, $R_3 = 30\,K.ohm$, $C = 100\,pF$, C_z (measured) = 7.2 pF, and $V_c = 5\,V.d.c.$
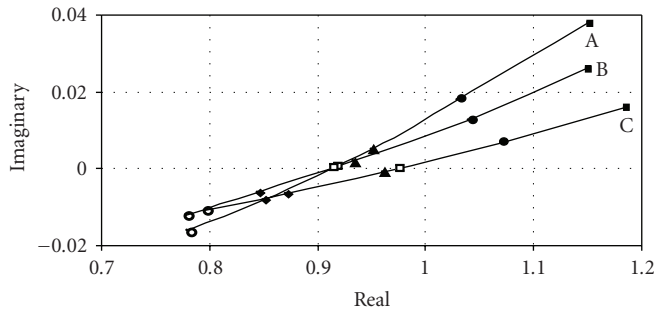
(b) VCQO-tuning characteristics with $C = 1\,nF$

(c) VCQO wave-response with build-up feature tuned for $f_o = 1.02\,MHz$

(d) Nyquist plot of loop function $F_1F_2(s)$ measured in the vicinity of $u = 1 \pm 10\%$ with above keys. Nominal tuned frequency (f_0): A → 1 MHz B → 0.72 MHz C → 0.5 MHz
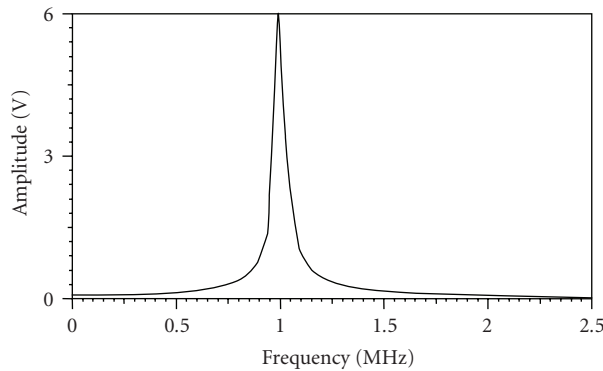
(e) Frequency spectrum of the loop-function $F_1F_2(s)$ measured at the tuned frequency of 1 MHz

FIGURE 2: Experimental results.

where

$$C_o' = \{C_z + C(1 - V_C(1 - \varepsilon_m))\}. \qquad (8)$$

Inspection of (7) indicates the realisability of high quality integration ($Q \gg 1$) where Q may be preset to a high value by R_4, and R_3 sets the realisability while V_c tunes τ electronically and independently. For example, if we assume $\varepsilon(\max) = 10\%$ for a desired $Q = 50$ at $f = 1$ MHz with a typical set of values $V_c = 5$ V d.c., $C = 1$ nF, $C_o' \approx 0.5$ nF, and $R_4 = 10$ KΩ, then from (7) we get $R_3 \approx 5.5$ KΩ.

3. VCQO Design

The quadrature oscillator finds various applications in SSB modulators and spectral phase measurements: its functional capabilities are further enhanced if electronic tuning property can be incorporated. We design a VCQO using the proposed integrator in a two integrator loop, each being used single ended, one inverting and the other in noninverting mode, that is, from (3) we designed $F_1(s) \equiv Vo/V_1 = 1/s\tau$ and $F_2(s) \equiv Vo/V_2 = -1/s\tau$, thereafter cascading the two integrators in a loop.

With identical integrator, the oscillation frequency would be $f_o \approx 0.16/RC(1 - kV_c)$. The frequency stability factor (S_f) is evaluated by $S_f = \Delta\theta/\Delta u$ at $u = \omega/\omega_0 = 1$, where θ is loop phase shift. After putting $n = R_4/R$, we obtained $S_f = 2n(2-3\varepsilon) \approx 4n \gg 1$ since we selected $R_4 \gg R$. A comparison of the S_f values with some recent CDBA based oscillators is listed in Table 1.

4. Simulation and Experimental Results

Both the integrator and VCQO functions have been tested with PSPICE macromodel simulation [13] and by breadboarding hardware circuit after implementing the CDBA block with a pair of AD-844 devices [3] being biased with $V_{cc} = 0 \pm 10$ V.d.c. regulated supply. The results are shown in Figure 2. The responses had been measured for a range of 150 KHz $\leq f \leq 1$ MHz with suitable set of RC components wherein $0 \leq Vc \leq 10$ V d.c. is used for the tunability range taking $k = 0.1$. The ICL-8013 multiplier element is implemented through the Macromodel databook [7–9]. It may be mentioned here that one can select any of the two default values of the multiplier constant $k = 0.1$ and $k = 0.5$ for the ICL 8013 multiplier device [7–9, 13, 14] in order to enhance the tuning range concomitantly while keeping $k V_c \leq 1$ and $\pm V_{c(\max)} \leq V_{cc}$ as the limit.

We tested the frequency response of the integrator with antiphase input sinusoid signals and observed the phase error of about $5.5°$ at 1 MHz. The CMRR had been measured to be 96 dB with sinusoid excitation. It may be seen that the select-frequency was reported in the range of a maximum of 200 KHz in the earlier circuits [3, 4, 6]. Embedding the HA 2557 multiplier device [7, 8] with BW ≈ 130 MHz, in place of the ICL-8013 BW(≈ 1 MHz), it is possible to obtain an extended frequency range.

In order to examine the tuning error in f_0, we had carried out a new type of measurement using the Nyquist

plot of the loop transfer function $F_1F_2(s)$ of the double-integrator loop in the vicinity of f_o, as shown in Figure 2(d). The deviation (Δf) is then computed from the intersection of the function with the real axis of the plot following the Barkhaussen criterion. We obtained three such graphs corresponding to oscillation generation at the nominal frequencies of 500 KHz, 720 KHz, and 1.02 MHz. The tuning error is then derived as shown in Figure 2(e) and Table 2.

5. Conclusion

A new single CDBA-based differential integrator with a multiplier element in the circuit loop is presented for obtaining electronic tunability. Subsequently, a double integrator type VCQO had been designed and tested in a frequency range of 150 KHz–1 MHz with suitable design. Albeit other electronically tuned active realisations were reported recently in relatively lower frequency-range using CFA [14], current conveyors [15, 16], or OTA-based allpass filter [17], such a function circuit using the CDBA had not yet been presented.

References

[1] C. Acar and S. Ozoguz, "A new versatile building block: current differencing buffered amplifier suitable for analog signal-processing filters," *Microelectronics Journal*, vol. 30, no. 2, pp. 157–160, 1999.

[2] S. Özoğuz, A. Toker, and C. Acar, "Current-mode continuous-time fully-integrated universal filter using CDBAs," *Electronics Letters*, vol. 35, no. 2, pp. 97–98, 1999.

[3] J.-W. Horng, "Current differencing buffered amplifiers based single resistance controlled quadrature oscillator employing grounded capacitors," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E85-A, no. 6, pp. 1416–1419, 2002.

[4] A. Ü. Keskin, "Voltage-mode high-Q band-pass filters and oscillators employing single CDBA and minimum number of components," *International Journal of Electronics*, vol. 92, no. 8, pp. 479–487, 2005.

[5] M. Gülsoy and O. Cicekoglu, "Lossless and lossy synthetic inductors employing single current differencing buffered amplifier," *IEICE Transactions on Communications*, vol. E88-B, no. 5, pp. 2152–2155, 2005.

[6] W. Tangsrirat, D. Prasertsom, T. Piyatat, and W. Surakampontorn, "Single-resistance-controlled quadrature oscillator using current differencing buffered amplifiers," *International Journal of Electronics*, vol. 95, no. 11, pp. 1119–1126, 2008.

[7] Intersil Datasheet, file number 2477.5, September 1998.

[8] Intersil Datasheet, file number 2863.4, April 1999.

[9] *Semiconductor Product Databook*, Intersil Corp., Milpitas, Calif, USA, 2000.

[10] *Analog Devices: Linear Products Databook*, Norwood, Mass, USA, 1990.

[11] A. Zeki and H. Kuntman, "Accurate and high output impedance current mirror suitable for CMOS current output stages," *Electronics Letters*, vol. 33, no. 12, pp. 1042–1043, 1997.

[12] B. J. Maundy, A. R. Sarkar, and S. J. Gift, "A new design topology for low-voltage CMOS current feedback amplifiers," *IEEE Transactions on Circuits and Systems II*, vol. 53, no. 1, pp. 34–38, 2006.

[13] *Macromodel of AD844AN in PSPICE Library*, Microsim Corp., Irvine, Calif, USA, 1992.

[14] R. K. Nagaria, A. Goswami, P. Venkateswaran, S. K. Sanyal, and R. Nandi, "Voltage controlled integrator/differentiator using current feedback amplifier," in *Proceedings of the International Symposium on Signals, Circuits and Systems (ISSCS '03)*, vol. 2, pp. 573–576, Iasi, Romania, 2003.

[15] H. Sedef, M. Sagbas, and C. Acar, "Current-controllable fully-integrated inductor simulator using CCCIIs," *International Journal of Electronics*, vol. 95, no. 5, pp. 425–429, 2008.

[16] N. Padey and S. K. Paul, "A novel electronically tunable sinusoidal oscillator based on CCCII(-IR)," *Journal of Active & Passive Electronic Devices*, vol. 3, pp. 135–143, 2008.

[17] A. U. Keskin, K. Pal, and E. Hancioglu, "Resistorless first-order all-pass filter with electronic tuning," *AEU—International Journal of Electronics and Communications*, vol. 62, no. 4, pp. 304–306, 2008.