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IMPROVEMENT OF MOSFET CHARACTERISTICS

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By inclusion of a semi-dielectric layer, a novel MOSFET Structure, the T-MOSFET, and its integrated circuit version are presented. Both for the enhancement mode and the depletion mode, equivalent circuit models are developed. Also, the high frequency behaviour is explained by a model and the behaviour of a T-MOSFET under different conditions is given.

I. INTRODUCTION

A disadvantage of MOSFET (Metal Oxide Semiconductor Field Effect Transistor) over FET is its low output resistance. For FET, the range of O/P resistance is 0.1 – 1 MΩ whereas for MOSFET it is only 1–50 KΩ.

This low output resistance or drain resistance (r_d) makes the apparent load R_L' comparable to the actual load R_L.

The apparent load is given by

$$R_L' = r_d \parallel R_L = \frac{r_d R_L}{r_d + R_L} = \frac{R_L}{1 + \frac{R_L}{r_d}} \tag{1}$$

For $r_d \gg R_L$,

$R_L' \simeq R_L$

For $r_d \ll R_L$,

$R_L' \simeq r_d$,

which occurs with large load resistance in a MOSFET.

So the net voltage gain decreases. For $r_d \ll R_L$ it appears as $g_m R_L' \simeq g_m r_d \ll g_m R_L$.

To increase the drain resistance, r_{ds} (for a common source amplifier which is used in most cases), a thin highly resistive film is introduced between the source and drain of the MOSFET as shown in Fig. 1. As the dielectric and semi-dielectric has the appearance of letter T, this type of MOSFET may be named T-MOSFET. The integrated circuit version of the device is shown in Fig. 2.

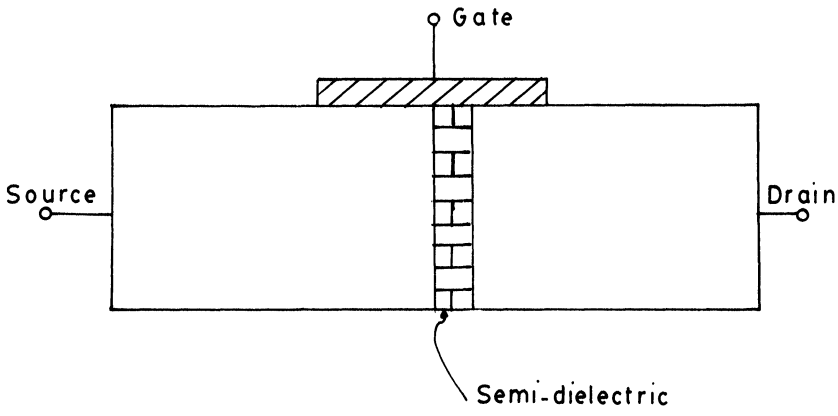

FIGURE 1 Shows the T-MOSFET device.

II. PHENOMENON OF IONIC CONDUCTION IN THE DIELECTRIC DUE TO ELECTRIC FIELD

When a strong electric field is applied to a dielectric, the ionic charges located in the dielectric are free to move, and a change of electrical characteristics will be observed as a function of time. Although the mobility of positive ions in the dielectric is quite small under large electric field, an appreciable drift velocity is observed at room temperature for electric fields of the order 10^5 to 10^6 V/cm.

In the T-MOSFET, an electric field due to drain-source voltage, V_{ds}, should be sufficiently large to produce an electric field in order to get a reasonable current through the dielectric.

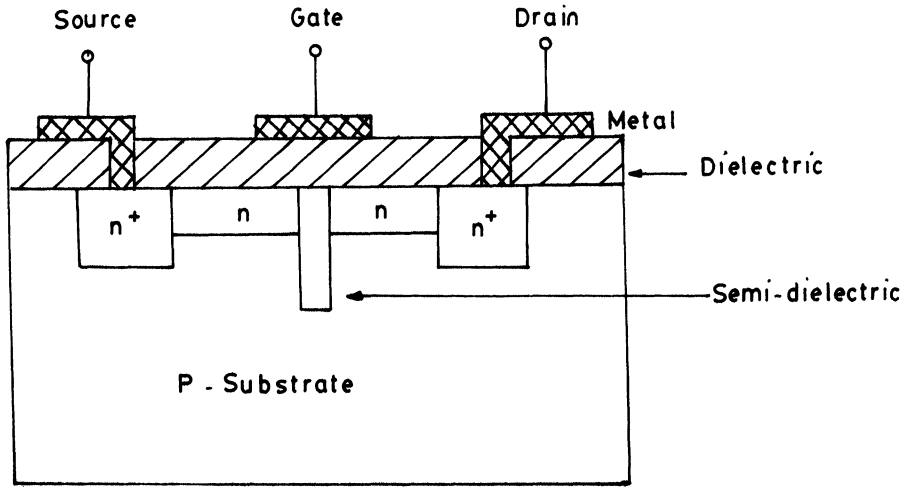

FIGURE 2 Shows the integrated circuit version of n type T-MOSFET.

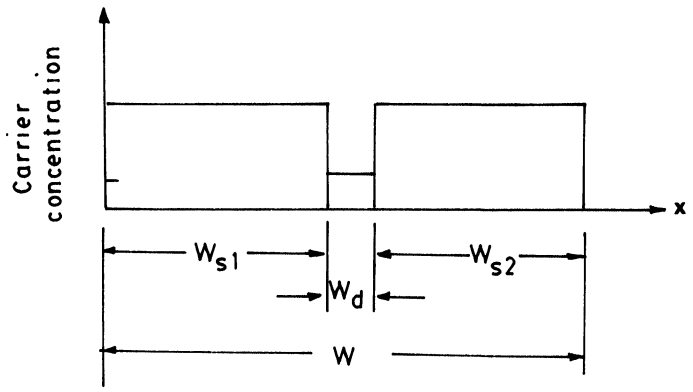

FIGURE 3 Shows the carrier concentration on the device with respect to distance from one side of the device.

Open Circuited T-MOSFET

When the crystal of an extrinsic semiconductor with the dielectric is formed between the source and the drain, no depletion region is formed. Fig. 3 shows the carrier concentration of an open circuited, drain-source region. Fig. 4 shows the electric field intensity. It is a straight line coinciding with the x axis, as there is no depletion region for open circuited T-MOSFET.

III. PHYSICAL DEVELOPMENT OF SMALL SIGNAL MODEL

For a semiconductor, conductivity is defined by the equation:

$$\sigma = (n\mu_n + p\mu_p)q$$

n = No. of electrons, μ_n = Mobility of Electrons, p = No. of holes/volume, μ_p = Mobility of holes, and q = Electronic charge,

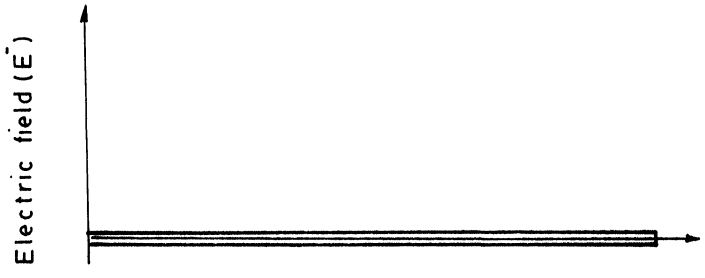

FIGURE 4 Shows the electric field intensity of the T-MOSFET.

For an n type semiconductor,

$$\text{as } n \gg p_i,\ \sigma \simeq nq\mu_n \tag{3}$$

The resistance in the drain-source region is equal to resistance due to semiconductors and the dielectric:

$$r_d = \frac{1}{nq\mu_n} \times \frac{(W_{s_1} + W_{s_2})}{A} + \rho_d \frac{W_d}{A} \tag{4}$$

where, A = the cross-sectional area of the T-MOSFET, W_{s_1}, W_{s_2} are semiconductor widths, ρ_d = resistivity of the semi-dielectric, and W_d = width of semi-dielectric. The drain current,

$$I_d = \frac{V_{ds}}{r_d} = \frac{V_{ds}}{\frac{1}{nq/\mu_n}(W_{s_1} + W_{s_2}) + \rho_d \frac{W_d}{A}} \tag{5}$$

where V_{ds} = drain-source voltage.

For the enhancement mode:

When a gate-source voltage, V_{gs}, is applied (for n type positive voltage), more electrons are attracted near the gate. Thus,

$$n = f_1(V_{gs}): \text{ a function of } V_{gs} \tag{6}$$

From equation (5),

$$I_d = \frac{V_{ds}}{\frac{K_1}{n} + K_2}$$

where K_1 and K_2 are constants for a particular device.

$$K_1 = \frac{W_{s_1} + W_{s_2}}{q\mu_n A};\ K_2 = \rho_d \frac{W_d}{A} \tag{8}$$

Thus,

$$I_d = \frac{V_{ds}}{\frac{K_1}{f_1(V_{gs}) + K_2}} = f_2(V_{gs}, V_{ds}) \tag{9}$$

For the depletion mode:

For depletion mode, the area that is under depletion A_d depends on V_{gs}.

So,

$$A_d = f_3(v_{gs}) \tag{10}$$

where $A_d = K_3A$ and $K_3 = a$. (11)

From equation (5),

$$I_d = \frac{V_{ds}}{K_4/A} \text{ where } K_4 = \text{constant}$$

$$= \frac{W_{s_1} + W_{s_2}}{nq\mu_n} + \rho_d W_d$$

$$= \frac{V_{ds}A}{K_4}$$

$$= \frac{V_{ds}A_d}{K_3K_4}$$

$$= \frac{V_{ds}f_3(V_{gs})}{K_3K_4} \tag{12}$$

Thus,

$$I_d = f_4(V_{gs}, V_{ds}) \tag{13}$$

For both the enhancement and depletion mode,

$$I_d = f(V_{gs}, V_{ds}) \tag{14}$$

Like the general type of MOSFET,

$$I_d = g_m V_{gs} + \frac{I}{r_d} V_{ds} \tag{15}$$

$$\text{where } g_m = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} \simeq \left.\frac{i_d}{V_{GS}}\right|_{V_{DS}} \tag{16}$$

$$\text{and } r_d = \left.\frac{\partial V_{DS}}{\partial i_D}\right|_{V_{GS}} \simeq \left.\frac{V_{ds}}{i_s}\right|_{V_{GS}} \tag{17}$$

The small signal model is given in Fig. 5. In this figure, the gate-source resistance, r_{gs}, and gate-drain resistance, r_{gd}, are taken as infinity. Taking this into account, the full, small signal model is illustrated in Fig. 6.

From equation (4),

$$r_d = \frac{W_{s_1} + W_{s_2}}{nq\mu_n A} + \rho_d \frac{W_d}{A}$$

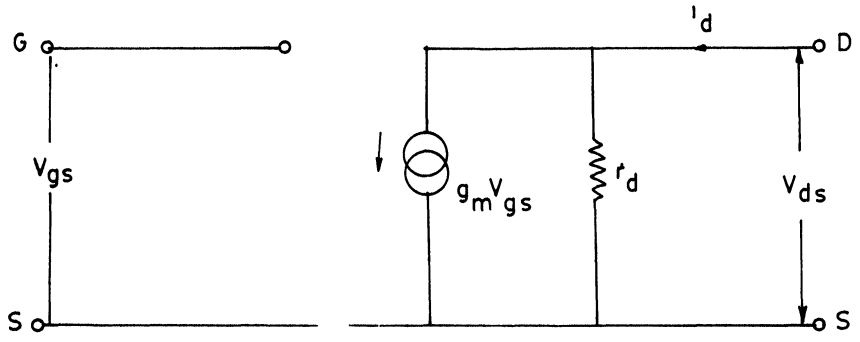

FIGURE 5 Shows the small signal model taking r_{gd} and r_{gs} infinity of T-MOSFET.

As the semi-dielectric resistivity is high,

$r_d \longrightarrow \infty$

and the approximate T-MOSFET model is given in Fig. 7.

IV. DEVELOPMENT OF THE HIGH FREQUENCY MODEL

The gate-drain capacitance, C_{gd} and the gate-source capacitance C_{gs} are present in the gate region of the T-MOSFET, as in the general type of MOSFET.

IV.1. The drain source capacitance calculation:

For the enhancement mode:

Due to enhancement, the conductances are increased for the semiconductor

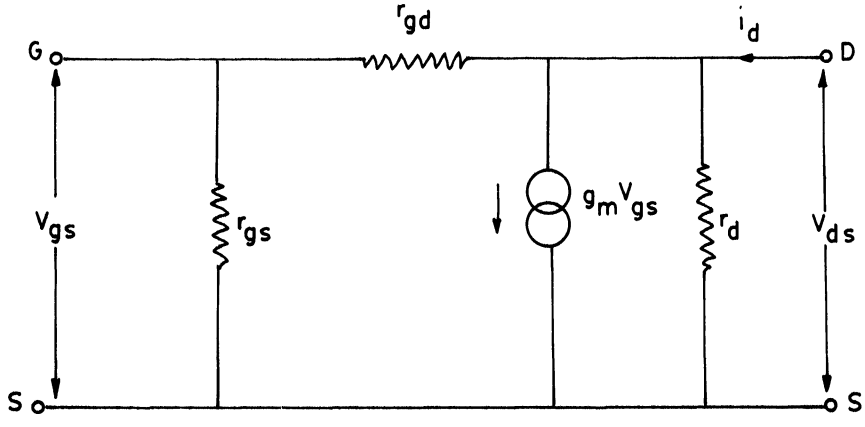

FIGURE 6 Shows the full small signal mode of T-MOSFET.

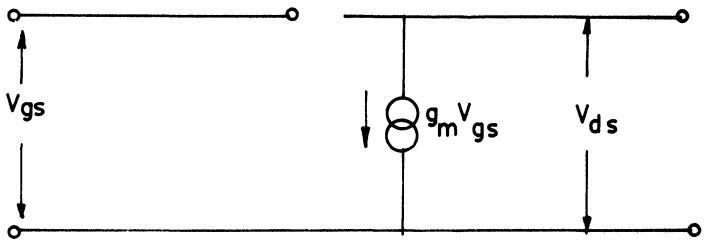

FIGURE 7 Shows the approximate small signal node of T-MOSFET.

portion, and the drain-source capacitance,

$$C_{ds} = Co = \frac{\varepsilon_d A_n}{td} \tag{18}$$

where Co = Capacitance due to dielectric and td = thickness of the semi-dielectric.

For the depletion mode:

Due to depletion, the immobile charge carriers region acts as a dielectric;

C_{ds} = series capacitance due to the depletion region of the extrinsic semiconductor and dielectric. It is given by the equation

$$\frac{1}{C_{ds}} = \frac{1}{C_o} + \frac{1}{C_{s_1}}\frac{1}{C_{s_2}} \equiv \frac{\varepsilon_d A}{td} + \frac{\varepsilon_s A_{d_1}}{X_{d_1}} + \frac{\varepsilon_s A_{d_2}}{X_{d_2}} \tag{19}$$

where A_{d_1} and A_{d_2} are the cross-sectional areas of depletion region, x_{d_1} and x_{d_2} are lengths of the depletion regions, and C_{s_1}, C_{s_2} are semiconductor capacitances in port 1 and 2 of the T-MOSFET. The high frequency model is shown in Fig. 8.

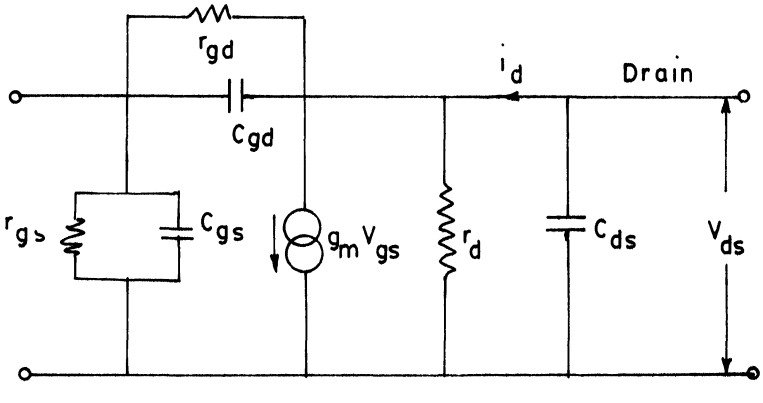

FIGURE 8 Shows the complete high frequency model of the T-MOSFET which is similar to general MOSFET.

V. T-MOSFET AT DIFFERENT CONDITIONS

V.1. If a dielectric is used instead of a semi-dielectric in the source-drain region:

From equation 4,

$$r_d = \frac{(W_{s_1} + W_{s_2})}{nq\mu_n} + \rho_d \frac{W_d}{A}$$

The resistivity of the dielectric ρ_d is very high, so

$$r_d \simeq \rho_d \frac{W_d}{A} \tag{20}$$

Thus,

$$I_d = \frac{V_{ds}}{Wd/A} \tag{21}$$

For the enhancement mode, from equation (6)

$$n = f_1(v_{gs}),$$

Thus, gate-source voltage has no control over the device. For the depletion mode.

From equation, (10) and (11),

$$A = \frac{1}{K_3} f_3(V_{gs}) \tag{22}$$

Thus,

$$I_d = \frac{V_{ds}}{K_3 \rho_d W_d} f_3(V_{gs}) \tag{23}$$

Thus, the gate-source voltage has control over the drain current; but as $\rho_d \rightarrow$ large, $I_d \rightarrow 0$ also, there is negligible control due to gate-source voltage in depletion mode, i.e. $g_m \rightarrow 0$.

V.2. If the semi-dielectric layer is thick:

As W_d is large, again from equation (4) we have

$$r_d \simeq \rho_d \frac{W_d}{A} \longrightarrow \infty$$

and, from previous section

$g_m \longrightarrow 0$

This device acts as an open circuit, with practically high resistances (see Fig. 9). For high frequencies, capacitances play a role and the equivalent circuit is shown in Fig. 10.

V.3. When gate-source voltage is zero:

This device will act like a two terminal device with passive components, as shown in Figures 9 and 10 for low and high frequency.

V.4. When V_{gs} is very large:

For enhancement mode:

The number of electrons, n increases, and thus the conductivity of the semiconductor, $\sigma \simeq nq\mu_n$, increases. Therefore, the resistance due to the semiconductor

$$= \frac{1}{nq\,\mu_n}\frac{2W_s}{A} \ll \text{resistance due to semi-dielectric}$$

and $r_d \approx$ resistance due to the dielectric:

$$r_d \simeq \rho_d \frac{W_d}{A}$$

$$\text{Again, } I_d = \frac{V_{ds}\,A}{\rho_d\,W_d} \tag{24}$$

$$\text{So, } \frac{\partial I_d}{\partial V_{gs}} = 0 \text{ for } V_{ds} = \text{constant}$$

$$\text{i.e. } g_m = 0$$

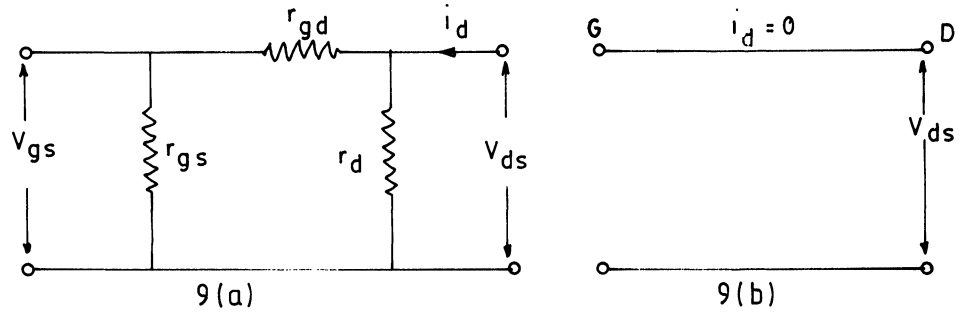

FIGURE 9 (a) and (b) shows the equivalent circuit of T-MOSFET when semidielectric layer is thick.

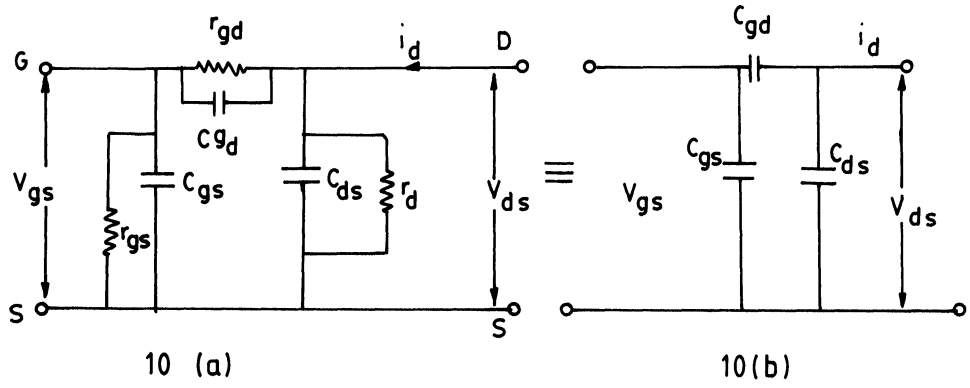

FIGURE 10 (a) and (b) shows the T-MOSFET at high frequency when semidielectric layer is thick.

For depletion mode:

In this mode, n decreases from equation (4).

$$r_d = \frac{(W_{s_1} + W_{s_2})}{nq\mu_n A} + \rho_d \frac{W_d}{A}$$

$$I_d = \frac{V_{ds}}{r_d} \longrightarrow 0$$

$$\frac{I_d}{V_{gs}}\bigg| V_{ds} \longrightarrow 0$$

and $g_m \to 0$

V.5. For Very high frequencies:

From the actual small signal model (Fig. 8)

$$\frac{1}{Z_{gd}} = \frac{1}{r_{gd}} + \frac{1}{1/jwC_{gd}} \tag{25}$$

$\approx j\omega C_{gd}$ as $r_{gd} \longrightarrow \infty$

$1/r_{gd} \longrightarrow 0$

As $w = 2 \overline{\wedge} f$

$$Z_{gd} = \frac{1}{j2 \overline{\wedge} f \cdot C_{gd}} \tag{26}$$

For very high frequencies,

$Z_{gd} \longrightarrow 0.$

Similarly, $Z_{gs} \rightarrow 0$ and $Z_{ds} \rightarrow 0$ and the net model is shown in Fig. 11, which is a short circuit.

VI. FABRICATION CONSIDERATIONS OF THE SEMIDIELECTRIC IN INTEGRATED CIRCUITS

As it is difficult to penetrate a semi-dielectric while fabricating it during the construction of the wafer, the material selected should be such that:

(i) It will have a high diffusion coefficient for diffusion processes so that it can be diffused from the upper side during growth of the integrated circuit in Fig. 2.
(ii) It should continue the crystal lattice with the n type semiconductor material used.

VII. CONDITIONS FOR THIS DEVICE TO ACT AS AN AMPLIFIER

From the results of the T-MOSFET at different conditions,

(i) In the drain-source region, a semi-dielectric is to be used instead of dielectric. A semi-dielectric may be formed by allowing a dielectric and a semiconductor.
(ii) The thickness of the semi-dielectric layer should be such that: a) The drain-source resistance is very high to act as an open circuit. b) The transconductance, g_m, should not be zero.
(iii) The dielectric in the gate to the rest of device is to be of such dimension that r_{gs} and r_{gd} are very high.
(iv) The gate source voltage is not to be increased appreciably.
(v) The device is to be operated in low frequencies only, as new methods for increasing the high frequency response cannot be used for further complications in the device itself.

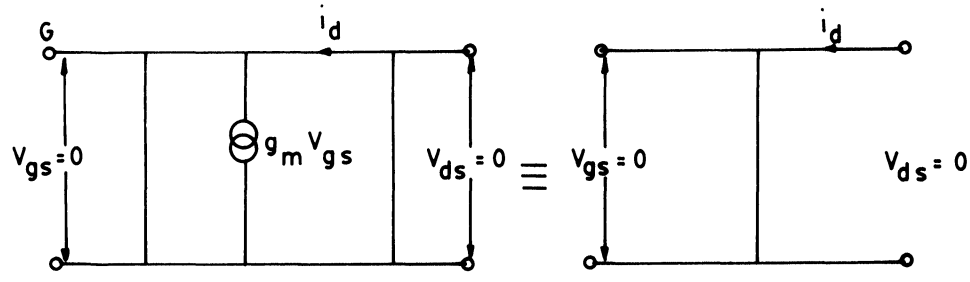

FIGURE 11 Shows the equivalent circuit of T-MOSFET at very high frequencies.

(vi) This device can be used only in integrated circuits although fabrication difficulties will arise to get a good transconductance, which is:

$$g_m = g_{m1} + g_{m2} + \cdots + g_{mn}$$

Calculations for transconductance are given in the Appendix.

VIII. SIMILARITIES AND DIFFERENCES WITH GENERAL MOSFET

A T-MOSFET is similar to a general type of MOSFET except (i) transconductance is very low for a T-MOSFET: hence the gate has less control over the device; (ii) the drain resistance is very high, hence, it works like an ideal transconductance amplifier; (iii) T-MOSFET is more difficult to fabricate than a MOSFET.

CONCLUSION

Overcoming the fabricational difficulties in integrated circuits, and forming the proper semi-dielectric, this device can be effectively used as MOSFET circuits.

APPENDIX

Calculation of total transconductance in integrated circuit of T-MOSFET:

As a T-MOSFET is an ideal transconductance amplifier, its input and output are connected in parallel in integrated circuits. Thus, all the inputs get same input voltage and all the output currents are added. Let the output currents in the amplifiers be I_{d_1}, I_{d_2}, . . . I_{d_n} with transconductances g_{m_1}, g_{m_2}, . . . g_{m_n}. So, the net current,

$$I_d = I_{d_1} + I_{d_2} + \cdots + I_{d_n}$$
$$= g_{m_1}V_{gs} + g_{m2}V_{gs} + \cdots g_{m_n}V_{gs} \qquad \text{(A1)}$$

As the same voltage, V_{gs}, is applied to all amplifiers,

$$= (g_{m_1} + g_{m_2} + \cdots + g_{m_n})V_{gs} - g_mV_{gs} \qquad \text{(A2)}$$

where g_m = total transconductance

$$= g_{m_1} + g_{m_2} + \cdots + g_{m_n} \qquad \text{(A3)}$$

REFERENCES

1. Richman, P. 'MOS Field Effect transistors and integrated circuits' PP. 150–155, Wiley Interscience 1973.
2. Millman J. and Halkias C.—"Integrated Electronics," McGraw Hill Co. (1971) PP. 321.
3. Ref. 2 PP. 28
4. Ref. 2 PP. 318, 319, 328.
5. Ref. 2, PP. 409.