Piezoresistance in silicon up to 3 GPa

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The room-temperature longitudinal piezoresistance of n-type and p-type silicon along selected crystal axes has been investigated under uniaxial compressive stresses up to 3 GPa. While the conductance of n-type silicon saturates at $\approx 50\%$ of its zero-stress value (G_0) in accordance with Herring and Vogt's model, in p-type material the conductance increases above its theoretically predicted limit of ≈ 4 times G_0 without any measurable saturation. The consequences of these observations for piezoresistive and strained-silicon technology are discussed.

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In many-valleyed semiconductors such as silicon, applied mechanical stress (X) modifies the band structure, principally changing the carrier mobility and hence the conductance, G [1–3]. In n-type silicon, uniaxial compressive stress along the [100] crystal directions lifts the 6-fold degeneracy of the ellipsoidal conduction bands, resulting in a charge transfer from the four bands perpendicular to X into the two which are parallel with X. This Herring and Vogt (HV) model [2] correctly describes piezoresistance data up to several hundred MPa [4]. In p-type silicon the band structure is more complex and band repopulation effects are not significant [5] so that a description of the piezoresistance using the HV model is not possible. Instead, mobility changes result from changes in the effective mass and scattering rates within the band, as well as a perturbation from the spin-orbit split off band [3, 6–8]. Using numerical $\mathbf{k}\cdot\mathbf{p}$ calculations, apparently satisfactory agreement with piezoresistance data is obtained up to several hundred MPa [6, 8]. In both the n-type and p-type cases, the models predict a saturation of the piezoresistance once the density-of-states averaged mobility ceases to change with X. The threshold stress for saturation depends on the doping density and varies from 500 MPa at low densities up to more than 1 GPa at high densities as observed in both n-type silicon and germanium [4, 9]. In p-type silicon high stress piezoresistance has not yet been reported, but saturation is predicted to occur at ≈ 2 GPa [6, 7] depending on the crystal direction. This is well above typically accessible externally applied stresses. From a practical viewpoint, saturation of the piezoresistance in silicon not only reveals something of the band structure, but will ultimately limit the increase in mobility afforded by strained-silicon technology [6].

Here we study, using a modified mechnical press, piezoresistance in n- and p-type silicon up to 3 GPa, well beyond the predicted onset of saturation. While the piezoresistance saturation predicted by the HV model holds in n-type silicon up to at least 2.4 GPa, in p-type silicon at even higher stresses, no such saturation is observed in stark contrast with theoretical predictions.

Experimentally, great care must be taken in order to reproducibly apply such large, mechanical stresses. To do so, a mechanical press was adapted to permit two-terminal conductance measurements perpendicularly across bulk semiconducting samples under compressive stress. The chuck assembly depicted in Fig. 1a ensures that the force is applied perpendicularly, by means of a flexible O-ring and a teflon sleeve that maintain parallelicity between the opposing steel chucks. Flat, mechanically polished tungsten plates are placed between the silicon sample and the steel chucks to avoid indentation of the steel, as had occurred during initial testing of the chuck assembly. Rigid, metal-covered non-conductors (ceramics and glass) were initially trialled in place of the tungsten but were found to reach their elastic limit and shatter at relatively low stress. The steel chucks themselves are electrically isolated from the press using glass plates to avoid short circuiting the sample with the press housing. A load cell measures the applied force, which is recorded together with the sample conductance.

The samples were prepared from commercially available double-side-polished n-type [(100), 5-10 Ω.cm, thickness 280 μm] and p-type [(110), $>$ 1 Ω.cm, thickness 400 μm] and [(111), 4-7 Ω.cm, thickness 275 μm] silicon wafers. Low doping densities were chosen to ensure that the measured two-terminal resistance is dominated by the sample itself rather than the leads. Ohmic contacts ($\rho_c = 10^{-6}\Omega\text{cm}^2$) are formed by a 100 nm deep thermally activated implant process on both faces of the

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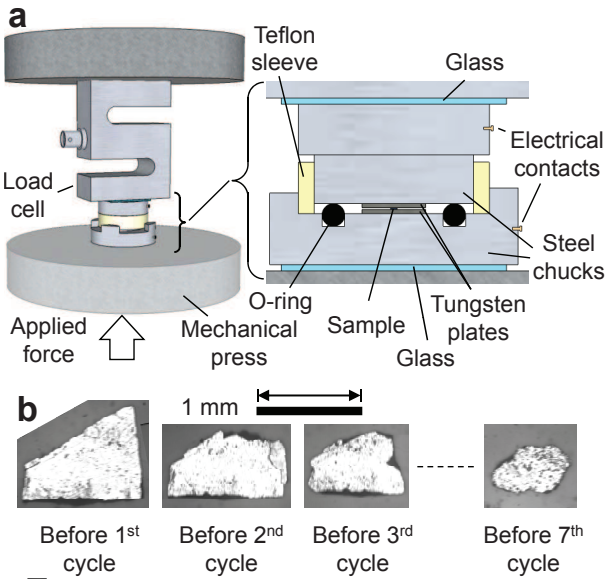

FIG. 1: (a) Cross-sectional view of the press, chuck assembly and sample, along the with the electrical connections for the conductance measurement. (b) A series of photographs of a p-type ⟨111⟩ sample before each application of stress, showing the cleaving of the sides.

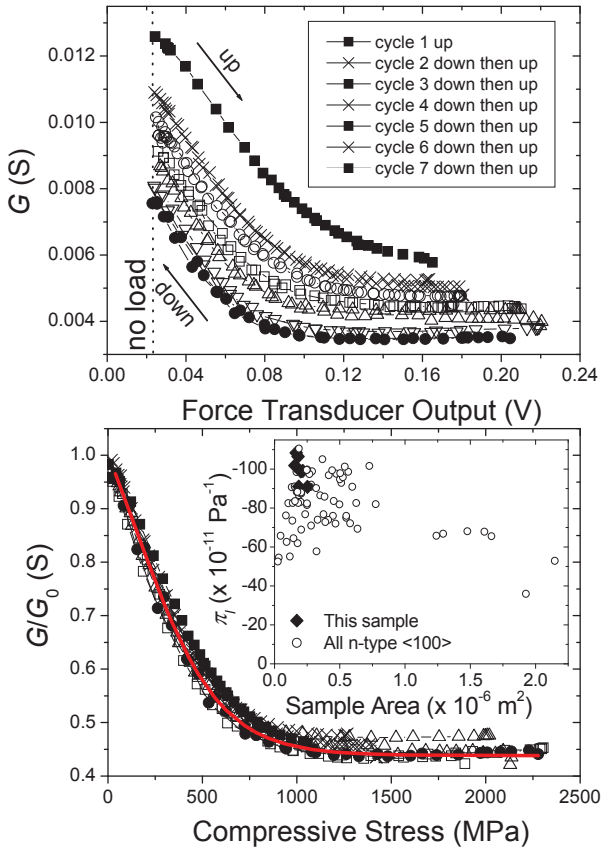

FIG. 2: (a) Raw data obtained along the ⟨100⟩ crystal direction in n-type silicon, showing discontinuous decreases in conductance due to in-situ cleaving of the sample edges. (b) Data corrected for changes in sample surface area showing clear saturation of the conductance. The fit of the HV model to these curves (solid line) yields $\Xi_u = 12.1$ eV and $\mu_\perp/\mu_\parallel = 2.9$.

wafer (doping density $\approx 10^{20}$ cm^{-3}) and finished with annealed aluminum contacts. After processing, the samples are cleaved with a diamond tipped scribe into pieces of size $\approx 5 \times 10^{-7}$m^2 (see Fig. 1b), so that a pressure of 1 GPa is obtained when about 500 N is applied.

Before measurement, the surface area of each sample is estimated from an image taken in an optical microscope (see Fig. 1b). In a first cycle, force is gradually applied to the sample while the conductance is measured. The stress is ramped up until a discontinuous decrease in the sample conductance is observed (point (a) in Fig. 2a). This jump, which is accompanied by an audible crack, corresponds to the edges of the sample cleaving off in the press, thereby reducing the effective surface area and decreasing the conductance (see Fig. 1b). The reduction in surface area also leads to an instantaneous increase in the applied stress, as the applied force remains unchanged. In the next cycle, the force is gradually ramped down to zero (without removing the sample) and then slowly ramped up until the sample cracks again. This process is repeated until the entire sample suddenly shatters into a fine powder, presumably because the instantaneous increase in stress resulting from one cracking event causes a cascade of additional cracking events. This typically occurs after about 5 cycles. The resulting raw data is a series of curves relating the sample conductance to the voltage output of the force transducer, as shown for a typical n-type sample in Fig. 2a. These curves cannot be directly compared because the cross-sectional area of the sample is different for each one, so that the relationship between the applied stress and the transducer output is not fixed. Furthermore, the conductance at zero stress, G_0, is reduced as the sample area is decreased. The surface area of the sample during each cycle is calculated by multiplying the initial surface area by the ratio of the present and initial zero-stress conductances. In this way, the measured force and calculated surface area can be used to determine the applied stress for each cycle. The conductance during each sweep is also normalized to G_0, allowing a direct comparison of the piezoresistance between samples of differing surface area. The corrected G/G_0 data corresponding to the raw data of Fig. 2a is plotted against the applied compressive stress in Fig. 2b. The corrected curves lie very close to one another and a saturation of the piezoresistance occurs at ≈ 1 GPa.

The data in Fig. 2b is fitted using Aubrey's adaptation [4] of the HV model [2] which has two free parameters; Ξ_u, the shear deformation potential and $\mu_\perp/\mu_\parallel$, the mobility ratio of the ellipsoidal valleys perpendicular and parallel to the applied stress. The solid curve in Fig. 2b corresponds to this fit and, over all the n-type samples tested, $\Xi_u = 12.6 \pm 3.5$ eV and $\mu_\perp/\mu_\parallel = 2.6 \pm 0.4$ is found. These values correspond well with those calculated and measured elsewhere [2, 4], thereby

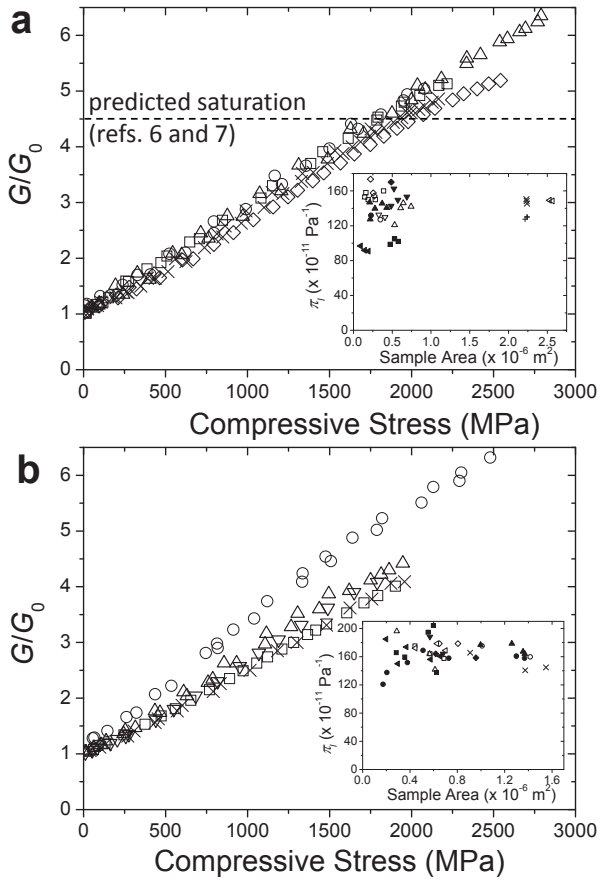

FIG. 3: Corrected data obtained along the (a) ⟨110⟩ and (b) ⟨111⟩ directions in p-type silicon. No saturation is observed in either case.

indicating that the conductance correction technique described above is reasonable. Furthermore, the slopes of the G/G_0 curves at low stress yield the longitudinal piezoresistance coefficient, π_l, from which it is found that $\pi_l = \partial G/\partial X \times 1/G_0 = -82 \pm 15 \times 10^{-11}$ Pa^{-1} slightly lower than with values obtained from the literature [10].

Figure 3a and b show the data in p-type silicon obtained along the ⟨110⟩ and ⟨111⟩ crystal directions respectively. Despite predictions to the contrary [6, 7] (see dotted horizontal in Fig. 3a), no saturation at high stress is observed in either case. At the highest stresses obtained (≈ 3 GPa), $G/G_0 \approx 6$, well above the predicted limit of about 4. At lower stresses, the slopes of these curves yield $\pi_l = 140 \pm 21 \times 10^{-11}$ Pa^{-1} for the ⟨110⟩ direction and $\pi_l = 159 \pm 37 \times 10^{-11}$ Pa^{-1} for the ⟨111⟩ direction, slightly higher than other values found in the literature [8, 10]. Since changes in conductance are primarily associated with changes in mobility and not the carrier concentration, the unexpected lack of saturation has potential consequences for strained-silicon technology, especially in the technologically relevant ⟨110⟩ p-type material. If the measured conductance change is attributed solely to a change in mobility, then the data presented in Fig. 3 indicate that much larger hole mobilities than previously envisaged could be possible at high process induced stresses.

It is also worth commenting on the possible consequences of the observations made here for piezoresistive strain gages. The sensitivity or gage factor ($\mathcal{G}$) of a strain gage is related to π_l through Young's modulus, E: $\mathcal{G} = E \times \pi_l$. High $\mathcal{G}$ strain gages are currently of interest for the detection of nano-scale strains in micro- and nano-electromechanical systems [11, 12]. In silicon, high $\mathcal{G}$ has been associated with interface and surface effects [11–13]. The data presented here indicate that working with a standard bulk silicon gage around some large, offset stress might yield non-negligible improvements in $\mathcal{G}$. Take for example the n-type data of Fig. 2b. If a quiescent compressive offset stress of $X_q = 500$ MPa is applied either via process induced stress or perhaps via a pressure difference across a membrane, then the effective G_0 is only about half the true value, $G_{0,eff} = G/2$. In this case, any stress variation about X_q may be detected by a gage with an effective gage factor $\mathcal{G}_{eff} = E \times \pi_{l,eff} = E/X \times \Delta G/G_{0,eff} = 2\mathcal{G}$. The same may be true for p-type strain gages where X_q is a large, tensile stress.

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