A Temperature-Dependent Model for Threshold Voltage and Potential Distribution of Fully Depleted SOI MOSFETs*

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Abstract: A temperature-dependent model for threshold voltage and potential distribution of fully depleted silicon-on-insulator metal-oxide-semiconductor field-effect transistors is developed. The two-dimensional potential distribution function in the silicon thin film based on an approximate parabolic function has been applied to solve the two-dimensional Poisson's equation with suitable boundary conditions. The minimum of the surface potential is used to deduce the threshold voltage model. The model reveals the variations of potential distribution and threshold voltage with temperature, taking into account short-channel effects. Furthermore, the model is verified by the SILVACO ATLAS simulation. The calculations and the simulation agree well.

Key words: fully depleted silicon-on-insulator MOSFETs; potential; threshold voltage
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1 Introduction

Fully depleted (FD) silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) have become very attractive due to their superior immunity to short-channel effects (SCEs)[1], ideal subthreshold characteristics[2], and kink effect immunity[3]. There have been many related reports on the modeling of this device. Hou *et al.*[4] reported a model for the two-dimensional (2D) potential distribution function of SOI-MOSFETs by using the Green function technique. Chiang *et al.*[5] solved the 2D Poisson's equation through the superposition technique. Despite the accuracy of these models, they involve infinite series, which increase the mathematical complexity. Young's model has proposed the parabolic function distribution of potential in the silicon thin film. Subsequently, many improved models for FDSOI MOSFTs have been developed based on Young's assumption[6]. However, none of these models includes temperature influence. SOI devices are ideal high-temperature electronic devices, which have extensive applications in the military, for automobiles, and in nuclear industries, where operating in a high temperature environment is common[2,7]. In this paper, a model of potential distribution and threshold voltage for FDSOI MOSFETs over a wide temperature range from 300 to 600K is proposed. The parabolic function distribution of potential in the silicon thin film is adopted. The potential distribution at the front oxide/silicon thin film layer interface has been obtained by solving 2D Poisson's equation with suitable boundary conditions. Moreover, the threshold voltage model can be derived according to the minimum of the front surface potential distribution, taking into account of short-channel effects. The results of this analytical model are found to be in good agreement with the simulation results obtained by SILVACO ATLAS simulation software.

2 Analytical model and simulation

2.1 Potential distribution analysis

The schematic structure of an FDSOI nMOSFET is shown in Fig. 1. The silicon thin film under the front gate oxide is completely depleted. The two-dimensional potential distribution $\psi(x, y, T)$ in this fully depleted silicon film can be obtained by solving the 2D Poisson's equation. Assuming that the impurity doping density is uniform in the channel region, the

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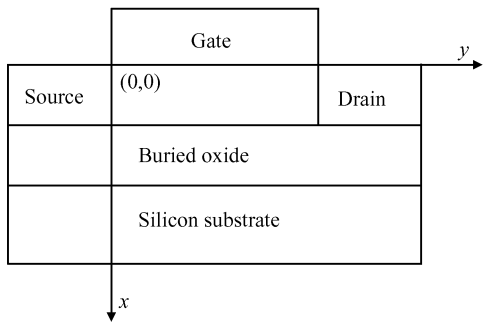

Fig. 1 Cross-sectional schematic of an SOI device

two-dimensional Poisson's equation, including the temperature factor, can be expressed as

$$\frac{\partial^2\psi(x,y,T)}{\partial x^2}+\frac{\partial^2\psi(x,y,T)}{\partial y^2}=\frac{qN_a}{\varepsilon_{Si}},\quad 0\leqslant x\leqslant T_{Si},0\leqslant y\leqslant L \tag{1}$$

where T is the absolute temperature, N_a is the doping concentration in silicon thin film, q is the electron charge, ε_{Si} is the permittivity of silicon thin film, T_{Si} is the thickness of the silicon thin film, and L is the channel length. The potential distribution in the silicon thin film can be approximated by a parabolic function:

$$\psi(x,y,T)=a_0(y,T)+a_1(y,T)x+a_2(y,T)x^2 \tag{2}$$

where $a_0(y,T)$, $a_1(y,T)$, and $a_2(y,T)$ are the functions of y and T, which may be determined by using the following boundary conditions:

$$\psi(x,y,T)\mid_{x=0}=\phi_f(y,T) \tag{3}$$

$$\psi(x,y,T)\mid_{x=T_{Si}}=\phi_b(y,T) \tag{4}$$

$$\frac{\partial\psi(x,y,T)}{\partial x}\mid_{x=0}=\frac{\varepsilon_{OX}}{\varepsilon_{Si}}\times\frac{\phi_f(y,T)-V_{gfeff}(T)}{T_{fox}} \tag{5}$$

$$\frac{\partial\psi(x,y,T)}{\partial x}\mid_{x=T_{Si}}=\frac{\varepsilon_{OX}}{\varepsilon_{Si}}\times\frac{\phi_{gbeff}(T)-\phi_b(y,T)}{T_{box}} \tag{6}$$

where $\phi_f(y,T)$ and $\phi_b(y,T)$ are the potential distribution function at the front interface between the gate oxide and the silicon thin film and the potential distribution function at the back interface between the silicon thin film and buried oxide layer, respectively. ε_{OX} is the permittivity of the gate oxide, and T_{fox} and T_{box} are the thickness of the front gate and back gate, respectively. $V_{gfeff}(T)$ and $V_{gbeff}(T)$ are the effective bias voltage of the front gate and back gate, respectively, which is given by

$$V_{gfeff}(T)=V_g-V_{FBf}(T) \tag{7}$$

$$V_{gbeff}(T)=V_{SUB}-V_{FBb}(T) \tag{8}$$

where V_g is the front gate bias voltage, and V_{SUB} is the bias voltage of substrate silicon. $V_{FBf}(T)$ and $V_{FBb}(T)$ are the flat-band voltages for the front gate oxide and the buried oxide, respectively, which can be given by

$$V_{FBf}(T)=\phi'_M-\left(\chi'+\frac{E_g(T)}{2q}+\phi_f(T)\right)+\eta \tag{9}$$

$$V_{FBb}(T)=\frac{kT}{q}\ln\left(\frac{N_{SUB}}{N_a}\right) \tag{10}$$

where ϕ'_M is the modified metal work function, χ' is the modified electron affinity, k is the Boltzmann constant, N_{SUB} is the doping concentration of the silicon substrate, and η is a fitting parameter. $E_g(T)$ is the band gap energy dependent on the temperature, which is given by[8]

$$E_g(T)=1.08+4.73\times10^{-4}\times\left(\frac{300^2}{300+636}-\frac{T^2}{T+636}\right) \tag{11}$$

$\phi_f(T)$ is the Fermi potential of the silicon thin film, which is given by

$$\phi_f(T)=\frac{kT}{q}\ln\left(\frac{N_a}{n_i(T)}\right) \tag{12}$$

where $n_i(T)$ is the intrinsic concentration depending on temperature, which is given by[8]

$$n_i(T)=\sqrt{N_C(T)N_V(T)}\exp\left[-\frac{E_g(T)}{2kT}\right] \tag{13}$$

where $N_C(T)$ and $N_V(T)$ are the effective density of states for electrons and holes, which are given by

$$N_C(T)=\left(\frac{T}{300}\right)^{1.5}\mathrm{NC300} \tag{14}$$

$$N_V(T)=\left(\frac{T}{300}\right)^{1.5}\mathrm{NV300} \tag{15}$$

where NC300 and NV300 are 2.8×10^{19} and 1.04×10^{19} cm^{-3}, respectively.

Using Eqs. (3) ~ (6) as boundary conditions in Eq. (2), $a_0(y,T)$, $a_1(y,T)$, and $a_2(y,T)$ can be determined by

$$a_0(y,T)=\phi_f(y,T) \tag{16}$$

$$a_1(y,T)=\frac{\varepsilon_{OX}}{\varepsilon_{Si}}\times\frac{\phi_f(y,T)-V_{gfeff}(T)}{T_{fox}} \tag{17}$$

$$a_2(y,T)=\frac{(C_{fox}/C_{Si}+C_{fox}/C_{box})V_{gfeff}(T)+V_{gbeff}(T)-(1+C_{fox}/C_{Si}+C_{fox}/C_{box})\phi_f(y,T)}{T_{Si}^2(1+2C_{Si}/C_{box})} \tag{18}$$

where C_{fox}, C_{Si}, and C_{box} represent the capacitances of the front gate oxide, the silicon thin film, and the buried oxide are given, respectively, by $\frac{\varepsilon_{OX}}{T_{fox}}$, $\frac{\varepsilon_{Si}}{T_{Si}}$, $\frac{\varepsilon_{OX}}{T_{box}}$.

Substituting Eqs. (16) and (17) into Eq. (2), the 2D potential distribution function $\psi(x,y,T)$ can be expressed in terms of the front surface potential distribution function $\phi_f(y,T)$. The front surface potential function may be derived by solving the 2D Poisson's equation:

$$\frac{d^2\phi_f(y,T)}{dy^2}-\alpha_f\phi_f(y,T)=\beta_f(T) \tag{19}$$

$$\alpha_f=\frac{2(1+C_{fox}/C_{Si}+C_{fox}/C_{box})}{T_{Si}^2(1+2C_{Si}/C_{box})\gamma} \tag{20}$$

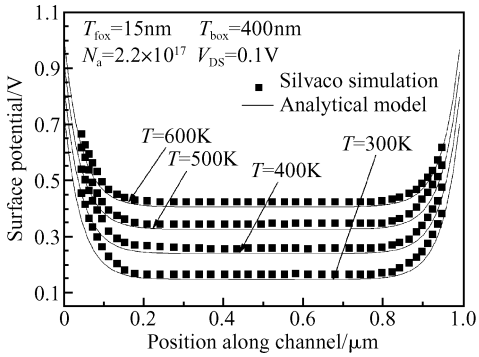

Fig. 2　Simulated and calculated front surface potential along channel at different temperatures (T_{Si} = 40nm)

$$\beta_f(T)=\left[\frac{qN_a}{\varepsilon_{Si}}-2\frac{(C_{fox}/C_{Si}+C_{fox}/C_{box})V_{gfeff}(T)+V_{gbeff}(T)}{T_{Si}^2(1+2C_{Si}/C_{box})}\right]/\gamma \tag{21}$$

Figure 2 illustrates the front surface potential distribution along the channel length at different temperatures at a small drain voltage bias (0.1V). The front surface potentials increase with temperature at the same position in the channel region because, when the temperature increases, the intrinsic concentration increases and the Fermi potential decreases[9].

Figure 3 shows the front surface potential distribution along the channel length with different gate lengths. The difference in potential minimum is clear. The devices with short channel length have higher potential minimums compared to devices with long channel length. We ascribe this difference to the short-channel effects in small devices[10]. As the drain bias voltage increases, the front surface potential minimum also increases owing to drain-induced barrier lowering (DIBL).

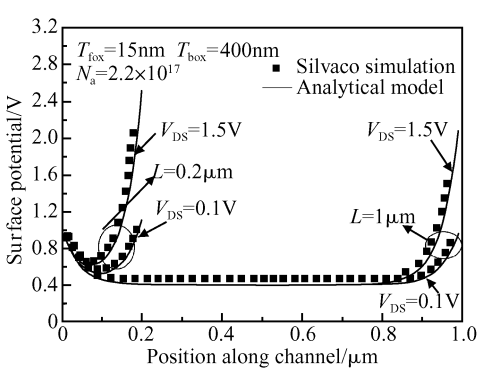

Fig. 3　Simulated and calculated front surface potential along channel with different channel lengths, at different drain bias voltages (T_{Si} = 40nm)

where γ is given by

$$\gamma = 1+\frac{2}{3}\left[T_{box}^2\left(\frac{C_{fox}+2C_{Si}}{C_{box}+2C_{Si}}\right)\right]/\left[T_{Si}^2(1+2C_{Si}/C_{box})\right] \tag{22}$$

Differential equation (19) can be solved by using the following boundary conditions:

$$\psi_f(0,T)=\phi_{bi}(T) \tag{23}$$

$$\psi_f(L,T)=V_{ds}+\phi_{bi}(T) \tag{24}$$

where $\phi_{bi}(T)$ is the built-in potential across the body-source junction, which is given by

$$\phi_{bi}(T)=\frac{kT}{q}\ln\left(\frac{N_aN_{ds}}{n_i^2(T)}\right) \tag{25}$$

where N_{ds} is the doping concentration of the drain and source. Therefore, the front surface potential $\psi_f(y,T)$ can be derived by

$$\psi_f(y,T)=-\frac{\beta_f(T)}{\alpha_f}+\frac{\phi_{bi}(T)+V_{ds}+\beta_f(T)/\alpha_f-[\phi_{bi}(T)+\beta_f(T)/\alpha_f]\exp(-\sqrt{\alpha_f}L)}{2\mathrm{sh}(\sqrt{\alpha_f}L)}\exp[-\sqrt{\alpha_f}(L-y)]+$$
$$\frac{2[\phi_{bi}(T)+\beta_f(T)/\alpha_f]\mathrm{sh}(\sqrt{\alpha_f}L)-\phi_{bi}(T)-V_{ds}-\beta_f(T)/\alpha_f+(\phi_{bi}(T)+\beta_f(T)/\alpha_f)\exp(-\sqrt{\alpha_f}L)}{2\mathrm{sh}(\sqrt{\alpha_f}L)} \tag{26}$$

2.2　Threshold voltage model

Threshold voltage is an important parameter in devices. Several models for threshold voltage have been proposed[11~13]. Veeraraghavan *et al*.[11] formulated a charge sharing model predicting an L^{-1} threshold voltage dependence. However, this model assumes a constant surface potential. Guo *et al*.[12] developed the threshold voltage model by solving the two-dimensional (2D) Poisson's equation with complicated mathematical operations. In this work, a simple analytical model for threshold voltage is derived based on the approach suggested by Young's model, which takes the temperature factor into account.

Threshold voltage is defined as the gate voltage where the minimum surface potential is $2\phi_f$. The minimum surface potential can be obtained by solving the equation $\frac{d\psi_f(y,T)}{dy}=0$. The minimum surface potential can be obtained by

$$\psi_{f,min}(T)=-\frac{\beta_f(T)}{\alpha_f}+2\left\{\left[\phi_{bi}(T)+\frac{\beta_f(T)}{\alpha_f}-\left(\phi_{bi}(T)+V_{ds}+\frac{\beta_f(T)}{\alpha_f}\right)\times\exp(-\sqrt{\alpha_f}L)\right]\times\right.$$
$$\left.\left[\phi_{bi}(T)+V_{ds}+\frac{\beta_f(T)}{\alpha_f}-\left(\phi_{bi}(T)+\frac{\beta_f(T)}{\alpha_f}\right)\times\exp(-\sqrt{\alpha_f}L)\right]\right\}^{\frac{1}{2}}\times\frac{\exp(-\sqrt{\alpha_f}L/2)}{1-\exp(-2\sqrt{\alpha_f}L)} \tag{27}$$

Therefore, the threshold voltage of devices with long channel length can be obtained, in which the second term of Eq. (27) is omitted:

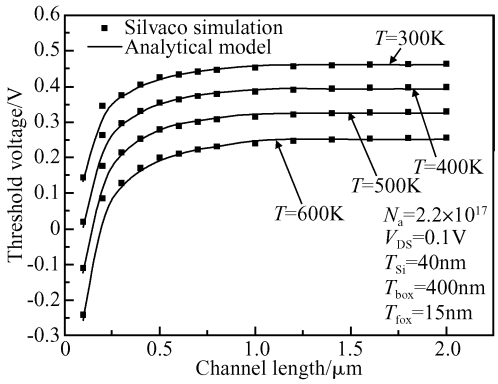

Fig. 4 Threshold voltage versus gate length at different temperatures with T_{Si} = 40nm

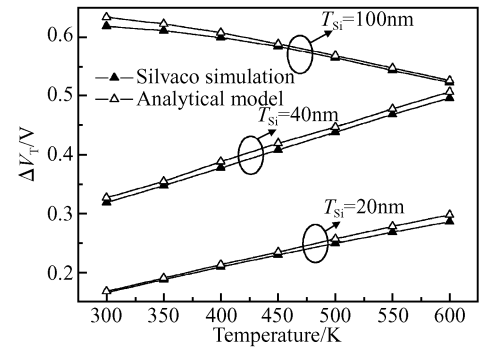

Fig. 6 Threshold voltage difference ΔV_T between the long channel (2μm) and the short channel (0.1μm) at different temperatures, for different thicknesses of silicon film

$$-\frac{\beta_f(T)}{\alpha_f} = 2\phi_f(T) \tag{29}$$

$$V_{thL}(T) = \frac{qN_a T_{Si}^2(1 + 2C_{Si}/C_b) - 2\varepsilon_{Si} V_{gbeff}(T) + 4\phi_f(T)\varepsilon_{Si}(1 + C_f/C_{Si} + C_f/C_b)}{2\varepsilon_{Si}(C_f/C_{Si} + C_f/C_b)} + V_{FBf}(T) \tag{30}$$

On the other hand, for the devices with short channel length, the second term of Eq. (27) cannot be omitted, so the following approximation is used: $\exp(-\sqrt{\alpha_f}L) \ll 1$. The threshold voltage can be solved by using a Newton iteration. Figures 4 and 5 display the threshold voltage versus channel length at different temperatures, with T_{Si} = 40nm and T_{Si} = 100nm, respectively. The threshold voltage decreases as the temperature increases because the minimum surface potential increases as the temperature increases, as illustrated in Fig. 2.

Figure 6 shows the threshold voltage difference ΔV_T between the long channel (2μm) and the short channel (0.1μm) at different temperatures. The short-channel effects are suppressed when the temperature increases if the silicon film is thick (T_{Si} = 100nm). Otherwise, when the silicon film is completely depleted (T_{Si} = 40nm and T_{Si} = 20nm), the short-channel effects become severe as the temperature increases. This is because the ratio of the charge controlled by the gate increases as the temperature increases for thick silicon film devices, while it is reduced for thin silicon film devices.

Figure 7 displays the simulated threshold voltage versus temperature for different thickness of the silicon film. The threshold voltage decreases as the temperature increases. The sensitivity of the threshold voltage to temperature decreases for thinner silicon film, due to the better coupling between the front gate and the back gate.

3 Conclusions

Analytical models for the front surface potential distribution and the threshold voltage for SOI MOSFETs have been presented in this paper. These models include the temperature influence. The analytical models are verified by the simulation software SILVACO TCAD. Good agreement is obtained between the model and the simulation. To the best of our knowledge, other related models proposed in the literature have not considered the temperature factor and involve too many fitting parameters. This model is predictive for the design of SOI devices at different temperatures.

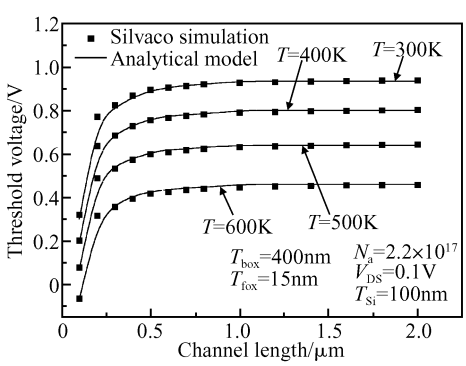

Fig. 5 Threshold voltage versus gate length at different temperatures with T_{Si} = 100nm

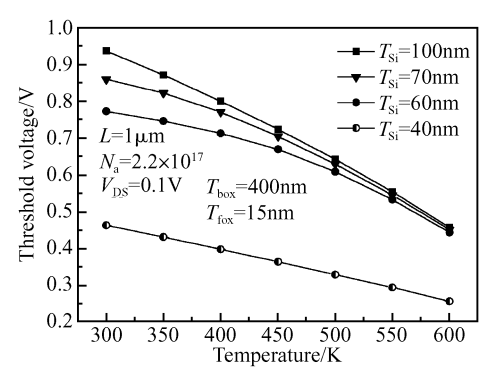

Fig. 7 Simulated variations of threshold voltage with temperature, for different thicknesses of silicon film

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全耗尽 SOI MOSFETs 阈值电压和电势分布的温度模型*

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摘要：提出了一个全耗尽 SOI MOSFETs 器件阈值电压和电势分布的温度模型.基于近似的抛物线电势分布模型,利用适当的边界条件对二维的泊松方程进行求解.同时利用阈值电压的定义得到了阈值电压的模型.该温度模型详细地研究了电势分布和阈值电压跟温度之间的变化关系,同时还近似地探讨了短沟道效应.为了进一步验证模型的正确性,利用 SILVACO ATAS 软件进行了相应的模拟.结果表明,模型计算与软件模拟吻合较好.

关键词：全耗尽 SOI MOSFETs；电势；阈值电压

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