A Heuristic Method for Statistical Digital Circuit Sizing

S. Boyd, S.-J. Kim, D. Patil, and M. Horowitz

Invited paper, *Proceedings of SPIE*, Vol. 6156, 2006

- stat_design_ML06.pdf
- stat_design_ML06_talk.pdf

In this paper we give a brief overview of a heuristic method for approximately solving a statistical digital circuit sizing problem, by reducing it to a related deterministic sizing problem that includes extra margins in each of the gate delays to account for the variation. Since the method is based on solving a deterministic sizing problem, it readily handles large-scale problems. Numerical experiments show that the resulting designs are often substantially better than one in which the variation in delay is ignored, and often quite close to the global optimum. Moreover, the designs seem to be good despite the simplicity of the statistical model (which ignores gate distribution shape, correlations, and so on). We illustrate the method on a 32-bit Ladner-Fischer adder, with a simple resistor-capacitor (RC) delay model, and a Pelgrom model of delay variation.