# A New Method for Design of Robust Digital Circuits

*D. Patil, S. Yun, S.-J. Kim, A. Cheung, M. Horowitz and S. Boyd*

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As technology continues to scale beyond 100nm, there is a significant increase in performance uncertainty of CMOS logic due to process and environmental variations. Traditional circuit optimization methods assuming deterministic gate delays produce a flat "wall" of equally critical paths, resulting in variation-sensitive designs. This paper describes a new method for sizing of digital circuits, with uncertain gate delays, to minimize their performance variation leading to a higher parametric yield. The method is based on adding margins on each gate delay to account for variations and using a new soft maximum function to combine path delays at converging nodes. Using analytic models to predict the means and standard deviations of gate delays as posynomial functions of the device sizes, we create a simple, computationally efficient heuristic for uncertainty-aware sizing of digital circuits via Geometric Programming. Monte-Carlo simulations on custom 32bit adders and ISCAS'85 benchmarks show that about 10% to 20% delay reduction over deterministic sizing methods can be achieved, without any additional cost in area.

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