ORACLE: Optimization with Recourse of Analog Circuits including Layout Extraction

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Long design cycles due to the inability to predict silicon realities is a well-known problem that plagues analog*RF integrated circuit product development. As this problem worsens for technologies below 100nm, the high cost of design and multiple manufacturing spins causes fewer products to have the volume required to support full custom implementation. Design reuse and analog synthesis make analog*RF design more affordable; however, the increasing process variability and lack of modeling accuracy remains extremely challenging for nanoscale analog*RF design. We propose an analog*RF circuit design methodology ORACLE, which is a combination of reuse and shared-use by formulating the synthesis problem as an optimization with recourse problem. Using a two-stage geometric programming with recourse approach, ORACLE solves for both the globally optimal shared and application-specific variables. Concurrently, we demonstrate ORACLE for novel metal-mask configurable designs, where a range of applications share common underlying structure and application-specific customization is performed using the metal-mask layers. We also include the silicon validation of the metal-mask configurable designs.