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研发、设计、测试

H.264标准中的CAVLC编码算法与FPGA实现

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摘要 H.264视频编码标准在基本档次和扩展档次采用CAVLC（基于上下文的自适应可变长编码）熵编码方法，但标准并未给出详细的CALVC编码句法。从CALVC的解码原理出发，详细分析了H.264视频编码标准中的CAVLC编码算法，提出了一种应用于H.264标准的快速低功耗CAVLC编码器结构，给出了各个功能模块的详细设计原理与FPGA实现方法，并对较复杂的几个模块进行了算法和结构上的优化，降低了实现的复杂度。FPGA实验验证表明，该方案编码系统时钟可达100 MHz，能满足对高速、实时应用的编码要求。

关键词 H.264标准 CAVLC 熵编码 编码器 FPGA

分类号

CAVLC and its FPGA realization for H.264

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Abstract

CAVLC is adopted as a entropy coding method in baseline and extended profile in H.264/AVC standard，but the detailed syntax on which is not provided.A profound analysis on the CAVLC coding algorithm in H.264 standard is performed based on the principle of CALVC decoding method.A high-speed and low power-consumption CAVLC coder for H.264 standard is presented according to the former analysis.And the detailed design and FPGA realization method on each sub-blocks are also concerned.Besides，some optimizations on algorithm and architecture of complex sub-blocks are also performed to reduce complexity of hardware realization.Finally，FPGA verification and realization indicates that the maximum coding system clock can up to 100 MHz，which can adequately meet the needs of some high-speed and real-time applications.

Key words H.264 CAVLC entropy coding encoder FPGA

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