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一种准循环低密度校验码部分并行编码结构设计

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A Partly parallel Coder Structure of Quasi-cyclic Low-density Parity check Codes

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摘要

为了满足在一个系统中使用多码率低密度奇偶校验（LDPC）码字的需求，设计了一个多码率准循环LDPC（QC LDPC）码编码器；按照功能，将编码器分成输入缓存单元（ISU）、生成矩阵存储单元（GMSU）、矩阵乘法运算单元（MMU）以及输出缓存单元（OSU）4个主要组成部分；通过使用多个小块存储器组合的方式设计ISU可以使无效存储空间降到最低；通过分析各种码率生成矩阵特点，将矩阵进行分割，从而将各种码率生成矩阵所需要的信息存储在若干个存储单元中；MMU用于完成信息位与矩阵的乘法与求和运算，运算单元的数目和GMSU的数目相等；OSU中包括两个存储器，采用乒乓操作，以提高编码速度。通过管脚的选择，此编码器支持0.4，0.6以及0.8码率3种编码模式。最后用Altera公司的现场可编程门阵列（FPGA）EP1S801508C7对编码器进行了实现。结果显示此编码器仅耗费5 339个逻辑单元，占FPGA总逻辑单元的7%，耗费439 296比特的存储器资源，占FPGA总存储器资源的6%。

关键词： 通信传输技术 硬件资源 低密度奇偶校验码 部分并行编码 多码率 现场可编程门阵列

Abstract：

To meet the requirement of using multi-rate low-density parity check (LDPC) codes in a communication system, a multi-rate quasi-cyclic LDPC(QC-LDPC) codes coder architecture is presented and implemented on an Altera field programmable gate array (FPGA) device. The coder is divided according to the function into four major parts: the input storage unit (ISU), the generator matrix storage unit (GMSU), the matrix multiplying unit (MMU), and the output storage unit (OSU). Combining several small memories instead of a single large one to keep the input information bits can minimize the null storage space of the ISU. Every vector of the multi-rate generator matrixes is reserved in the memories based on the generator matrix characteristic in the GMSU. The MMU performs matrix multiplication with the information bits, and is made up of a shift register, a register, some AND doors and some XOR doors in the circuit. The number of the MMU is equal to that of the GMSU. The OSU includes two memories, organized in ping pang format, so as to improve the coding rate. Using pin selection, three operating modes, i.e., the 0.4, 0.6, and 0.8 code modes, are supported. Synthesized using FPGA EP1S801508C7, the result indicates that the proposed multi-rate LDPC code coder-uses only 5339 logic elements,or 7% of the total, and 439296 memory bits, or 6% of the total.

Keywords： communication transmission technology hardware resources low-density parity-check codes partly-parallel coding multi-rate field programmable gate arrays

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