

研发、设计、测试

频率可调带宽可选的VLBI多相数字基带转换器

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摘要 VLBI数据采集终端是VLBI台站的重要设备,近年来随着数字硬件设备例如ADC、DSP、FPGA的快速发展,数字基带转换器代替模拟基带转换器成为现实。现有采用多相滤波器实现DBBC的方法不可避免存在盲区,且频率、带宽均不可调。提出一种通用的基于多相结构的宽带数字下变频方法,将多速率信号处理和并行处理方法应用在其中,成功实现了VLBI多个通道的单边带数字基带转换,且能实现中频中心频率可调、带宽可选。硬件测试结果表明VLBI数字基带转换器频率设置正确,带宽选择正确,且数字基带转换器带通特性好于模拟基带转换器。

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Polyphase based VLBI digital baseband converter with adjustable IF center frequency and bandwidth

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Abstract

The VLBI (Very Long Baseline Interferometry) data acquisition backend plays an important role in the VLBI station. Recently, based on advances in digital hardware like ADC (Analog-to-Digital Conversion), DSP (Digital Signal Processing), FPGA (Field Programmable Gate Arrays) and so on, it has become practical to sample and digitally process the intermediate frequency signal directly. DBBC (Digital Base-Band Converters) will replace ABBC (Analog Base Band Converters) in the VLBI data acquisition backend. A VLBI digital backend using poly-phase filter banks exits blind frequency zone inevitably. Moreover, the frequency and the band width are not adjustable in this method. This paper analyzes this limitation and presents a sequence of simple modifications to sampled data structures based on the analog prototype system to obtain the poly-phase structure in the VLBI data acquisition backend which can eliminate the blind frequency zone. The theoretical principles of digital SSB (Single Side Band) converters are discussed in detail. The approach adopts multi-rate signal processing for the designed filters in a digital SSB converter which is carried out by virtex-4 FPGA chips. The result of hardware VLBI experiments indicate that it can receive random IF band-pass in and bandwidth can be selected. Meanwhile, a conclusion is reached from the experiment that the VLBI DBBC has a better band pass performance than the ABBC.

Key words [Very Long Baseline Interferometry \(VLBI\)](#) [digital base-band converter](#) [Single Side Band \(SSB\)](#) [poly-phase filter banks](#) [blind frequency zone](#) [Field Programmable Gate Arrays \(FPGA\)](#)

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