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Low Cost Dynamic Architecture Adaptation Schemes for Drowsy Cache Management

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Abstract

Energy consumption and speed of execution have long been recognized as conflicting requirements for processor design. In this work, we have developed a low-cost dynamic architecture adaptation scheme to save leakage power in caches. This design uses voltage scaling to implement *drowsy caches*. The importance of a *dynamic* scheme for managing drowsy caches, arises from the fact that not only does cache behavior change from one application to the next, but also during different phases of execution within the same application. We discuss various implementations of our scheme that provide a tradeoff between granularity of control and design complexity.

We investigate a combination of policies where the cache lines can be turned off completely if they are not accessed, when in the drowsy mode. We also develop a simple dynamic cache-way shutdown mechanism, and propose a combination of our dynamic scheme for drowsy lines, with the cache-way shutdown scheme. Switching off cache ways has the potential of greater energy benefits but provides a very coarse grained control. Combining this with the fine grained scheme of drowsy cache lines allows us to exploit more possibilities for energy benefits without incurring a significant degradation in performance.

Keywords: Drowsy Cache, Architecture Adaptation, Low Power, Leakage Reduction, Dynamic Scheme

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