Enter search terms:
Search
in this series
Advanced Search

Notify me via email or RSS

Browse

Collections
Disciplines
Authors

Author Corner

Author FAQ

Links

University Libraries
UMass Amherst
Contact Us

Masters Theses 1896 - February 2014

Off-campus UMass Amherst users: To download campus access theses, please use the following link to log into our proxy server with your UMass Amherst user name and password.

Non-UMass Amherst users: Please talk to your librarian about requesting this thesis through interlibrary loan.

Theses that have an embargo placed on them will not be available to anyone until the embargo expires.

Online NBTI Wear-out Estimation

Download

SHARE

Mehernosh H. Dabhoiwala, *University of Massachusetts Amherst*

Follow

Document Type
Open Access

Degree Program
Electrical & Computer Engineering

Degree Type
Master of Science in Electrical and Computer Engineering (M.S.E.C.E.)

Year Degree Awarded
2013

Month Degree Awarded
September

Keywords
Online NBTI wear-out estimation

Abstract
CMOS feature size scaling has been a source of dramatic performance gains, but it has come at a cost of on-chip wear-out. Negative Bias Temperature Instability (NBTI) is one of the main on-chip wear-out problems which questions the reliability of a chip. To check the accuracy of Reaction-Diffusion (RD) model, this work first proposes to compare the NBTI wear-out data from the RD wear-out model and the reliability simulator - Ultrasim RelXpert, by monitoring the activity of the register file on a Leon3 processor. The simulator wear-out data obtained is considered to be the baseline data and is used to tune the RD model using a novel technique *time slicing*. It turns out that the tuned RD model NBTI degradation is on an average 80% accurate with respect to RelXpert simulator and its calculation is approximately 8 times faster than the simulator. We come up with a *waveform compression technique*, for the activity waveforms from the Leon3 register file, which consumes 131KB compared to 256MB required without compression, and also provides 91% accuracy in NBTI degradation, compared to the same obtained without compression. We also propose a NBTI ΔV_{th} *estimation/prediction technique*

to reduce the time consumption of the tuned RD model threshold voltage calculation by an order of with one day degradation being 93% within the same of the tuned RD model. This work further proposes to a novel NBTI Degradation Predictor (NDP), to predict the future NBTI degradation, in a DE2 FPGA for WCET benchmarks. Also we measure the ΔV_{th} variation across the 4 corners of the DE2 FPGA running a single Leon3, which varies from 0.08% to 0.11% of the base V_{th}.

Advisor(s) or Committee Chair

Burleson, Wayne P

This page is sponsored by the University Libraries.

© 2009 University of Massachusetts Amherst • Site Policies