

研发、设计、测试

混合Cache的低功耗设计方案

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摘要 在嵌入式处理器中, Cache的功耗所占的比重越来越大。为降低嵌入式系统中混合Cache的功耗, 引入一种基于程序段的重构算法——PPBRA, 并提出一种新的基于分类访问的可重构混合Cache结构, 该方案能够根据不同程序段对Cache容量的需求, 动态地分配混合Cache的指令路数和数据路数, 还能够对混合Cache进行分类访问, 过滤对不必要路的访问, 从而实现降低混合Cache的功耗的目的。Mibench仿真结果表明, 该方案在有效降低Cache功耗的同时, 还能提高Cache的综合性能。

关键词 [Cache](#) [可重构](#) [低功耗](#)

分类号

Low-power design of unified Cache

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Abstract

Caches compose larger and larger proportion in the power consumption of the embedded processors. In order to decrease the power of the unified cache, a Program Phase Based Reconfiguration Algorithm (PPBRA) and a new reconfigurable unified cache structure based on classification access are presented. The scheme can automatically, transparently, and dynamically manage the reconfigurable unified cache on a per-phase and it also can access the unified cache with classification, so it can avoid accessing the unnecessary ways, save the energy consumption. Mibench simulation results show that it decreases the average energy consumption and improves the comprehensive performance compared with the conventional unified cache.

Key words [Cache](#) [reconfigurable](#) [low-power](#)

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