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产品、研发、测试

一种高性能子字并行乘法器的设计与实现

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摘要 提出了一种支持子字并行的乘法器体系结构，并完成了其VLSI设计与实现。该乘法器在16 bit阵列子字并行结构的基础上，扩展了有符号与无符号之间的混合操作，采用多周期合并技术，实现了32 bit宽度的子字并行，并支持子字模式的乘累加，同时采用流水线设计技术，能够在单周期内完成4个8×8、2个16×16或1个32×16的有符号/无符号乘法操作。0.18 μm的标准单元库的实现表明该乘法器既能减小面积又能提高主频，是硬件消耗和运算性能的较好折衷，非常适用于多媒体微处理器的设计。

关键词 子字并行 乘法器 多媒体

分类号

Design and implementation of high performance subword parallel multiplier

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Abstract

This paper proposes a multiplier architecture capable of supporting subword parallelism，and has completed its VLSI design and implementation using 0.18 μm standard cell process.Based on the 16 bit array sub-word parallel architecture，this multiplier extends signed and unsigned hybrid operations，and uses multi-cycle combination technique to realize 32 bit sub-word parallel operations.In addition，it also supports sub-word multiply accumulate operations.With pipelined operation style，it can perform one 32×16，two 16×16，and four 8×8 bit signed/unsigned multiplications in single cycle respectively.The implementation results show that the proposed sub-word parallel multiplier can reduce the area and improve the frequency，which is a good compromise of hardware consumption and performance.It is well suitable for multimedia microprocessor design.

Key words subword parallelism multiplier multimedia

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