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Power Efficient Continuous-Time Delta-Sigma Modulator Architectures for Wideband Analog to Digital Conversion

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POWER EFFICIENT CONTINUOUS-TIME

DELTA-SIGMA MODULATOR ARCHITECTURES FOR WIDEBAND ANALOG

TO DIGITAL CONVERSION

A Dissertation Presented

by

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Electrical and Computer Engineering

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DEDICATION

To my beloved family for all their support and patience during my years of study

ABSTRACT

POWER EFFICIENT CONTINUOUS-TIME DELTA-SIGMA MODULATOR
ARCHITECTURES FOR WIDEBAND ANALOG-TO-DIGITAL CONVERSION

MAY 2012

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This work presents novel continuous-time delta-sigma modulator architectures

with low-power consumption and improved signal transfer functions which are suitable

for wideband A/D conversion in wireless applications, e.g., 3G and 4G receivers. The

research has explored two routes for improving the overall performance of continuous-

time delta-sigma modulator. The first part of this work proposes the use of the power

efficient Successive-Approximations (SAR) architecture, instead of the conventional

Flash ADC, as the internal quantizer of the $\Delta\Sigma$ modulator. The SAR intrinsic latency

has been addressed by means of a faster clock for the quantizer as well as full-period

delay compensation. The use of SAR quantizer allows for increasing the resolution

while reducing the total power consumption and complexity. A higher resolution

quantizer, made feasible by the SAR, would allow implementing more aggressive noise

shaping to facilitate wideband $\Delta\Sigma$ A/D conversion at lower over-sampling-rates. As

proof of concept, a first-order CT-$\Delta\Sigma$ modulator with a 5-bit SAR quantizer is designed and implemented in a 130 nm CMOS process which achieves 62 dB dynamic range over 1.92 MHz signal bandwidth meeting the requirements of the WCDMA standard. The prototype modulator draws 3.1 mW from a single 1.2 V supply and occupies 0.36 mm^2 of die area.

The second part of this research addresses the issue of out-of-band peaking in the signal-transfer-function (STF) of the widely used feedforward structure. The STF peaking is harmful to the performance of the modulator as it allows an interferer to saturate the quantizer and result in severe harmonic distortion and instability. As a remedy to this problem a general low-pass and peaking-free STF design methodology has been proposed which allows for implementing an all-pole filter in the input signal path for any given NTF. Based on the proposed method, the STF peaking of any feedforward modulator can be eliminated using extra feed-in paths to all the integrator inputs.

A major drawback of the conventional feedforward topology having low-pass STF is the large sensitivity of the STF to the coefficients. In particular, component mismatch, due to random errors in the relative values of individual resistors or capacitors, can significantly degrade the anti-aliasing of the CT modulator and give rise to the unwanted STF peaking. To solve this problem two new architectures, namely dual-feedback and dual-feed-in are proposed which allow us to synthesize a low-pass STF with a smaller number of coefficients than the feedforward structure. The dual-feedback structure which shows significantly lower sensitivity to coefficient mismatch is extensively analyzed and simulated. Also for proof of concept a third-order modulator

is implemented in a 130 nm CMOS process which achieves 76 dB dynamic-range over 5 MHz signal bandwidth meeting, for example, the requirements of a DVB-H receiver standard. In addition the modulator shows 77 dB anti-aliasing and less than 0.1 dB worst-case STF peaking. The measured power consumption of the modulator is 6 mW from a single 1.2 V and the die area is 0.56 mm^2.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Delta-Sigma ($\Delta\Sigma$) Modulators have received increasing popularity in recent years [1]. Traditionally, they are well-suited for high-resolution and low-speed applications like instrumentation where the conversion speed is traded off with the resolution. A common practice in the implementation of $\Delta\Sigma$ modulators is the use of a single-bit feedback digital-to- analog converter (DAC) which is inherently linear and allows for building precision $\Delta\Sigma$ analog-to-digital converters ($\Delta\Sigma$-ADC) with low cost. However, single-bit internal quantizers pose stability issues in third or higher-order $\Delta\Sigma$ modulators. To overcome this problem, a multi-bit internal quantizer can be used which has a well-defined gain and allows for implementing a stable $\Delta\Sigma$ loop filter. In recent years, with a shift toward higher speed applications, $\Delta\Sigma$ designs are predominantly multi-bit [2]. Also technology scaling has increased the maximum unity gain bandwidth of analog signal processing blocks, enabling the design of wide-band $\Delta\Sigma$ modulators with higher conversion rates which are needed for high speed communication applications.

The current trend toward System-On-Chip (SOC) design with ever increasing levels of integration necessitates reducing the power budget of the individual building blocks to reduce the overall power consumption . Low power consumption is particularly an important feature in portable applications which is needed for a long battery life. As a result of this trend, power-efficient data converter architectures such as

continuous-time delta-sigma (CT-ΔΣ) modulators have been attracting more attention in recent years.

From a design perspective, discrete-time (DT) ΔΣ modulators are often implemented using switched-capacitors (SC) technique. However in a SC-design the gain-bandwidth product (GBW) of the amplifiers need to be significantly higher than the sampling frequency for a linear settling. This requirement limits the highest conversion speed which can be achievable by a DT-modulator for a given power budget. Continuous-time (CT) design relaxes the amplifier speed requirements and has better potential for high speed and low-power applications. In addition, CT ΔΣ modulators offer inherent Anti-Aliasing (AA) which can be leveraged to simplify or eliminate the explicit filter preceding the ADC. Relaxing the ADC pre-filter requirements can provide power and cost reduction opportunities in other parts of the system as well.

1.2 Objectives

This research has explored two possible avenues towards designing power-efficient multi-bit CT-ΔΣ modulators. . First, we have considered the power reduction opportunities in multi-bit CT-ΔΣ modulators by enabling the use of power-efficient quantizer architectures. This objective is motivated by the observation that the multibit quantizer comprises a significant percentage of total power consumption in CT-ΔΣ modulators, particularly in comparison with DT structures. It is also noted that the traditionally-used flash architecture is not the most power-efficient quantizer. The common use of flash quantizer in CT-ΔΣ modulators is explained by desire to avoid the excess-loop-delay issue owing to its fast speed. In this work, we have proposed using

the successive-approximation (SAR) quantizer, as the most power efficient architecture [3], as multibit quantizer within a CT-$\Delta\Sigma$ modulator along with delay compensation to preserve the modulator stability. A potential issue associated with using a multibit quantizer in CT-$\Delta\Sigma$ modulators, is the excess-loop-delay contribution of the dynamic-element-matching (DEM) block used for the linearity enhancement of the feedback DAC. We have addressed this issue by taking advantage of the SAR quantizer's serial operation and introducing the partial-data-weighted-averaging (Partial-DWA) as an alternative DEM solution.

As a second path, we have considered the opportunities associated with improving the signal-transfer-function (STF) of a CT-$\Delta\Sigma$ modulator. Figure 1.1(a) shows a direct-conversion receiver architecture which is commonly used in low-cost receiver applications [4]. The analog base-band includes a variable-gain-amplifier (VGA) followed by a low-pass filter for anti-aliasing (AA) and blocker attenuation. The VGA is intended for amplifying the week base-band signal and eventually making it detectable by the ADC. In principle, the VGA can be eliminated by increasing the ADC dynamic range to detect the week desired signal without any amplification. On the other hand, a low-pass STF in the CT–$\Delta\Sigma$ modulator would make it possible to relax the analog base-band filtering requirements and thereby, provide power and area saving. In this work, we have proposed two novel modulator architectures which ensure a low-pass STF with no out-of-band peaking. As shown in Figure 1.1(b) the elimination of the VGA combined with the order reduction of the base- band filter can make such CT-$\Delta\Sigma$ modulators a viable solution for receiver applications.
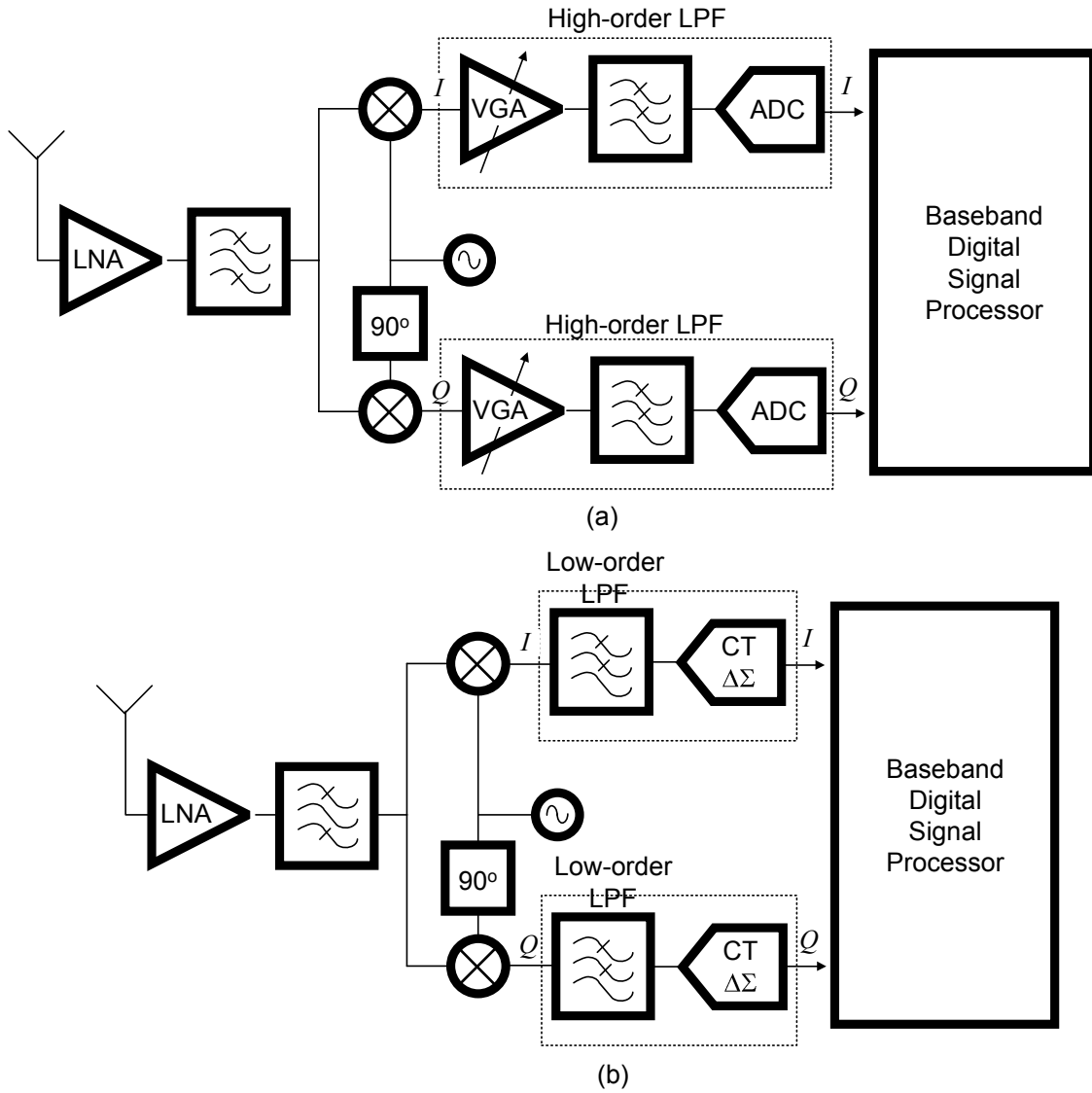
Figure 1.1: A direct conversion receiver. (a) conventional solution. (b) low-cost highly integrated solution based on CT-ΔΣ ADC with low-pass STF.

1.3 Outline of This Work

This work has been organized in seven chapters. The background theory of the ΔΣ modulators is provided in chapter-2 which concludes with an overview of the current state-of-the-art and the design trends. Behavioral modeling and simulation of various non-idealities has been discussed in chapter-3. Chapter-4 provides the details of

the proposed SAR-based architecture and presents the simulation and measurement results of a prototype modulator with a 5-bit SAR designed for a W-CDMA application. Chapter-5 presents two novel modulator topologies with robust STF and provides a methodology for designing low-pass STF with no out-of-band peaking. Capter-6 describes design, simulation and measurement results of a prototype third-order dual-feedback CT-$\Delta\Sigma$ modulator intended for a 5 MHz DVB-H application. Chapter-7 provides a summary of this work and lists the major contributions and also discusses some ideas for future research.

CHAPTER 2

DELTA-SIGMA MODULATION FUNDAMENTALS

Analog to Digital converters are key building blocks in most electronic systems. They serve as an interface between the real world analog signals and the digital signal processing heart of the system. The speed, resolution and power consumption needs of each application can suggest a specific ADC architecture to achieve the best trade-off between power and performance. $\Delta\Sigma$ A/D converters are the preferred architecture for high-resolution and low-speed applications [5]. $\Delta\Sigma$ modulators belong to the family of oversampling data converters that process many samples of the input signal to produce an output sample at the Nyquist rate. Moreover, $\Delta\Sigma$ modulators are closed-loop systems which are tolerant of some analog imperfections. The relatively low sensitivity to non-idealities such as offset and mismatch allows for using simple and low cost analog building blocks. In addition, signal processing in a $\Delta\Sigma$ ADC is split between analog and digital sub-sections, where analog filtering is employed for rejecting the quantization errors from the signal band, and digital filtering is used for increasing the effective resolution by eliminating the out of band quantization noise [6]. This chapter seeks to cover the fundamentals of $\Delta\Sigma$ modulators and the principle behind continuous-time (CT) to discrete-time (DT) transformation techniques often utilized in the design of CT-$\Delta\Sigma$ modulators.
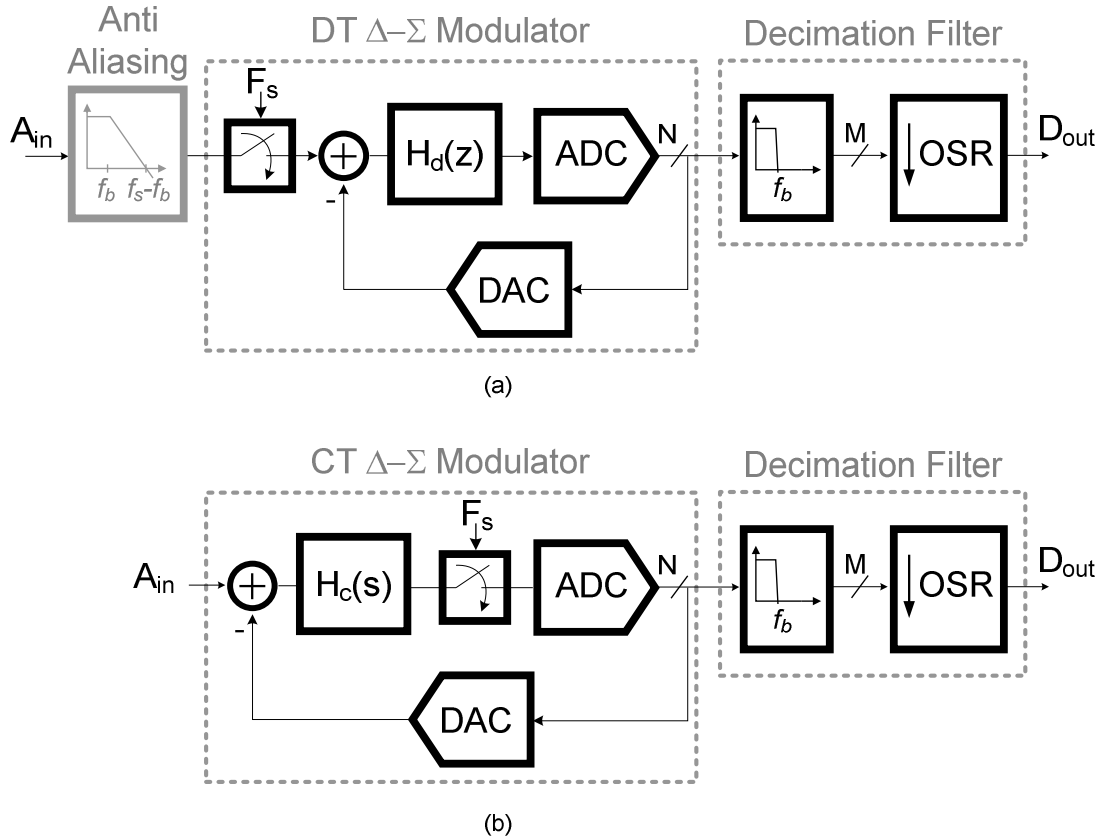
Figure 2.1: $\Delta-\Sigma$ modulation ADC (a) Discrete-Time. (b) Continuous-Time.

2.1 Oversampling and Anti-Aliasing

The block diagrams of typical $\Delta\Sigma$ A/D converters using discrete-time and continuous-time signal processing are shown in Figure 2.1 (a) and (b), respectively. Both structures involve sampling which is a fundamental operation in all A/D converters. The spectrum of the sampled signal will include the images of the original spectrum around the fundamental and all harmonics of the sampling frequency. Using Nyquist criterion the sampling rate, F_s needs to be at least twice the signal bandwidth f_b to enable reconstruction of the signal from its samples. A/D converters that use the minimum sampling rate of $F_s=2f_b$ are called Nyquist rate ADCs.

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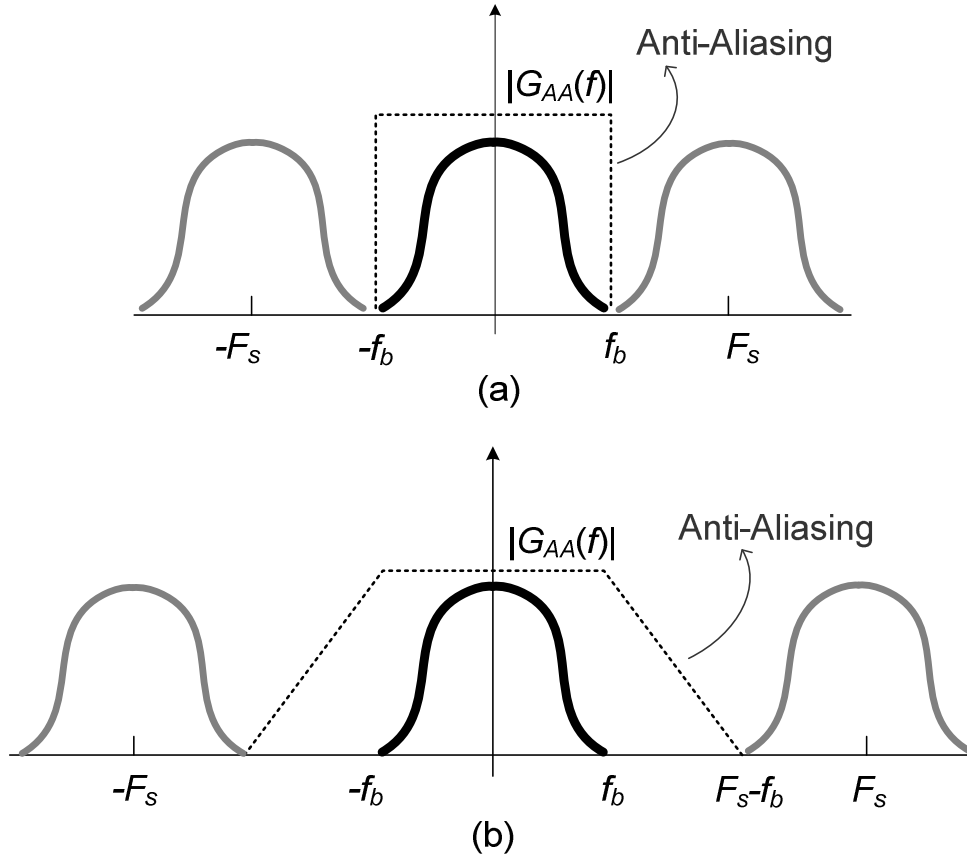
Figure 2.2: Spectrum of the sampled signal and AA-Filter requirements in (a) Nyquist rate ADCs (b) Oversampling ADCs

In contrast, $\Delta\Sigma$ modulators sample the analog signal at a rate much faster than $2f_b$ and are categorized as over-sampling data converters. The ratio of the actual sampling frequency to the Nyquist rate is called oversampling ratio (OSR) which is a key parameter in the design of $\Delta\Sigma$ modulators

$$OSR = \frac{F_s}{2f_b}.$$ (2.1)

To prevent Spectral Aliasing, the bandwidth of the signal to be sampled needs to be limited prior to sampling. The order and complexity of the anti-aliasing filter is related to the slope of its transition band. For example, when sampling frequency is near the Nyquist rate the slope of the transition band becomes very steep as shown in Figure

2.2(a), and consequently a very high-order filter will be required. However the use of oversampling, as shown in Figure 2.2(b), allows for widening the transition band of the anti-aliasing (AA) filter which significantly relaxes the filtering requirements. In addition to the oversampling ratio, the filter order in a wireless application depends on the targeted dynamic range and the amplitude of the interferers at the alias band. Assuming a Butterworth low-pass characteristic with 20 dB/Dec role-off the filter order, N_{AA} becomes (see Appendix A)

$$N_{AA} = \left\lceil \frac{SFDR + P_{ALS} - P_{SIG}}{20 \ \log_{10}(2OSR - 1)} \right\rceil \tag{2.2}$$

In the above $\lceil \cdot \rceil$ indicates rounding the result to the nearest integer towards plus infinity, *OSR* is the oversampling ratio, *SFDR* is the targeted spurious free dynamic range in dB, P_{SIG} and P_{ALS} the dBFS amplitude of respectively the input tone and the alias tone in the frequency band $F_s\text{-}f_b < f_{ALS} < F_s + f_b$. For example, when OSR =16, *SFDR = 90 dB* , P_{SIG}= *-6* dB and P_{ALS} = *0* dB at $f_{ALS} = F_s - f_b$, a 4th-order anti-aliasing filter will be needed. Also (2.2) clearly predicts that when *OSR=1* (i.e. no oversampling) the order of the AA filter is infinity.

As shown in Figure 2.1(a), anti-aliasing in DT $\Delta\Sigma$-ADCs is performed by an explicit A/D pre-filter. However in CT $\Delta\Sigma$ ADCs, the input signal gets band limited by the modulator filter $H_c(s)$ prior to sampling, as shown in Figure 2.1(b). The implicit anti-aliasing of CT $\Delta\Sigma$ modulators is a result of moving the sample-and-hold from the modulator input to the quantizer front-end. This is fundamentally impossible in DT $\Delta\Sigma$ modulators since a DT filter only processes sampled signals.
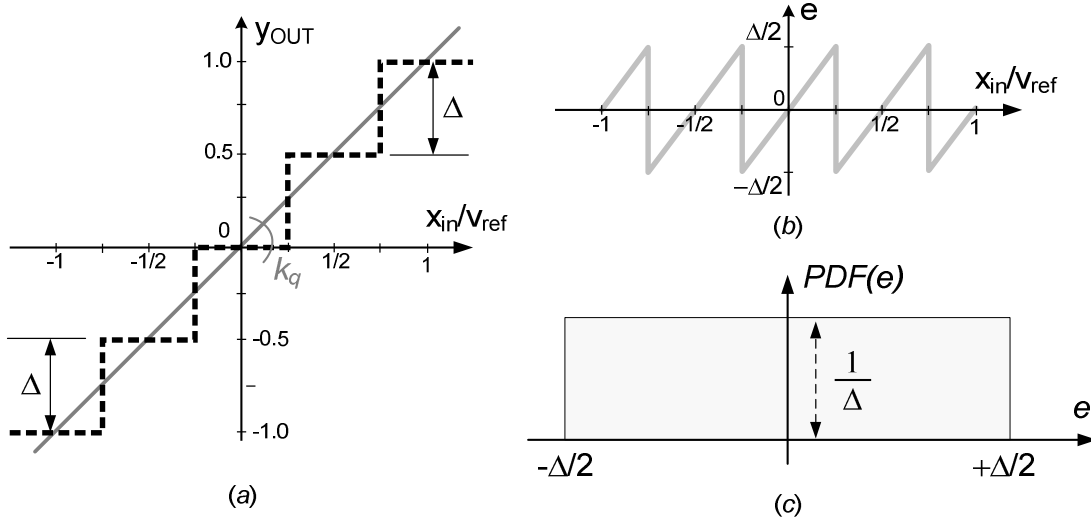
Figure 2.3: (a) Transfer characteristics of a multi-level uniform quantizer, (b) quantization error profile (c) Uniform PDF of the quantization error.

2.2 Quantization

Quantization of the amplitude is a nonlinear operation which is inherent to all A/D converters. Figure 2.3(a) shows the ideal transfer characteristics of a multi-level uniform quantizer. The error introduced during the quantization process, as shown in Figure 2.3(b), is the difference between the actual input and the quantized output and is called quantization noise. Assuming a bounded input within the $\pm V_{ref}$ range, the quantization error will be distributed uniformly over $[-\Delta/2, +\Delta/2]$ where Δ is the quantization step size defined as

$$\Delta = \frac{VFS}{N_{level}} = \frac{2V_{ref}}{2^N - 1} \tag{2.3}$$

In the above equation, *VFS* is the peak-to-peak full-scale range of the quantizer, V_{ref} is the reference voltage which is half of the full-scale, N_{level} is the number of quantization levels related to the quantizer resolution in bits (*N*) as $N_{level} = 2^N\text{-}1$.
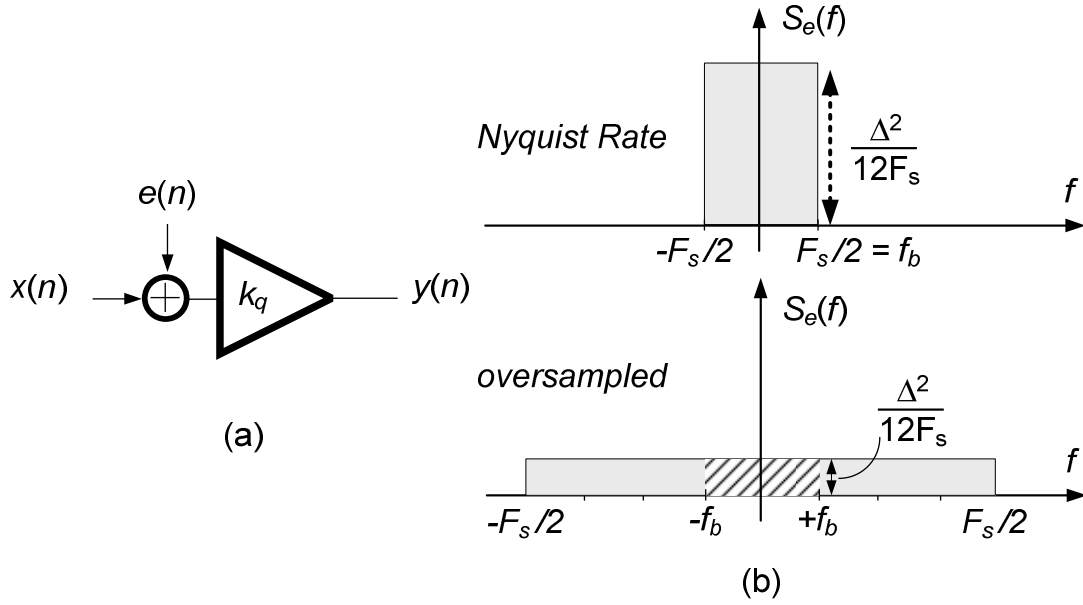
Figure 2.4: (a) Linear gain additive noise model of the quantizer. (b) Noise power spectral density in Nyquist rate and oversampled quantizers.

The total power of the quantization noise is calculated from the uniform PDF shown in Figure 2.3(c) as

$$P_e = \sigma_e^2 = \int_{-\infty}^{\infty} e^2 PDF(e)de = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.4}$$

The linearized additive noise model of the quantizer shown in Figure 2.4(a) is a useful tool for small signal analysis of $\Delta\Sigma$ modulator loops. In this model the quantizer gain k_q is defined as the slope of the line crossing the origin, and connecting the midpoints of the quantization steps as shown in Figure 2.3(a). A white noise approximation [7] can often be used for modeling the quantization noise where the errors are assumed to be independent of the input signal. With the white noise approximation, quantization noise assumes a flat power spectral density $S_e(f)$ where the

total power , as shown in Figure 2.4(b), is uniformly distributed over [–Fs/2 , Fs/2]. With the use of oversampling (i.e. $f_b \ll F_s/2$) the in-band quantization noise power P_q becomes only a fraction of the total noise

$$P_q = \int_{-f_b}^{+f_b} S_e(f)df = \int_{-f_b}^{+f_b} \frac{\Delta^2}{12F_s} df = \frac{1}{OSR} \cdot \frac{\Delta^2}{12} \qquad (2.5)$$

Using (2.5) and noting that the signal peak is approximately $V_{pk} \approx 2^{N-1}\Delta$ the signal-to-quantization-noise ratio (SQNR) of an N-bit quantizer with oversampling ratio OSR is calculated in dB as

$$SQNR_{dB} = 10\log_{10}\left(\frac{P_{sig}}{P_q}\right) = 6.02\left[N + \frac{\log_2(OSR)}{2}\right] + 1.76 \qquad (2.6)$$

The above equation shows that each doubling of the OSR increases the effective resolution by half bit.

2.3 Noise Shaping

The negative feedback of a ΔΣ modulator loop forces the coarse quantizer output to closely track the input signal in the band of interest. In other words, the in-band quantization noise is attenuated by the modulator loop filter and consequently the effective resolution is increased. This interesting property of ΔΣ modulators is called noise shaping. Using the combination of oversampling and noise-shaping, as shown in Figure 2.5 (a) and (b) respectively, a ΔΣ modulator achieves a dramatic increase of in-band SQNR. Further processing of the modulator output by a digital low-pass filter eliminates the out-of-band quantization noise before down-sampling the output to the Nyquist rate.
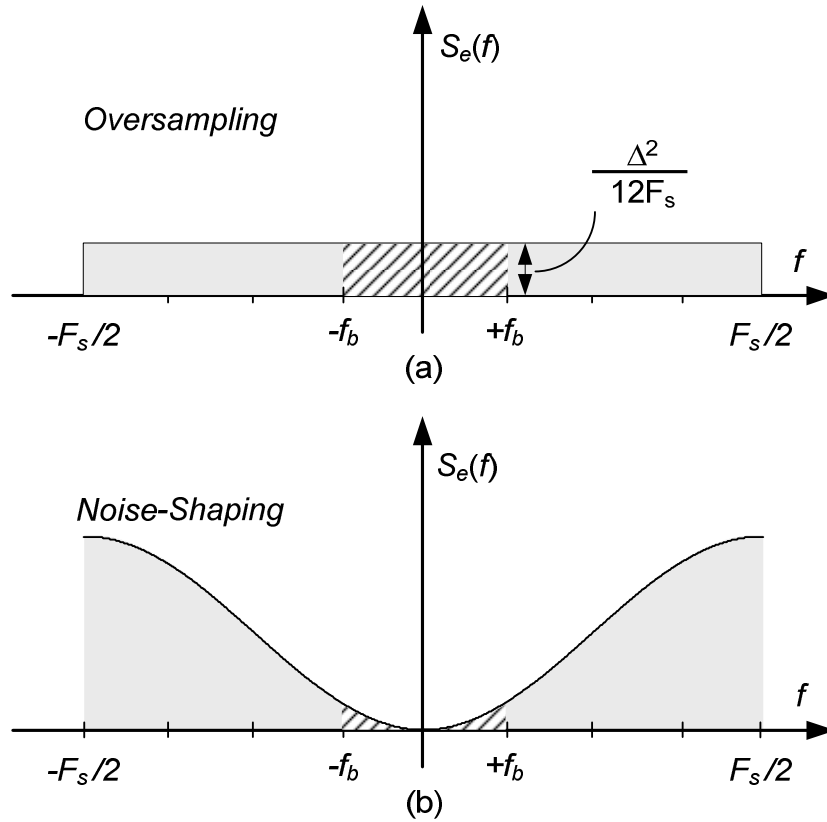
Figure 2.5: ΔΣ modulation principles (a) oversampling (b) noise shaping.

In order to gain a quantitative understanding of noise-shaping, we will refer to the linearized model of the DT ΔΣ modulator shown in Figure 2.6 where the coarse ADC is replaced by its additive noise model with gain k_q. Also to account for any prefiltering of the input signal a separate transfer function $G_d(z)$ is used for the input path. The noise transfer function of this modulator can be expressed as

$$NTF(z) = \frac{Y(z)}{Q(z)} = \frac{k_q}{1 + k_q H_d(z)}$$ (2.7)

Using (2.7) the required modulator loop filter $H_d(z)$ to realize a known $NTF(z)$ should be

$$H_d(z) = \frac{1}{NTF(z)} - \frac{1}{kq}$$ (2.8)

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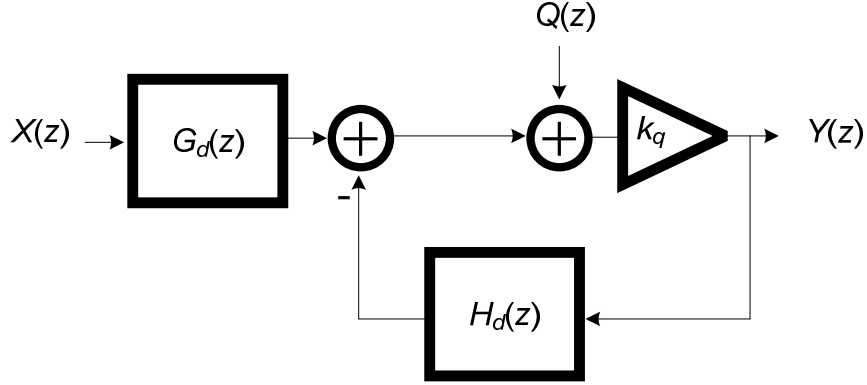
Figure 2.6: Linearized model of a DT ΔΣ modulator.

Similarly the signal transfer function from *X(z)* to *Y(z)* is expressed as

$$STF(z) = \frac{Y(z)}{X(z)} = G_d(z) \cdot NTF(z) \tag{2.9}$$

Note that in most ΔΣ modulator topologies $G_d(z) = H_d(z)$, but in general $G_d(z)$ and $H_d(z)$ can be different. Assuming a unity gain quantizer with $k_q = 1$ and a DT integrator as the modulator loop filter (i.e. $H_d(z) = z^{-1}/(1-z^{-1})$) a first-order noise shaping is obtained as

$$NTF(z)|_{\text{first-order}} = 1 - z^{-1} \tag{2.10}$$

which is the classical DT differentiator with a single zero at DC. Also using (2.8) and assuming $G_d(z) = H_d(z)$, the signal transfer function of the first-order modulator is

$$STF(z)|_{\text{first-order}} = z^{-1} \tag{2.11}$$

which is a pure delay that does not alter the spectrum of the sampled signal.

The NTF in (2.10) provides a first-order high-pass filtering of the quantization noise by a single zero at DC. To improve the SQNR, higher order NTFs can be realized by placing more transfer function zeros at signal band.
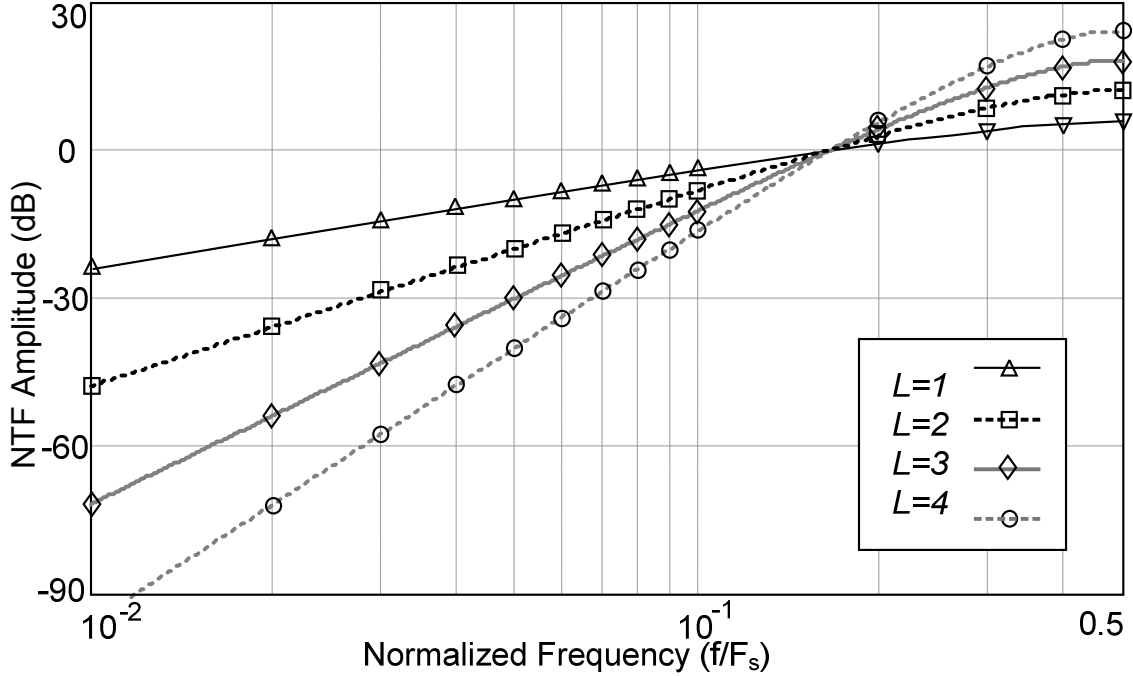
Figure 2.7: Classical L-th order Noise Transfer Functions (all zeros at DC).

A classical higher-order NTF with all zeros at DC is expressed as

$$NTF(z) = (1 - z^{-1})^L \tag{2.12}$$

In the above, L is the order of noise shaping, which in general is equal to the number of NTF zeros. Figure 2.7 shows the NTF magnitude response for modulator orders $L=1$ to $L=4$. It is noted that by increasing the order of noise shaping the NTF out-of-band gain is also increased. A large NTF out-of-band gain usually limits the dynamic range of the modulator by reducing the maximum stable input amplitude. The maximum stable amplitude (MSA) is sometimes referred to as the overload level.

For an L-th order classical NTF given by (2.12) a closed-form expression can be derived [8] for the modulator dynamic range. To this end, the power spectral density of the quantization noise is obtained as
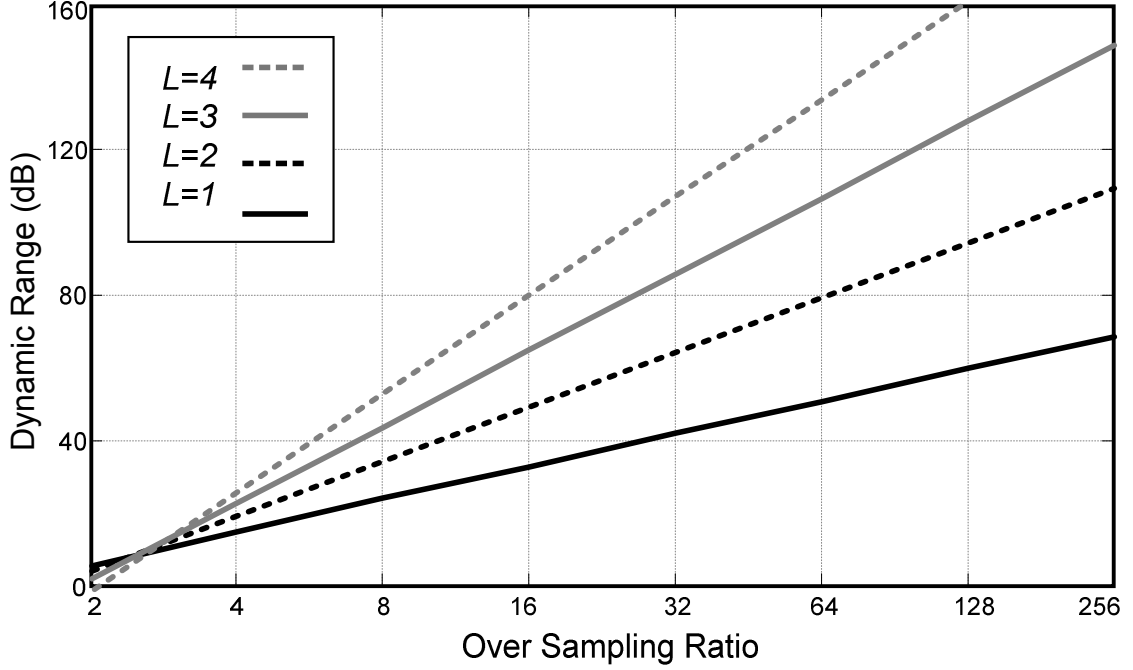
Figure 2.8: single-bit modulator dynamic range versus OSR for different NTF orders.

$$S_Q(f) = S_e(f)\left|NTF(z)\right|^2\Big|_{z=\exp(\frac{j2\pi f}{F_s})}$$

$$= \frac{\Delta^2}{12F_s}\left|1-\exp(\frac{-j2\pi f}{F_s})\right|^{2L} = \frac{\Delta^2}{24f_b OSR}\left[2\sin(\frac{\pi f}{2f_b OSR})\right]^{2L} \qquad (2.13)$$

The power of the in-band quantization noise is obtained by integrating the noise PSD given by (2.13) over the frequency interval $[-f_b, f_b]$

$$P_Q = \int_{-f_b}^{f_b} \frac{\Delta^2}{24f_b OSR}\left[2\sin(\frac{\pi f}{2f_b OSR})\right]^{2L} df = \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)OSR^{(2L+1)}} \qquad (2.14)$$

Using the above equation the ideal SQNR of an *L*-th order $\Delta\Sigma$ modulator with *N*-bit quantization becomes [8]

$$SQNR = \frac{3}{2}\cdot\frac{(2^N-1)^2(2L+1)OSR^{(2L+1)}}{\pi^{2L}} \qquad (2.15)$$

The above equation assumes a full-scale input with the power of $P_{in}=0.5 \ (2^{N-1}\Delta)^2$, where Δ is the quantization step size (i.e. one LSB). It should be noted that (2.15) predicts an upper bound for SQNR and does not take into account any reduction due to overload. The SQNR of single-bit $\Delta\Sigma$ modulators versus OSR is shown in Figure 2.8 for different noise-shaping orders. These graphs show that the slope of *SQNR* versus *OSR* increases by increasing the modulator order *L*, such that for a given dynamic range target a lower *OSR* can be used with the choice of a higher order noise shaping.

2.4 Higher Order Stable NTFs with Optimized Zeros

The maximum out-of-band gain of a classical NTF with all zeros at DC grows exponentially with increasing the modulator order *L* according to $\| \ NTF \ \|_{Fs/2} = 2^L$. A large out-of-band gain reduces the maximum stable input range Therefore, it is imperative in practice to limit the NTF out-of-band gain by proper choice of NTF poles [8]. To this end, the NTF can be implemented as a high-pass Butterworth or inverse Chebyshev transfer function with a cut-off frequency outside the signal band. The out-of-band gain is typically maximized for best SQNR while ensuring loop stability. These transfer functions provide an almost flat stop-band and their zero locations can be optimized for SQNR improvement using the following criteria [8]

$$\min\left[\int_0^{f_b} |NTF(f)|^2 \, df\right] \Rightarrow \begin{cases} \min\left[\int_0^1 \prod_{i=1}^{L/2} (f - f_{zi})^2 df\right] & , \quad \text{L even} \\ \min\left[\int_0^1 f^2 \prod_{i=1}^{(L-1)/2} (f - f_{zi})^2 df\right], & \text{L odd} \end{cases} \quad (2.16)$$
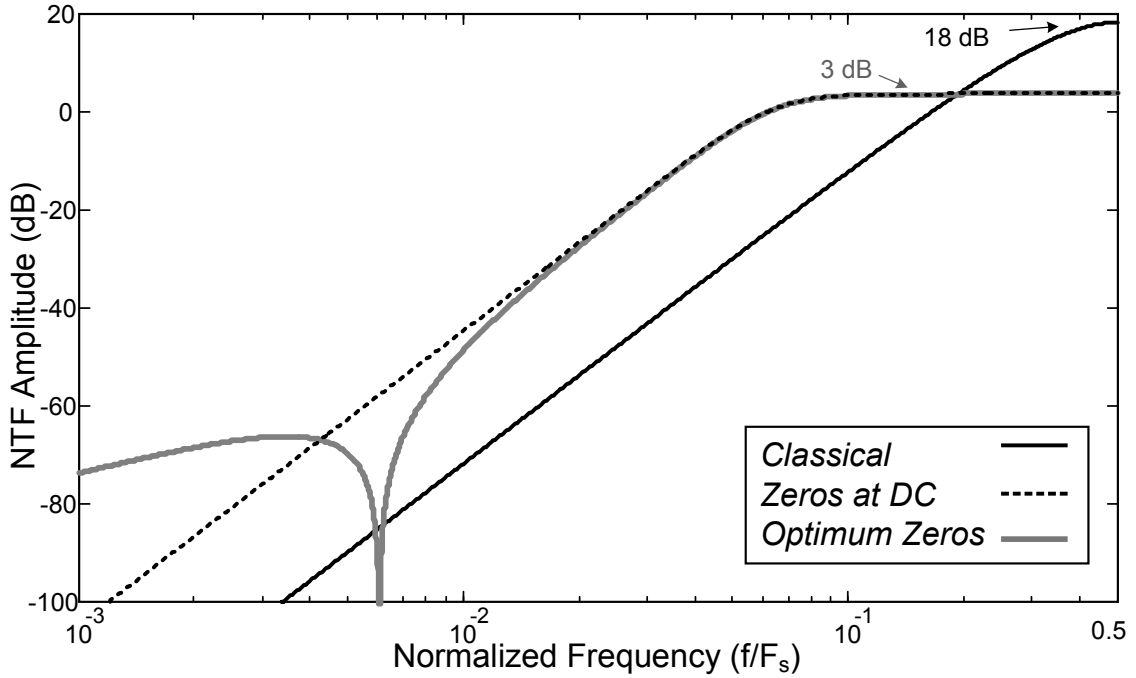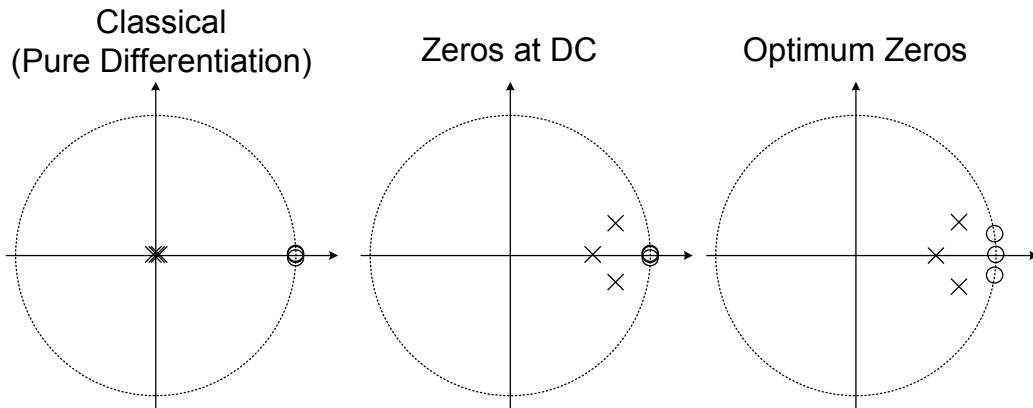
Figure 2.9: (a) Third-order NTF design comparison showing the effect of pole placement on the out-of-band gain. (b) Pole/Zero maps.

A solution to (2.16) for *NTF*s of up to 5-th order and *OSR* of 100 and 64 is given in Table 2.1 where the optimum f_{zi} s are normalized to the signal bandwidth. It is noted that the actual optimum frequencies are inversely proportional to the *OSR* and the improvement in dynamic range ($\Delta SQNR$) depends on the NTF order only and is inde-

Table 2.1: Optimum NTF zeros normalized to the signal bandwidth.

NTF Order	Optimum NTF Zeros	
	Normalized to f_b (f_z / f_b)	Δ *SQNR*
1	0	0
2	±0.5773	+3.5 dB
3	0 , ±0.7744	+8 dB
4	±0.3401 , ±0.8609	+13 dB
5	0 , ±0.5384 , ±0.9059	+18 dB

pendent of *OSR*. Also there is a single zero at DC whenever noise shaping order is odd. A more comprehensive listing of optimum zeros for *NTF*s of up to 8-th order and *OSR* of *64* is provided in [8].

2.5 Multi-Bit Delta-Sigma Modulators

Single-bit quantization is widely used in low-speed $\Delta\Sigma$ ADCs due to its inherent linearity and simple design. However as shown in Figure 2.10(a) a single-bit DAC can assume different gain values when used in the negative feedback loop of a $\Delta\Sigma$ modulator. The gain variability is related to the statistics of the input signal and can be explained by Describing Function (DF) method [9-10]. In higher order modulators with aggressive noise-shaping, the ill-defined gain of a single-bit quantizer can pose serious stability issues. The root locus of a third-order single-bit modulator with different NTF out-of-band gain is shown in Figure 2.11 where the quantizer gain k_q is linearly swept
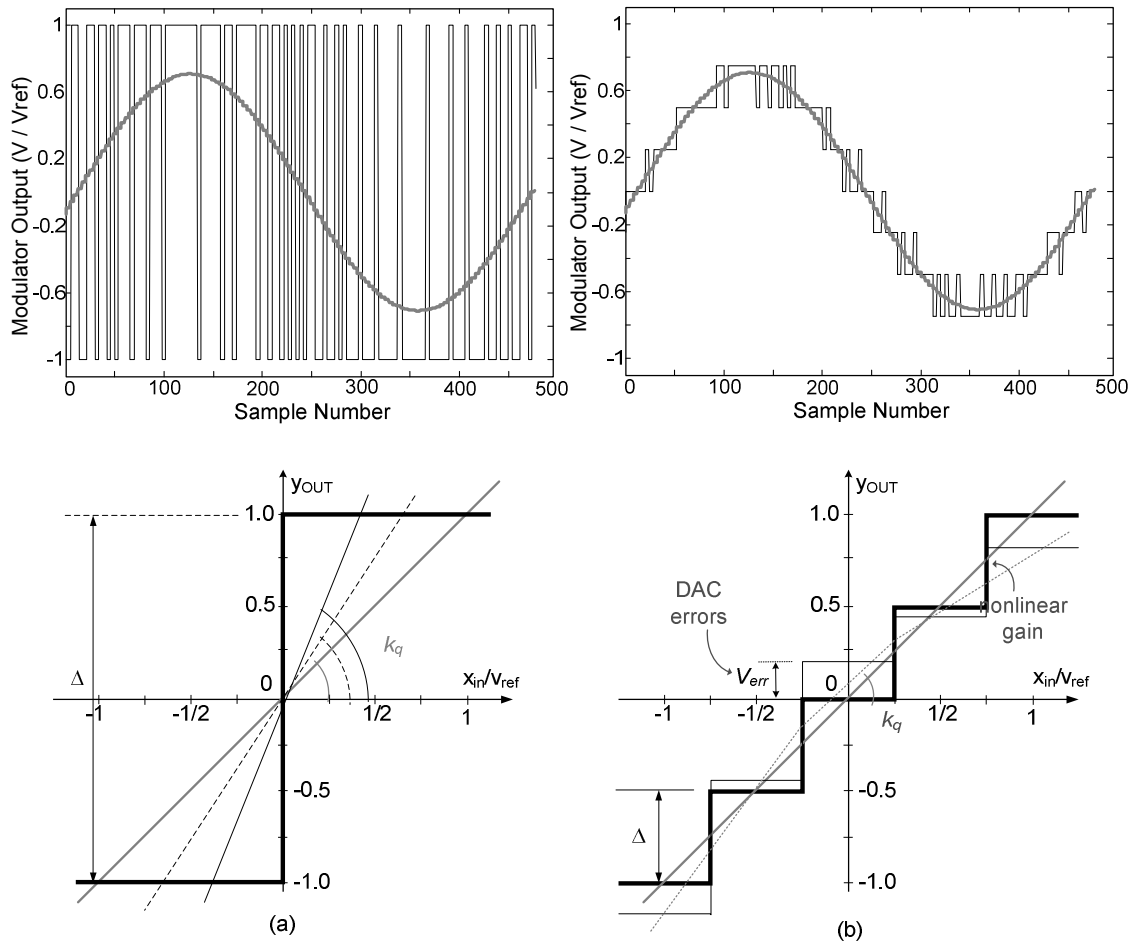
Figure 2.10: ΔΣ Modulator output using (a) Single-bit and (b) Multi-bit quantization shown with respective transfer characteristics.

from 0.1 to 10. It is noted that too small or too large a k_q makes the modulator unstable, and the range of stable gain values gets more and more restricted as the NTF out-of-band gain is increased. The minimum quantizer gain at which the NTF poles stay inside the unit circle is shown by k_{crit}. The critical quantizer gain k_{crit} is related to modulator overload where a smaller k_{crit} implies a higher overload level and vice versa. Therefore, to avoid dynamic range loss associated with overload at low input levels, aggressive noise shaping is not possible in single-bit ΔΣ modulators.
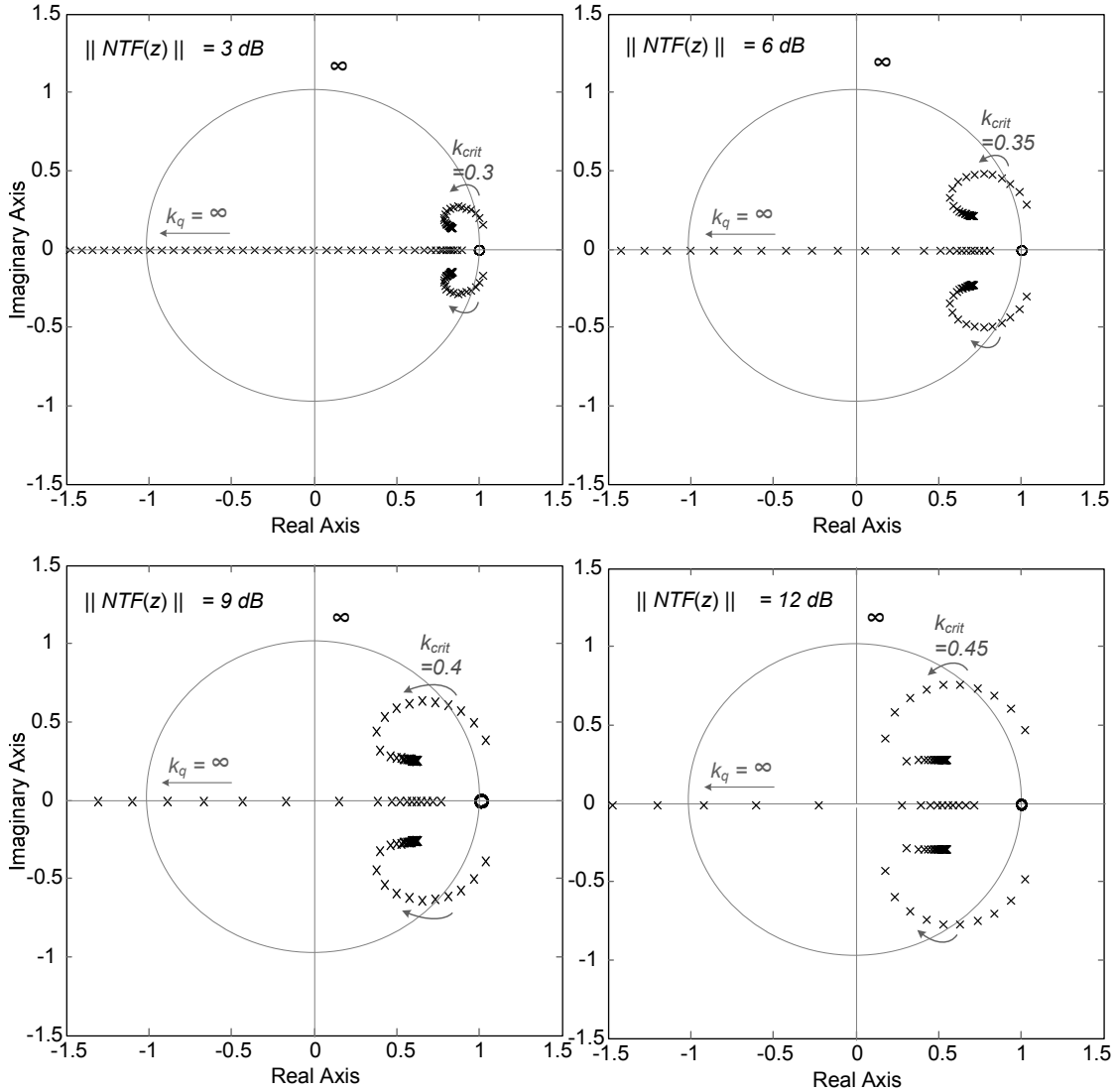
Figure 2.11: Root locus of various single-bit 3rd-order NTFs versus quantizer gain.

A robust solution to this problem without compromising the NTF out-of-band gain is to use a multi-bit quantizer with a defined gain as shown in Figure 2.10(b). However, a multi-bit DAC can be nonlinear due to mismatch among its unit elements. Any error caused by the nonlinearity of the first DAC will find its way to the modulator output through the signal transfer function, just the same way as the input signal. This necessitates improving the element matching of the input DAC to the level

corresponding to the desired ΔΣ modulator linearity. To this end a variety of linearity enhancement techniques have been proposed in the literature in the form of background calibration [11] or dynamic element matching (DEM) [12].

Most DEM techniques attenuate the DAC errors in the signal band by adopting the noise-shaping principle used by ΔΣ modulators. Hence their performance is influenced by the OSR of the modulator. At high oversampling rates a first-order DEM such as data-weighted-averaging (DWA) [13] can significantly relax the matching retirements of the DAC unit elements. However in wide-band modulators with low OSR, mismatch shapers are less effective, and employing a calibration technique to deal with DAC nonlinearity may be a more effective solution.

2.6 Single Loop Delta-Sigma Modulator Architectures

Single loop topologies are widely used because of their lower sensitivity to analog imperfection [8] as opposed to Multi-Loop or cascaded structures which need precision circuits. In the following sections we will review two major classes of single loop modulators using feedback and feedforward architectures and will present the derivation of noise and signal transfer functions in these topologies.

2.6.1 Chain of Integrators with Feedback (CIFB)

An straightforward method for implementing the noise shaping filter of a ΔΣ modulator is through cascading DT integrators with transfer function $I(z) = z^{-1}/(1-z^{-1})$. Figure 2.12 shows such a structure using the cascade of integrators with feedback (CIFB) which includes L feedback DACs attached to the integrator inputs in an Lth-
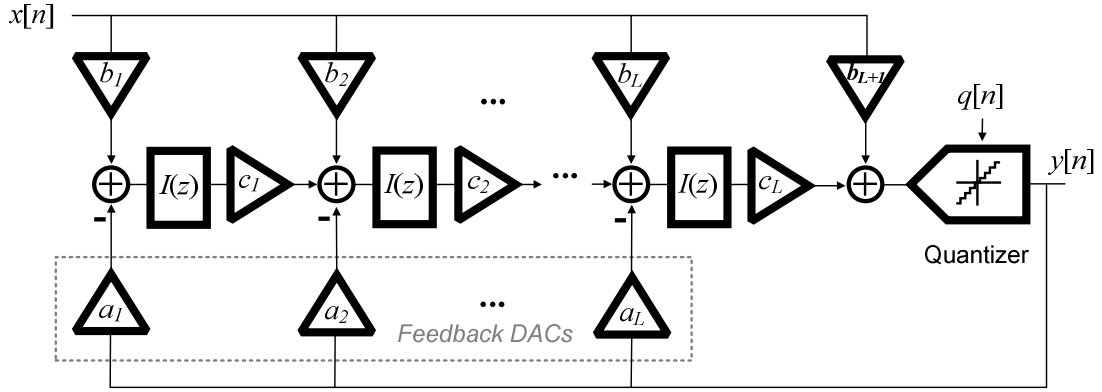
Figure 2.12: ΔΣ modulator using chain of integrators with feedback paths.

order modulator. The modulator feedback and input path transfer functions (see Figure 2.6) are respectively given by $H_d(z)$ and $G_d(z)$ as

$$H_d(z) = \sum_{i=1}^{L} a_i \prod_{j=i}^{L} c_j \left[I(z) \right]^{L+1-i} \qquad (2.17)$$

$$G_d(z) = b_{L+1} + \sum_{i=1}^{L} b_i \prod_{j=i}^{L} c_j \left[I(z) \right]^{L+1-i} \qquad (2.18)$$

In the above, a_i and b_i respectively represent the gain of the feedback and feed-in paths associated with the i-th integrator input, and c_i denotes the scaling factor of the i-th integrator output going to the next stage. Substituting the above equations into (2.7) and (2.9) the NTF and the STF of the CIFB structure are obtained as

$$NTF(z) = \frac{k_q}{1 + k_q \displaystyle\sum_{i=1}^{L} a_i \prod_{j=i}^{L} c_j \left[I(z) \right]^{L+1-i}} \qquad (2.19)$$

$$STF(z) = \frac{k_q \left(b_{L+1} + \displaystyle\sum_{i=1}^{L} b_i \prod_{j=i}^{L} c_j \left[I(z) \right]^{L+1-i} \right)}{1 + k_q \displaystyle\sum_{i=1}^{L} a_i \prod_{j=i}^{L} c_j \left[I(z) \right]^{L+1-i}} \qquad (2.20)$$

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Figure 2.13: $\Delta\Sigma$ modulator using chain of integrators with feedforward paths.

According to (2.19) and (2.20) the a_i coefficients control the NTF of the modulator and b_i coefficients provide leverage on STF zeros. The c_i coefficients are intended for adjusting the integrator output swings. Also It is noted that the choice of $b_i = a_i$, for $i = 1...L$, while $b_{L+1} = k_q^{-1}$ (k_q is the quantizer gain) results in a flat unity gain signal transfer function as *STF=1*. These conditions also eliminate the input signal from the modulator loop filter, and by solely the integrator output swings. In contrast when the input feed-in paths are removed (i.e. $b_i = 0$ for $i=2...L+1$) the integrator outputs will show a large signal swing which includes a significant amount of the input signal plus quantization noise.

2.6.2 Chain of Integrators with Feedforward (CIFF)

An alternative way of implementing single-loop noise shapers is a cascade of integrators with feed-forward paths (CIFF) as shown in Figure 2.13. The CIFF structure relies on a single quantizer feedback and uses *L* feedforward paths to the quantizer input

to implement a target L-th order NTF. The feedback and input path transfer functions $H_d(z)$ and $G_d(z)$ respectively are

$$H_d(z) = \sum_{i=1}^{L} a_i [I(z)]^i \prod_{j=1}^{i} c_j \tag{2.21}$$

$$G_d(z) = b_{L+1} + \sum_{i=1}^{L} \frac{b_i}{c_i} \left(\sum_{j=i}^{L+1-i} a_j [I(z)]^j \prod_{k=1}^{j} c_k \right) \tag{2.22}$$

Using the above definitions in (2.7) and (2.9), the NTF and STF of the CIFF structure are obtained as

$$NTF(z) = \frac{k_q}{1 + k_q \sum_{i=1}^{L} a_i [I(z)]^i \prod_{j=1}^{i} c_j} \tag{2.23}$$

$$STF(z) = \frac{k_q \left\{ b_{L+1} + \sum_{i=1}^{L} \frac{b_i}{c_i} \left(\sum_{j=i}^{L+1-i} a_j [I(z)]^j \prod_{k=1}^{j} c_k \right) \right\}}{1 + k_q \sum_{i=1}^{L} a_i [I(z)]^i \prod_{j=1}^{i} c_j} \tag{2.24}$$

In the above equations c_i is the scaling factor of i-th integrator input and can be used to adjust the integrator output swing. Similar to CIFB topology, the extra feed-in coefficients designated by b_i, $i=2...L+1$, control the STF. When $b_{L+1}=k_q^{-1}$ and $b_i = 0$, for $i=2 \ ... \ L$, the modulator will have a flat unity gain signal transfer function (i.e. $STF=1$). Also under these conditions the modulator loop will process the quantization noise only and whereby eliminating the input signal from the loop filter the signal swing of the integrator outputs will be drastically reduced.

A desirable feature of the CIFF structure is its single overall feedback DAC. This is especially advantageous in multi-standard receiver applications [14] where reconfigurable DACs can take a significant chip area. However the CIFF structure relies

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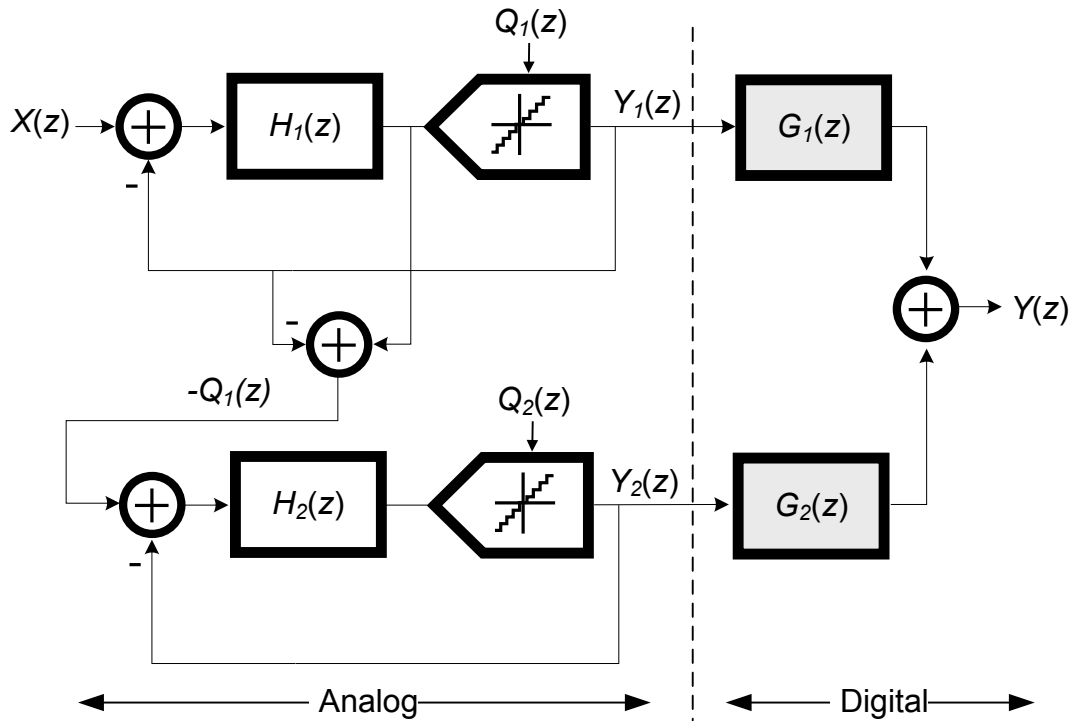
Figure 2.14: $\Delta\Sigma$ modulator with cascade architecture.

on an analog summer in the quantizer front-end which usually takes an extra amplifier to implement. In higher order modulators with numerous feedforward branches, the large feedback factor of the analog summer can pose a design challenge by putting a significant bandwidth requirement on the amplifier.

2.7 Cascade Delta-Sigma Modulator Architecture

An alternative way of realizing higher-order $\Delta\Sigma$ modulators is to cascade more robust lower-order single-loop noise-shapers as shown in Figure 2.14. In this structure the quantization noise of the first modulator is fed to the next stage in the cascade for further noise shaping. The outputs of all stages are combined in digital domain to

increase the noise shaping order. Referring to the 2-stage case shown in Figure 2.14, the

output Y can be expressed in terms of modulator input and the quantization noise as

$$Y(z) = G_1(z)Y_1(z) + G_2(z)Y_2(z) = X(z)STF_1(z)G_1(z) +$$
$$Q_1(z)[NTF_1(z)G_1(z) - STF_2(z)G_2(z)] + Q_2(z)NTF_2(z)G_2(z) \tag{2.25}$$

The above equation suggests that making $G_1(z)= STF_2(z)$ and $G_2(z)=NTF_1(z)$ can cancel

out the quantization error of the first stage. Therefore under ideal conditions the output

of the cascade modulator becomes

$$Y(z)_{ideal} = X(z) \times STF_1(z)STF_2(z) + Q_2(z) \times NTF_1(z)NTF_2(z) \tag{2.26}$$

which shows an overall NTF equal to the product of two lower-order NTF's. In reality,

the $G_1(z)$ and $G_2(z)$ transfer functions are implemented digitally with highest precision

while their corresponding transfer functions $STF_2(z)$ and $NTF_1(z)$ are implemented in

the analog domain using modulator loop filters $H_2(z)$ and $H_1(z)$ respectively. Therefore

the actual modulator output is expressed as

$$Y(z) = X(z) \times STF_1(z)S\widehat{T}F_2(z) + Q_2(z) \times N\widehat{T}F_1(z)NTF_2(z) +$$
$$Q_1(z) \times \left[NTF_1(z)S\widehat{T}F_2(z) - N\widehat{T}F_1(z)STF_2(z)\right] \tag{2.27}$$

In the above the hat sign is used to distinguish the transfer functions implemented in the

digital side. Clearly any mismatch between analog and digital transfer functions can

cause leakage of the quantization noise of the first stage to the output.

Preventing quantization noise leakage puts stringent requirements on the

amplifier DC gain and component matching in both DT and CT implementations [15-

16]. The noise leakage issue is more exacerbated in CT cascaded modulators due to the

dependence of the analog transfer function to the excess-loop-delay (ELD) originated

from the finite speed of the transistors, as well as the dependence on the absolute value of RC-time constants which show large variations over process corners [16].

2.8 Continuous-Time Delta-Sigma Modulators

The background theory provided in the previous sections mostly considered DT $\Delta\Sigma$ modulators which employed sampled-data loop filters. As shown in Figure 2.1(b) $\Delta\Sigma$ modulators can be built around CT loop filters as well. The resulting CT modulator is differentiated from its DT counterpart by the placement of the sampler after the CT filter $H_c(s)$. An implicit benefit of this feature is the free anti-aliasing provided by the modulator filter in the forward path [17]. Another significant advantage is relaxing the linearity requirements of the sampler due to the shaping of its errors by modulator NTF.

Figures 2.15(a) and (b) respectively show the signal flow around the feedback loop of the CT and DT delta sigma modulators. For simplicity the DAC of the CT modulator is assumed to have a zero-order-hold (ZOH) transfer function. In both structures the quantizer input and outputs are sampled-data signals designated by $x[n]$ and $y[n]$, respectively. In the CT $\Delta\Sigma$ modulator the feedback DAC receives a train of sampled-data impulses $y[n]$ and after D/A conversion holds the CT output $y(t)$ until the next clock cycle. However the DAC of the DT modulator reproduces $y[n]$ in analog form without altering its value. Assuming the input signal $u(t)$ to be zero, the output of the CT filter at the sampling instance $x(nT_s)$, will match the output of the DT filter $x[n]$ provided the sampled impulse response of the two loops are equal, in other words [17]

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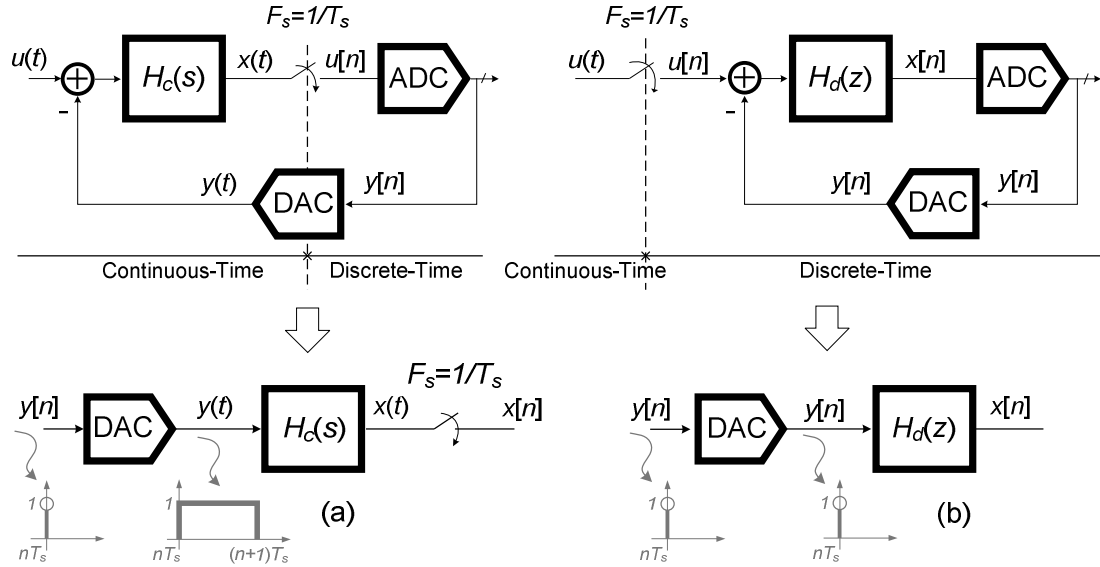
Figure 2.15: Comparison of (a) CT ΔΣ modulator and (b) DT ΔΣ modulator loops.

$$\mathcal{Z}^{-1}\left\{H(z)\right\} = \sum_{n=0}^{\infty} \delta(t - nT_s) \cdot \mathcal{L}^{-1}\left\{LF(s) \cdot H_{DAC}(s)\right\} \tag{2.28}$$

where $Z^{-1}\{.\}$ and $L^{-1}\{.\}$ denote inverse-Z and inverse-Laplace transforms, respectively, and $R_{DAC}(s)$ is the Laplace transform of the DAC output waveform.

In time-domain equation (2.28) can be expressed in terms of DAC waveform $w_{DAC}(t)$ and impulse responses of DT and CT loop filters $h_d[n]$ and $h_c(t)$ as

$$h_d[n] = \left[w_{DAC}(t) * h_c(t)\right]\big|_{t=nT_s} = \sum_{n=0}^{\infty} \int_{-\infty}^{\infty} w_{DAC}(\tau) * h_c(nT_s - \tau)d\tau \tag{2.29}$$

Equations (2.28) and (2.29) are known as the frequency-domain and time-domain forms of the impulse invariant transformation (IIT). It is noted that IIT establishes equivalence between the loop filters of the CT and DT modulators $H_c(s)$ and $H_d(z)$, respectively, based on the fact that both loops receive the same DT impulses and are expected to produce equal outputs at the sampling instants. This equivalence is of great practical

$w_{NRZ}(t)$

$w_{NRZ}(t) = u(t - T_s) - u(t)$

$$W_{NRZ}(s) = \frac{1}{s}\left(1 - e^{-sT_s}\right)$$

(a)

$w_{RZ}(t)$

$w_{RZ}(t) = u(t - \alpha T_s) - u(t - \beta T_s)$

$$W_{RZ}(s) = \frac{e^{-\alpha sT_s}}{s}\left(1 - e^{-(\beta-\alpha)sT_s}\right)$$

(b)

$w_{TRI}(t)$

$$w_{TRI}(t) = \begin{cases} 1 - \dfrac{t/T_s - \alpha}{(\beta - \alpha)} & ; \alpha T_s \leq t < \beta T_s \\ 0 & \text{otherwise} \end{cases}$$

$$W_{TRI}(s) = \frac{e^{-s\alpha T_s}}{s}\left[1 - \frac{1 - e^{-s(\beta-\alpha)T_s}}{s(\beta - \alpha)}\right]$$

(c)

$w_{EXP}(t)$

$$w_{EXP}(t) = \begin{cases} e^{-\left(\frac{t}{T_s} - \alpha\right)/\tau_N} & ; \alpha T_s \leq t < \beta T_s \\ 0 & \text{otherwise} \end{cases}$$

$$W_{EXP}(s) = \frac{T_s \cdot e^{-s\alpha T_s}\left(1 - e^{-(sT_s + \tau_N^{-1})\cdot(\beta-\alpha)}\right)}{sT_s + \tau_N^{-1}}$$

(d)
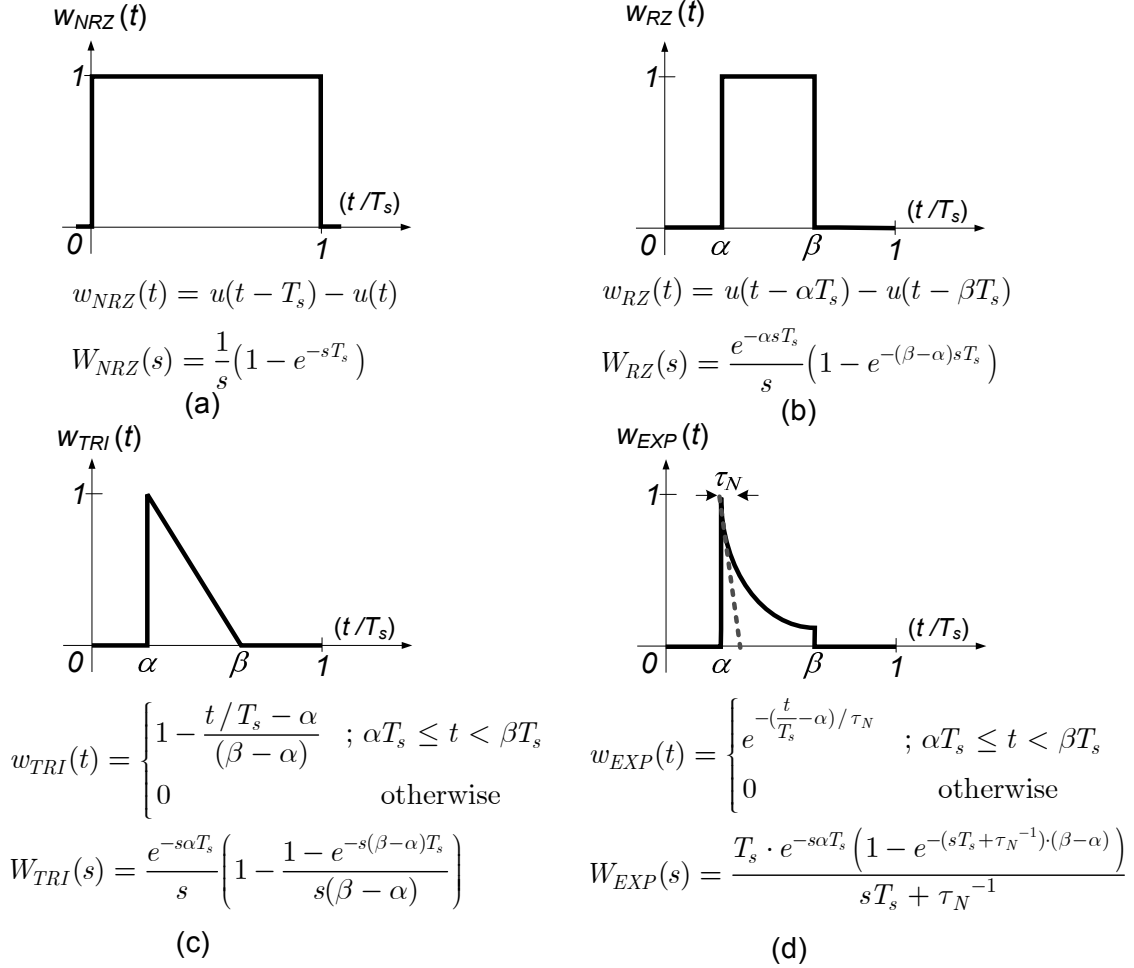
Figure 2.16: DAC waveforms and transfer functions (a) NRZ; (b) RZ ; (c)Triangular; (d) Exponential.

value, since the mature theory of the DT ΔΣ modulators can be readily applied to the design of CT modulators.

2.8.1 DAC Waveforms

Solving the IIT in (2.28) requires knowledge of the DAC transfer function $W_{DAC}(s)$ which is the Laplace transform of the DAC waveform denoted by $w_{DAC}(t)$ in (2.29). Figure 2.16 (a) to (d) shows the transfer function and waveform of no-return-to-

zero (NRZ), return-to-zero (RZ), triangular and exponential DACs respectively. Rectangular waveforms (i.e. NRZ or RZ) are commonly used due to their easier implementation, while the less popular triangular and exponential waveforms would result in better jitter tolerance [18]. All rectangular pulses, including but not limited to NRZ, RZ and half-way-return-to-zero (HZ) can be represented by a pulse with normalized break-points α and β as shown in Figure 2.16(b). The time and frequency domain descriptions of this DAC waveform are, respectively,

$$w_{DAC}(t) = u(t - \alpha T_s) - u(t - \beta T_s) \tag{2.30}$$

$$W_{DAC}(s) = \frac{e^{-s\alpha T_s}}{s}(1 - e^{-s(\beta - \alpha)T_s}) \tag{2.31}$$

In (2.30) $u(t)$ is the Heaviside (unit step) function, T_s is the sampling period, and α and β are normalized breaking points of respectively rising and falling edges where $0 \le \alpha < \beta$, $0 < \beta \le 1$. In an NRZ waveform, $\alpha = 0$ and $\beta = 1$, and using these values in (2.31) results, as expected, in the well-known zero-order-hold (ZOH) transfer function

$$W_{NRZ}(s) = \frac{1}{s}(1 - e^{-sT_s}) \tag{2.32}$$

2.8.2 DT to CT Conversion Using I.I.T

For a known DAC waveform, the CT loop filter $H_c(s)$ can be computed using IIT from the prototype DT loop filter $H_d(z)$. This will ensure that the NTFs of CT and DT modulators match. Similarly a backward transformation from CT to DT allows for modeling the non-idealities of the CT loop filter in the Z-domain for faster simulation. Pre-computed solution of (2.28) for DT-to-CT mapping of basic Z-domain transfer

Table 2.2: DT-to-CT conversion using IIT for rectangular DAC waveform.

z-domain	s-domain equivalent ($T_s = 1$)	Limiting case $z_k = 1$
$\dfrac{1}{z - z_i}$	$\dfrac{r_0}{s - s_k} \times \dfrac{1}{z_k^{1-\alpha} - z_k^{1-\beta}}$ $r_0 = s_k$	$\dfrac{r_0}{s}$ $r_0 = \dfrac{1}{\beta - \alpha}$
$\dfrac{1}{(z - z_i)^2}$	$\dfrac{r_1 s + r_0}{(s - s_k)^2} \times \dfrac{1}{z_k(z_k^{1-\alpha} - z_k^{1-\beta})^2}$ $r_1 = q_1 s_k + q_0$ $r_0 = q_1 s_k^2$ $q_1 = z_k^{1-\beta}(1 - \beta) - z_k^{1-\alpha}(1 - \alpha)$ $q_0 = z_k^{1-\alpha} - z_k^{1-\beta}$	$\dfrac{r_1 s + r_0}{s^2}$ $r_1 = \dfrac{1}{2}\dfrac{\alpha + \beta - 2}{\beta - \alpha}$ $r_0 = \dfrac{1}{\beta - \alpha}$
$\dfrac{1}{(z - z_i)^3}$	$\dfrac{r_2 s^2 + r_1 s + r_0}{(s - s_k)^3} \times \dfrac{1}{z_k^2(z_k^{1-\alpha} - z_k^{1-\beta})^3}$ $r_2 = q_2 s_k / 2 - q_1$ $r_1 = -q_2 s_k^2 + q_1 s_k + q_0$ $r_0 = q_2 s_k^3 / 2$ $q_2 = (z_k^{1-\beta})^2(1 - \beta)(2 - \beta)$ $\quad + (z_k^{1-\alpha})^2(1 - \alpha)(2 - \alpha)$ $\quad + [\beta(\beta + 3) + \alpha(\alpha + 3) - 4(1 + \alpha\beta)]z_k^{1-\alpha}z_k^{1-\beta}$ $q_1 = (z_k^{1-\beta})^2(3/2 - \beta) - (z_k^{1-\alpha})^2(3/2 - \alpha)$ $\quad + (\alpha + \beta - 3)z_k^{1-\alpha}z_k^{1-\beta}$ $q_0 = (z_k^{1-\alpha} - z_k^{1-\beta})^2$	$\dfrac{r_2 s^2 + r_1 s + r_0}{s_k^3}$ $r_2 = \dfrac{1}{12}\dfrac{1}{\beta - \alpha}[\beta(\beta - 9)$ $\quad + \alpha(\alpha - 9) + 4\alpha\beta + 12]$ $r_1 = \dfrac{1}{12}\dfrac{\alpha + \beta - 3}{\beta - \alpha}$ $r_0 = \dfrac{1}{\beta - \alpha}$

functions of the form $1/(z - z_i)^n$ are given in Table 2.2 for up to the 3-rd order. The

DAC is assumed to have a rectangular waveform with breakpoints of α and β and a

normalized sampling period of $T_s = 1$. An interesting outcome of applying IIT is that a

Z-domain pole z_k with multiplicity of n is mapped onto an S-domain pole s_k of the same

such that
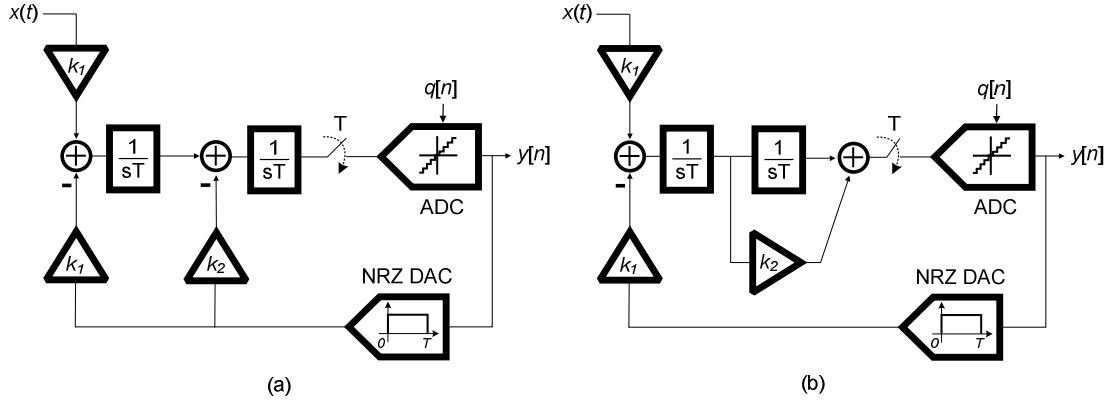
Figure 2.17: 2nd-order CT ΔΣ modulator implementations (a) CIFB, (b) CIFF.

$$s_k = \frac{1}{T_s} \ln(z_k) \tag{2.33}$$

As an example, let's consider a second order ΔΣ modulator. The goal is to compute the loop-filter of a CT modulator with NRZ DAC (i.e. $\alpha{=}0$ and $\beta{=}1$) such that multiplicity its NTF becomes $(1{-}z^{-1})^2$. Using (2.8) and assuming a unity gain quantizer with $k_q{=}1$, the required DT loop filter is calculated from the NTF as

$$H_d(z) = \frac{-2z + 1}{(z - 1)^2} \tag{2.34}$$

Taking the partial fraction expansion of (2.34) yields

$$H_d(z) = \frac{-2}{z - 1} + \frac{-1}{(z - 1)^2} \tag{2.35}$$

Referring to the Table 2.2 data the CT transfer function is obtained as

$$I.I.T\{H_d(z)\}_{NRZ} = H_c(s) = \frac{1.5}{s} + \frac{1}{s^2} \tag{2.36}$$

In both CIFB and CIFF prototype modulators shown in Figure 2.17(a) and (b), the CT loop TF is given by

$$H_c(s) = \frac{k_2}{s} + \frac{k_1}{s^2} \tag{2.37}$$

Comparison the above equation with (2.36) results in the coefficient values of $k_1=1$ and

$k_2=1.5$ in both structures.

2.8.3 CT to DT Conversion Using Modified Z-Transform

The modified Z-transform is a convenient and versatile tool for discretizing the

CT filters. This approach is an extended form of the Z-transform which accounts for the

CT events at all times in the calculated DT system. This is particularly useful in mixed-

signal sampled-data systems that include delay or sample-rate conversion. The

definition of the modified-Z-transform for a CT signal $f(t)$ is [19]

$$\mathscr{Z}_m = \sum_{n=0}^{\infty} f[(n-1+m)T_s]z^{-n}, \quad 0 \le m \le 1 \tag{2.38}$$

In the above, m is a fractional parameter related to the delay time t_d as $m=1-t_d/T_s$. It is

noted that the Z-transform is a special case of the modified-Z-transform with $m = 1$ (i.e.

no delay or $t_d = 0$). Considering the loop transfer function of the CT $\Delta\Sigma$ modulator

shown in Figure 2.15(a) the equivalent DT loop filter $H_d(z)$ can be computed using the

modified-Z-transform as

$$H_d(z) = \sum_{m_i} \mathscr{Z}_{m_i} \{H_c(s)W_{DAC}(s)\} \tag{2.39}$$

The parameter m_i in the above equation is related to the break points in the DAC

waveform. For instance, in the case of the rectangular waveform shown in Figure

2.16(b) the m_i values are obtained as $m_1=1-\alpha$ and $m_2=1-\beta$.

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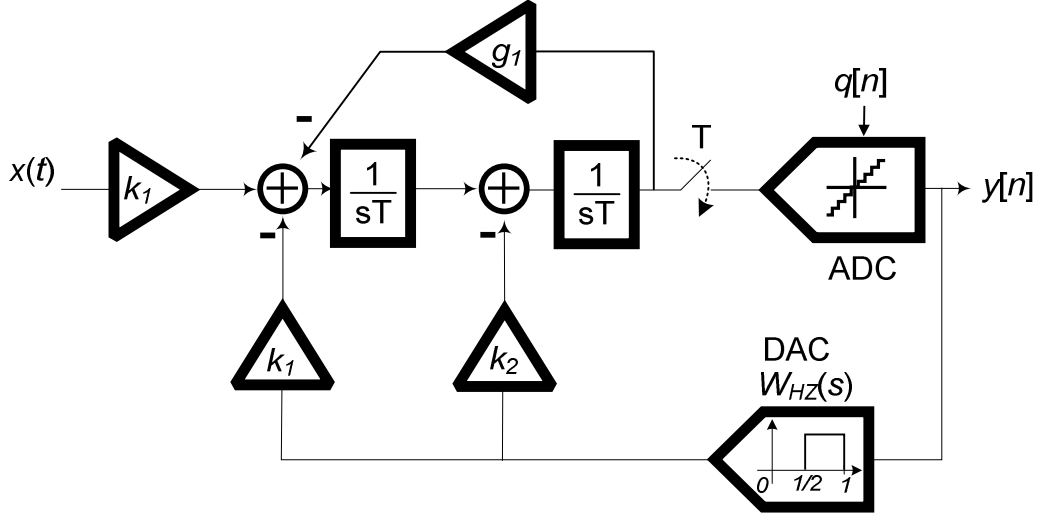
Figure 2.18: 2nd-order CIFB prototype CT $\Delta\Sigma$ modulator with triangular DAC.

The application of the modified Z-transform to discretization of CT $\Delta\Sigma$ modulator loops is explained by way of example. Consider the second-order prototype modulator shown in Figure 2.18 with a half-return-to-zero (HZ) DAC waveform and unknown coefficients k_1, k_2 and g_1. The goal is to derive the modulator coefficients such that it shows a 2nd-order NTF with 3dB out-of-band gain and optimized zeros at *OSR=32* as

$$NTF(z) = \frac{z^2 - 1.997z + 1}{z^2 - 1.224z + 0.441} \tag{2.40}$$

Using (2.8) and assuming a quantizer gain of $k_q=1$ the target DT loop filter becomes

$$H_d(z) = \frac{0.773z \text{ - } 0.559}{z^2 - 1.997z + 1} \tag{2.41}$$

Also the loop filter of the CT modulator is derived from Figure 2.18 as

$$H_c(s) = \frac{k_1 + k_2 s}{s^2 + g_1} = \frac{k_1 + k_2 s}{s^2 + \gamma^2} \tag{2.42}$$

Table 2.3: Modified Z-Transform of basic CT transfer functions up to 4-th order.

CT transfer function	Modified Z-Transform
$\dfrac{1}{s^2}$	$\dfrac{mT}{z-1} + \dfrac{T}{(z-1)^2}$
$\dfrac{1}{s(s+a)}$	$\dfrac{1}{a}\left(\dfrac{1}{z-1} - \dfrac{e^{-maT}}{z-e^{-aT}} \right)$
$\dfrac{1}{s^2+\gamma^2}$	$\dfrac{1}{\gamma}\left(\dfrac{z\sin(m\gamma T) + \sin[(1-m)\gamma T]}{z^2 - 2z\cos(\gamma T) + 1} \right)$
$\dfrac{1}{s^3}$	$\dfrac{T^2}{2}\left[\dfrac{m^2}{z-1} + \dfrac{2m+1}{(z-1)^2} + \dfrac{2}{(z-1)^3} \right]$
$\dfrac{1}{s^2(s+a)}$	$\dfrac{1}{a^2}\left(\dfrac{maT-1}{z-1} + \dfrac{aT}{(z-1)^2} + \dfrac{e^{-maT}}{z-e^{-aT}} \right)$
$\dfrac{1}{s(s^2+\gamma^2)}$	$\dfrac{1}{\gamma^2}\left(\dfrac{1}{z-1} - \dfrac{z\cos(m\gamma T) - \cos[(1-m)\gamma T]}{z^2 - 2z\cos(\gamma T) + 1} \right)$
$\dfrac{1}{s^4}$	$\dfrac{T^3}{6}\left[\dfrac{m^3}{z-1} + \dfrac{3m^2+3m+1}{(z-1)^2} + \dfrac{6m+6}{(z-1)^3} + \dfrac{6}{(z-1)^4} \right]$
$\dfrac{1}{s^3(s+a)}$	$\dfrac{1}{a^3}\left(\dfrac{m^2a^2T^2/2 - maT + 1}{z-1} + \dfrac{(m+1/2)a^2T^2 - aT}{(z-1)^2} + \dfrac{a^2T^2}{(z-1)^3} - \dfrac{e^{-maT}}{z-e^{-aT}} \right)$
$\dfrac{1}{s^2(s^2+\gamma^2)}$	$\dfrac{1}{\gamma^3}\left(\dfrac{m\gamma T}{z-1} + \dfrac{\gamma T}{(z-1)^2} - \dfrac{z\sin(m\gamma T) + \sin[(1-m)\gamma T]}{z^2 - 2z\cos(\gamma T) + 1} \right)$

while the DAC transfer function using the data shown in Figure 2.17(b) is

$$W_{DAC}(s) = \mathcal{L}\left\{ w_{HZ}(t) \right\}\Big|_{T_s=1} = \frac{e^{-s/2} - e^{-s}}{s} \tag{2.43}$$

Note that a normalized sampling period of $T_s=1$ is assumed in this example to simplify the derivations. Applying (2.39) to the loop transfer function of the modulator leads to

$$H_d(z) = k_2 \left\{ \mathcal{Z}_{m_1}\left(\frac{1}{s^2+\gamma^2}\right)_{m_1=1/2} - \mathcal{Z}_{m2}\left(\frac{1}{s^2+\gamma^2}\right)_{m_2=0} \right\}$$
$$+ k_1 \left\{ \mathcal{Z}_{m_1}\left(\frac{1}{s(s^2+\gamma^2)}\right)_{m_1=1/2} - \mathcal{Z}_{m2}\left(\frac{1}{s(s^2+\gamma^2)}\right)_{m_2=0} \right\} \qquad (2.44)$$

In the above, parameter γ is related to the resonator feedback as $\gamma^2 = g_1$ (see (2.42)).

The Z_m-domain equivalents of the basic CT transfer functions of up to the 4th order are listed in Table 2.2 [19]. Substituting for TF's in (2.44) from 3rd and 6th rows of Table 2.2 we obtain

$$H_d(z) = \frac{k_2}{\gamma} \cdot \frac{z\sin(\frac{\gamma}{2}) + [\sin(\frac{\gamma}{2}) - \sin(\gamma)]}{z^2 - 2z\cos(\gamma) + 1}$$
$$+ \frac{k_1}{\gamma^2} \cdot \frac{-z[\cos(\frac{\gamma}{2}) - 1] + [\cos(\frac{\gamma}{2}) - \cos(\gamma)]}{z^2 - 2z\cos(\gamma) + 1} \qquad (2.45)$$

Comparing the above equation with (2.41) a nonlinear system of equations with three equations and three unknown is formed which its solutions yields the coefficient values as $g_1=0.003$, $k_1=0.436$ and $k_2=1.44$.

2.8.4 Excess Loop Delay

In practical CT-$\Delta\Sigma$ modulators, there exists a certain amount of delay between the quantizer sampling instance and the DAC output, which originates from the limited switching speed of the transistors. This pure delay is known as excess loop delay (ELD) [20] which can be detrimental to the stability of the modulator loop. If the DAC waveform is not contained in one sampling period and enters the adjacent cycle due to the ELD, the effective order of the loop filter will be increased. As shown in Figure 2.19
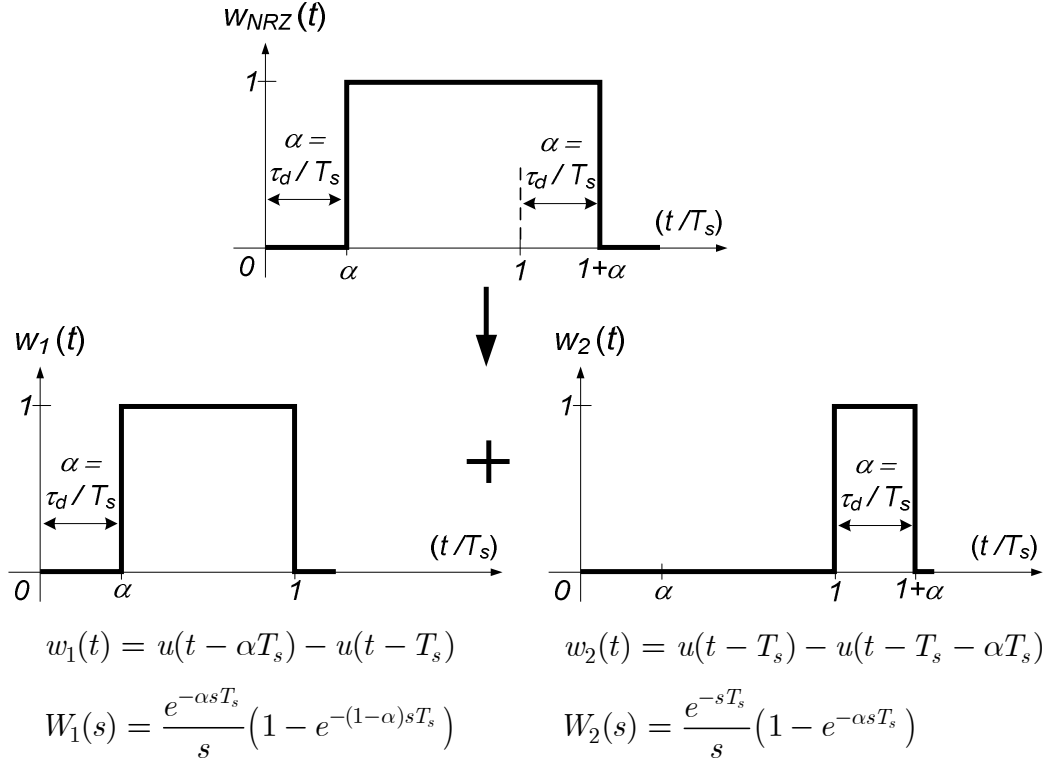
Figure 2.19: Decomposition of a delayed DAC waveform.

this increase in the loop-filter order can be explained by modeling the delayed DAC waveform as the superposition of two individual pulses as

$$w(t) = w_1(t)|_{(\tau_d, T)} + w_2(t - T)|_{(0, \tau_d)} \tag{2.46}$$

where $w_1(t)$ represents a pulse from $\alpha = \tau_d$ to $\beta = T$, and $w_2(t)$ represent a pulse from $\alpha = 0$ to $\beta = \tau_d$ delayed by one clock cycle. The resulting Z-transform is calculated as the superposition of the two terms, where the term associated with $w_2(t)$ includes a z^{-1} factor which is responsible for the increased order of the loop filter.

Let's consider the 2nd-order prototype modulators shown in Figure 2.17. The equivalent DT loop filter can be computed as a function of the ELD by applying the modified Z-transform to the $1/s$ and $1/s^2$ terms of the $H_c(s)$ in (2.37)
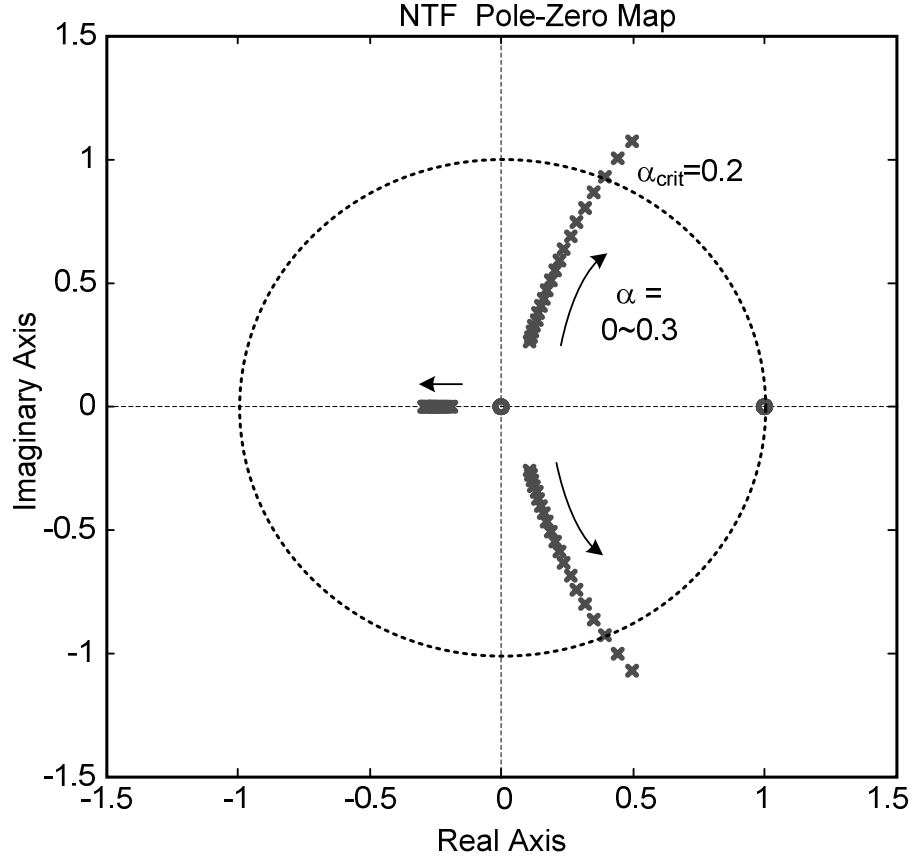
Figure 2.20: NTF Pole/Zero map subject to 0 to 30% ELD.

$$\frac{1}{s} \rightarrow \frac{1-\alpha}{z-1} + z^{-1}\frac{\alpha}{z-1} \tag{2.47}$$

$$\frac{1}{s^2} \rightarrow \frac{(0.5\alpha^2 - \alpha + 0.5)z + 0.5(1-\alpha^2)}{(z-1)^2} + z^{-1}\frac{\alpha(1-0.5\alpha)z + 0.5\alpha^2}{(z-1)^2} \tag{2.48}$$

Using $k_1=1$ and $k_2=1.5$ in (2.37) the discretized loop filter becomes

$$H_d(z,\alpha) = \frac{1}{2}\cdot\frac{z^2(4-\alpha)(1-\alpha) - 2z(\alpha^2 - 4\alpha + 1) + \alpha(3-\alpha)}{z(z-1)^2} \tag{2.49}$$

The root-locus of the NTF poles versus normalized ELD of α is plotted in Figure 2.20 where the DT loop transfer function of the modulator is given by (2.49). Clearly the number of poles is increased from 2 to 3 even for an infinitesimal delay. Further
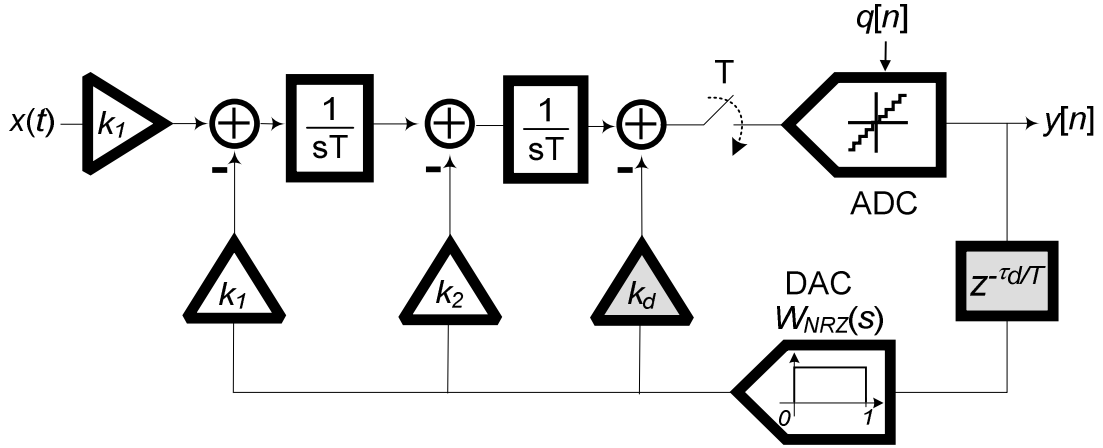
Figure 2.21: Use of direct feedback for ELD compensation.

increase of ELD pushes NTF poles outside of the unit circle where the critical delay is shown with $\alpha_{crit} = 0.2$.

The effect of ELD on the stability manifests itself as reduced overload-level which adversely affects the modulator dynamic range. It has also been shown that the ELD can elevate the quantization noise floor by degrading the NTF at low-frequencies [20]. Therefore to avoid potential dynamic range losses the excess delay in CT $\Delta\Sigma$ modulator loops needs to be controlled.

2.8.5 Classical ELD Compensation

The ELD of a CT $\Delta\Sigma$ modulator can be compensated by adding a direct feedback to the quantizer input [21] as shown in Figure 2.21. The CT modulator loop filter can be expressed in terms of the coefficients k_1, k_2 and k_d as

$$H_c(s) = \frac{k_1}{s^2} + \frac{k_2}{s} + k_d \tag{2.50}$$

Assuming a normalized ELD of α and NRZ DAC waveform, the equivalent DT loop filter can be obtained from the right-half-side (RHS) of (2.47) and (2.48)

$$H_d(z) = k_d z^{-1} + k_2 \times (\text{RHS of } (2.47)) + k_1 \times (\text{RHS of } (2.48)) = \frac{2z - 1}{(z - 1)^2} \quad (2.51)$$

In the above equation the parametric $H_d(z)$ is matched with the ideal loop TF of the second-order modulator given in (2.34). From the comparison of the numerator terms a system of three equations and three unknowns is formed as

$$\begin{cases} 0.5\alpha^2 k_1 - \alpha k_2 + k_d = 0 \\ (0.5 + \alpha - \alpha^2)k_1 + (2\alpha - 1)k_2 - 2k_d = -1 \\ (0.5\alpha^2 - \alpha + 0.5)k_1 + (1 - \alpha)k_2 + k_d = 2 \end{cases} \quad (2.52)$$

Solving the system of nonlinear equations in (2.52) yields the coefficient values of the delay compensated modulator as $k_1=1$, $k_2=1.5+\alpha$ and $k_d=0.5\alpha(\alpha+3)$. For example assuming a 50% ELD or $\alpha = \tau_d / T_s = 1/2$, the modulator coefficients become 1, 2 and 0.875 for k_1, k_2 and k_d respectively.

The direct feedback technique can also be used to compensate for the limited unity-gain-bandwidth (UGBW) of the amplifiers [22] or any non-ideality similar to ELD that causes phase lagging in the modulator loop.

2.9 State-of-The-Art and Design Trends

A literature survey on recently published ΔΣ modulators is summarized in Table 2.4. As stated earlier, ΔΣ modulators can be categorized under two distinct families of DT and CT based on the structure of their loop filter. DT modulators are implemented by one of the switched-capacitors (SC) or switched-currents (SI) techniques and CT modulators are often realized by Active-RC or Gm-C techniques. The signal bandwidth (f_{BW}), signal-to-noise-ratio (SNR), signal-to-noise-and-distortion-ratio (SNDR), and power consumption are key performance metrics that can be used for comparing different designs.

The figure-of-merit (FOM) for ADCs suggested by the analog committee of the IEEE International Solid-State Circuits Conference [23] takes into account the power dissipation, resolution, and sampling rate of ADCs It represents the energy used per conversion step

$$FOM_{ADC} = \frac{P}{2^N f_{BW}}$$

(2.53)

where P is the power consumption, N is the stated number of bits, and F_S is the sampling rate. The FOM in (2.53) produces optimistic results by not accounting for the performance limitation of ADCs due to harmonic distortion. Based on the peak signal-to-noise-and-distortion-ratio (SNDR) of an ADC its effective-number-of-bits (ENOB) is defined as

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

(2.54)

A FOM which is common in the recent literature [24] takes into account the ENOB and the Nyquist rate instead of the sated number-of-bits (i.e. N in (2.53)) and the

sampling frequency respectively. This figure of merit is known as the quantization energy which is defined as

$$FOM_1 = \frac{P}{2^{ENOB}(2f_{BW})} \qquad (2.55)$$

There is another FOM for ADCs suggested earlier by Robert Walden [25] which is nearly the inverse of (2.55)

$$FOM_2 = \frac{2^{ENOB} F_s}{P} \qquad (2.56)$$

The *FOM$_1$* in (2.55) emphasizes the power consumption, where the Walden's FOM in (2.56) emphasizes the effective resolution of an ADC. When comparing $\Delta\Sigma$ modulators a smaller *FOM$_1$* or a larger *FOM$_2$* suggests a better performance.

In order to obtain an idea about the current design trends, and to compare the potentials of DT and CT implementations we have surveyed both design approaches. Figure 2.22 puts into contrast the SNDR performance versus signal bandwidth of CT and DT implementations. From the data, the highest signal bandwidth (or conversion speed) is achieved by a CT design. Even though higher dynamic range designs are mostly DT, those implementations are still in the low-bandwidth range. In a different comparison, power consumption versus signal bandwidth is plotted in Figure 2.23 which shows that CT designs, even at wider bandwidths, show less power consumption than their DT counterparts. A final comparison is provided in Figure 2.24 based on the publication year and achieved FOM. The data clearly show that the current trend is toward CT designs and an increasing number of published $\Delta\Sigma$ works are based on the CT approach. Moreover, it is seen that the CT designs have a better FOM than their DT counterparts, which can explain the motivation behind the existing design trend.

Table 2.4: State of the Art Technology in Delta-Sigma Modulator Design.

Type	Ref.	Year	Fs (MHz)	BW (MHz)	Vdd (V)	P (mW)	SNDR (dB)	FOM₂ (MHz/mW)	Architecture	Process (nm)
DT	JSSC01 Vleugels	2001	64	2	2.5	150	87	308	2(5B)-2(3B)-1(3)	500
	ISSCC02 Jiang	2002	32	2	1.8	150	82	173	5(4B)	180
	ISSCC03 Dezzani	2003	38.4	2	1.2	4.3	64	756	2(2.3B)-1(2.3B)	130
	JSS04 Balmelli	2004	200	12.5	1.8	200	72	256	5(4B)	130
	ISSCC04 Gaggl	2004	105	1.1	1.2	15	76	476	1(3B)	130
	JSSC05 Nam05	2005	40	1.25	1.2	87	89	419	2(5B)-2(3B)	250
	ISSCC05 Yu	2005	40	1	1.3	2.1	61	547	2(4B-DEM Less	90
	ISSCC05 Fujimoto	2005	100	4	1.8	35	70	371	4(4B)	180
	ISSCC05 Brewer	2005	20	1.25	2.5	215	97	427	2(5B)-2(3.3B)-Flash(3.3)	250
	ISSCC05 Bosi	2005	80	10	3.3	185	73	248	2(4b)+Pipeline(9b)+LMSFIR	180
	ISSCC06 Kwon	2006	144	2.2	1.8	14	82	2043	2(3.3B)	180
	JSSC09 Fujimoto	2009	100	4	1.2 / 3	11.7	65.1	1005	4 (4B)+DEM	90
CT	JSSC02 Henkel	2002	100	1	2.7	21.8	56.7	32	2(1B) Complex	650
	ISSCC03 Philips	2003	64	1	1.8	4.4	75.5	1394	5(1B) Complex	180
	JSSC03 Veldhoven	2003	154	2	1.6	4.5	72	1820	5(1B)	180
	ISSCC04 Putter	2004	280	1.1	1.8	6	77	1338	3(1B-9FIRDAC)	180
	ISSCC04 Yan	2004	35.2	1.1	3.3	62	83	258	3(5B)	500
	JSSC04 Paton	2004	300	15	1.5	70	64	348	4(4B)	130
	JSSC04 Dagher	2004	2000	1.23	1.8	18	79	628	2(1B)	180
	JSSC05 Philips	2005	64	1	1.8	2.1	59	434	4(1B)	180
	JSSC05 Dorrer	2005	104	2	1.5	3	70	2167	3(4B-Tracking)	130
	ISSC06 Mittereger	2006	640	20	1.2	20	74	4096	3(4B)	130
	JSSC09	2009	250	10	1.2	18	65	1614	3 (4B)	130
	JSSC-11 Kauffmann	2011	500	25	1.2	8.5	63.5	7192	3 (4B)	90
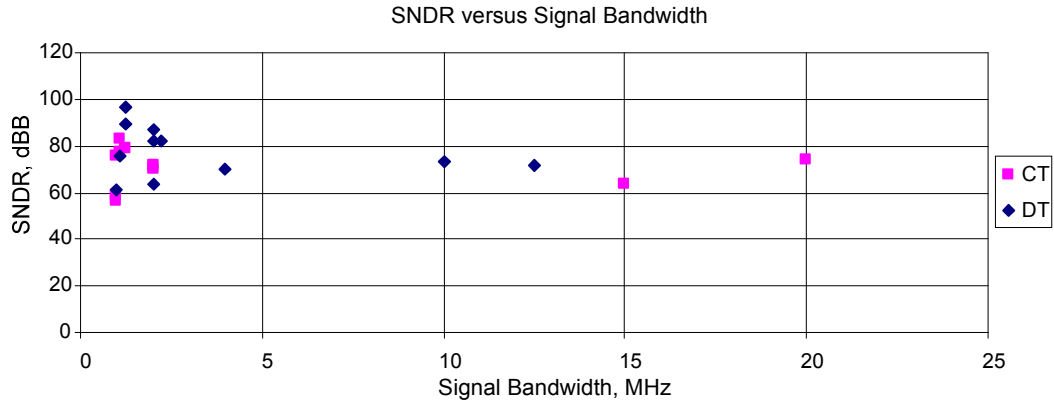
Figure 2.22: SNDR and signal bandwidth of recently published ΔΣ modulators.
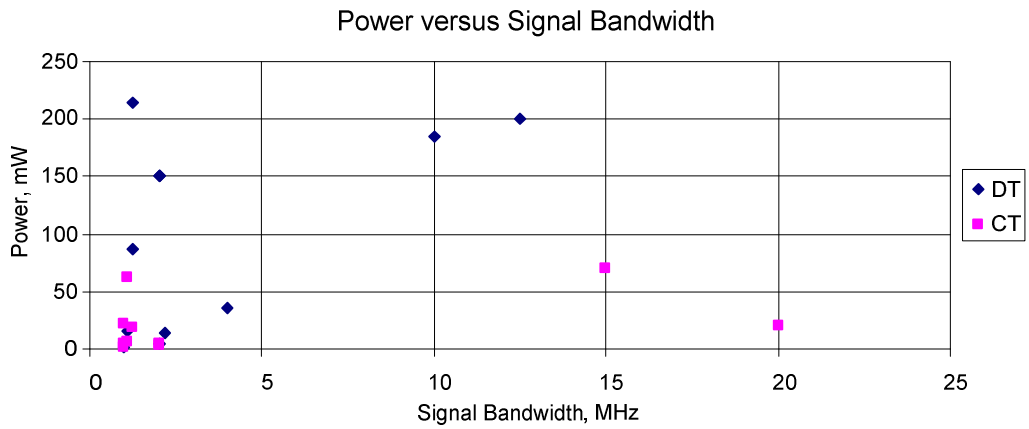
Figure 2.23: Power and signal bandwidth comparison of recent publications.
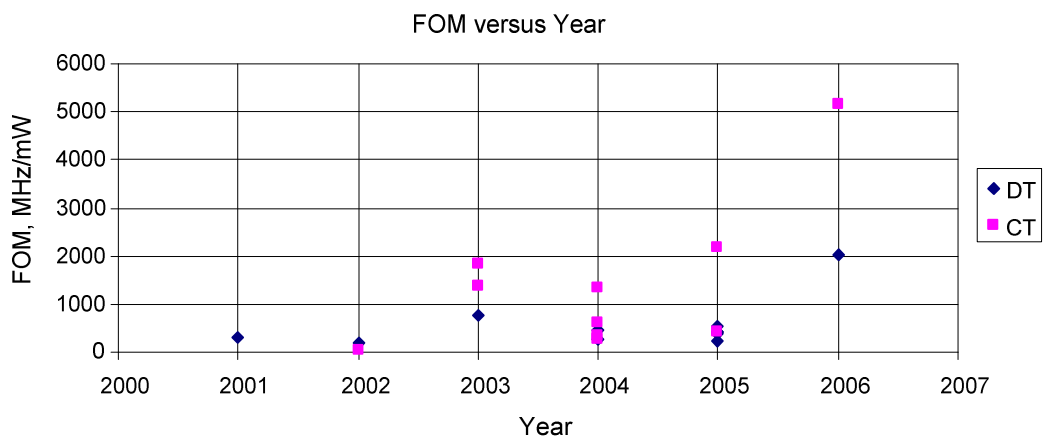
Figure 2.24: Comparison of FOM and Publication year for CT and DT.

2.10 Summary

This chapter provided a brief introduction to the fundamental theory of the delta-sigma modulators. The classical architectures and design trade-offs were discussed and important design equations and their application was explained by way of example. Also important non-idealities, such as excess loop-delay pertinent to CT $\Delta\Sigma$ modulators, were explained and the delay compensation technique was presented in details. The fundamental theory provided in this chapter will be frequently referred to and used throughout this dissertation.

CHAPTER 3

BEHAVIORAL MODELING OF NON-IDEALITIES

A continuous-time delta-sigma modulator is a mixed-signal system composed of digital and analog building blocks. Designing a robust modulator requires thorough analysis and simulation to make sure that each sub block functions as expected in conjunction with all other blocks and the whole system meets the design targets. Traditional tools such as SPICE are slow and inefficient for mixed-mode simulations and take too long for most optimizations. On the other hand, behavioral modeling can reduce the design and simulation time and also provide better insight into the system behavior in the presence of non-idealities. Behavioral models are a set of equations or look-up tables that define the relationship between the inputs and outputs of each sub-block. In this work we have used standard tools like MATLAB and SIMULINK [26] for modeling purposes.

The following sections will explain the modeling techniques used in this work for analyzing the effect of important non-idealities such as, amplifiers limited unity gain-bandwidth and DC gain, amplifiers input stage nonlinearity, DAC element mismatch, ADCs comparator random offset, and clock jitter.

3.1 Amplifier Unity Gain Bandwidth

The loop filter of a CT-$\Delta\Sigma$ modulator is made up of a cascade of CT integrators. The integrator can be implemented using the Active-RC or gm-C techniques as shown in Figure 3.1(a) and (b) respectively. In this work we will only consider Active-RC integrators due to their high linearity and their ability to provide a current sink path to
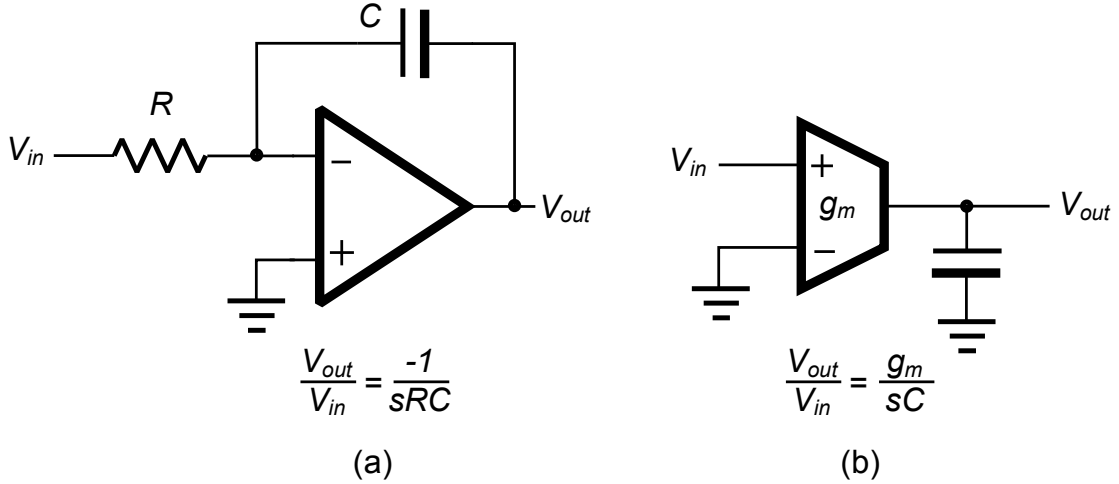
Figure 3.1: Continuous-Time integrators (a) Active-RC and (b) Gm-C .

$$\frac{V_{out}}{V_{in}} = \frac{-1}{sRC}$$

(a)

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{sC}$$

(b)

(a)

(b)

$$A_v = -\frac{V_{out}}{V_x}$$
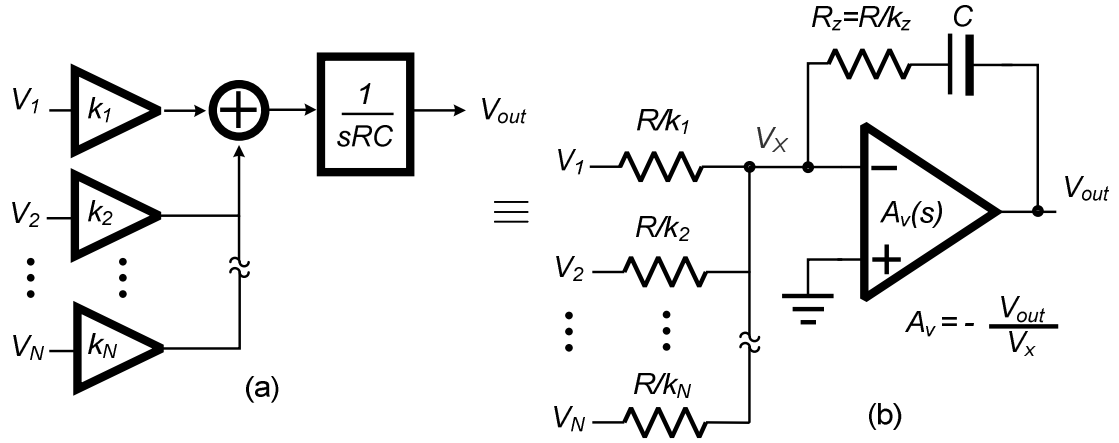
Figure 3.2: (a) A CT integrator use-case in a DS modulator; (b) Circuit level implementation using Active-RC technique.

the feedback DACs. Figure 3.2(a) shows the block diagram of a multi-input CT integrator with $k_1 \ldots k_N$ input scaling factors. The ideal integrator output can be written in terms of the input signals as

$$V_{out} = \frac{1}{sRC}(k_1 V_1 + k_2 V_2 + \ldots + k_N V_N) \tag{3.1}$$

The active-RC implementation of the above equation is shown in Figure 3.2(b). The unity-gain angular frequency of an integrator with gain $k_1{=}1$ is equal to the sampling

frequency F_s or proportional to the inverse of the RC-time-constant (i.e. $\omega_u = 1/RC = F_s$). The input gains are implemented by scaling the reference resistor R ($RC = T_s$) according to coefficients $k_1 \dots k_N$. The feedback resistor R_z is present either implicitly, as the resistance of the capacitor trimming switch, or explicitly as the nulling-resistor that adds a zero to the TF. The normalization factor k_z is used to represent the feedback resistance the same way as the k_i's for the input resistors. Since the Active-RC integrator employs an amplifier in its core, its transfer function will be affected by the amplifier non-idealities such as limited gain-bandwidth. The Active-RC integrator output voltage in Figure 3.2(b) can be written as

$$V_{out} = \frac{-\sum_{i=1}^{N} k_i V_i}{sRC} \left[(\frac{sRC}{k_z} + 1) \frac{A_v(s)\beta(s)}{[1 + A_v(s)\beta(s)]} \right] \tag{3.2}$$

In the above equation $\beta(s)$ is the feedback factor of the integrator loop and $A_v(s)$ is the voltage transfer function of the amplifier from the virtual ground node V_x to the output node. It is noted that the first factor in (3.2) represents the ideal transfer-function, the second factor describes the zero due to the series resistance, and finally the third factor accounts for the amplifier and feedback non-idealities. The feedback factor $\beta(s)$ is derived from Figure 3.2(b) as

$$\beta(s) = \frac{sRC}{sRC(1 + \sum_{i=1}^{N} \frac{k_i}{k_z}) + \sum_{i=1}^{N} k_i} \tag{3.3}$$

Knowing the amplifier transfer function $A_v(s)$, a block diagram representation of equation (3.2) is depicted in Figure 3.3 that can be used as a behavioral model for the active-RC integrators in MATLAB or SIMULINK. The blocks enclosed in dashed lines
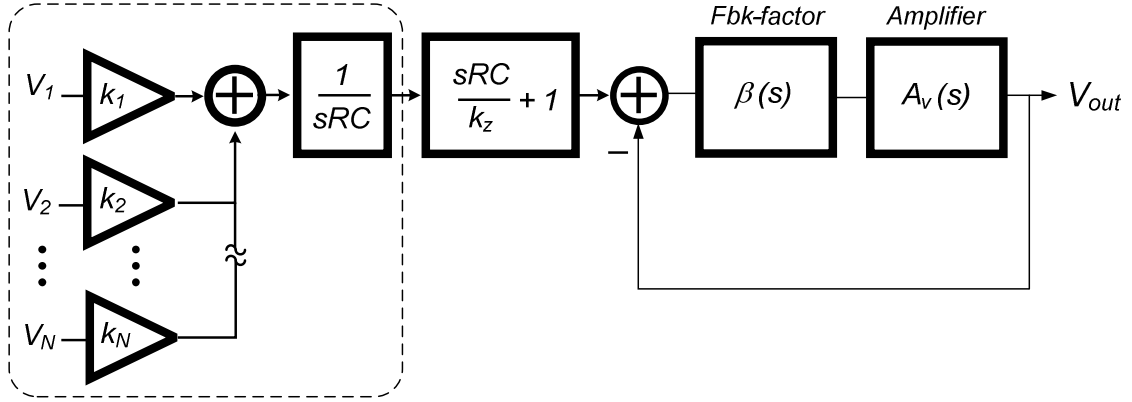
Figure 3.3: Behavioral model of the active-RC integrator.
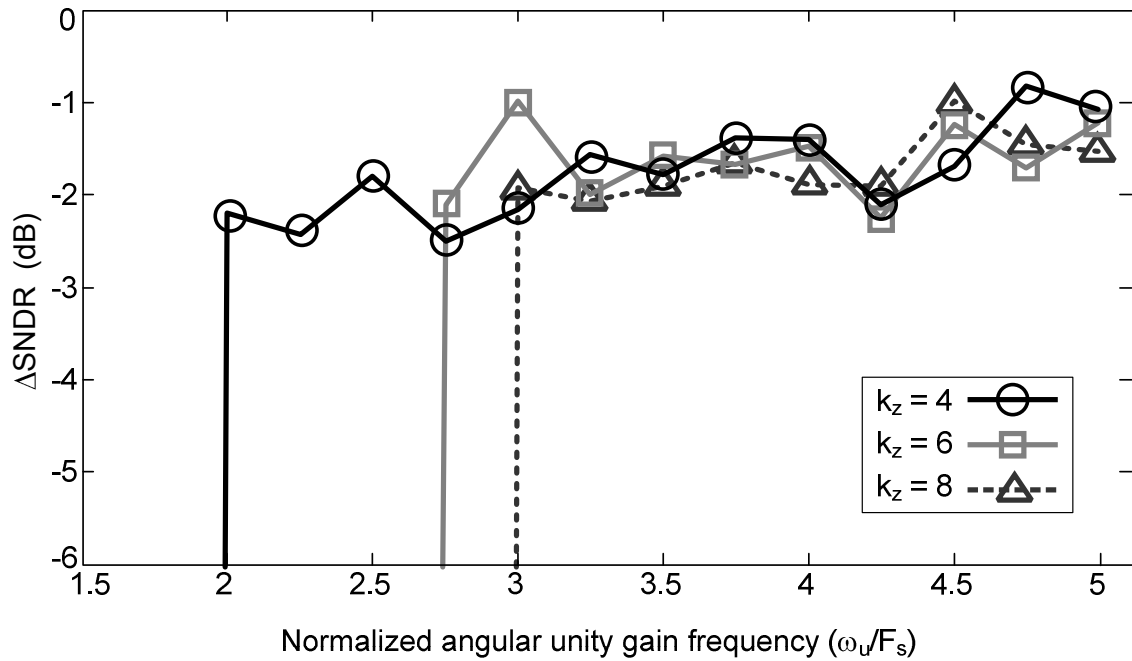
Figure 3.4: Effect of the first-integrator's amplifier UGBW on SNDR of a third-order feedforward ΔΣ-modulator. Results shown for different k_z 's.

is identical to the block diagram of the ideal integrator shown in Figure 3.2(a) and the rest models the non idealities. Assuming a single-pole model for the amplifier the voltage transfer function can be written as

$$A_v(s) = \frac{1}{s/\omega_u + A_0^{-1}} \tag{3.4}$$

where ω_u is the angular unity-gain frequency of the amplifier and A_0 is the DC gain.

Using this equation in the behavioral model in Figure 3.3 allows for modeling the effect

of amplifier unity gain-bandwidth (UGBW) and DC gain on modulator performance.

For instance, simulation of the SNDR performance versus amplifier UGBW of the first-

integrator is shown in Figure 3.4 for a third-order feedforward $\Delta\Sigma$-modulator. When

$k_z=4$ the ω_u can be as low as $2F_s$. SNDR experiences a sharp drop due to instability for

ω_u below $2F_s$. By increasing k_z the minimum required ω_u will increase but it does not

lead to considerable improvement in SNDR. This simulation clearly shows that the

parameter k_z can be leveraged to improve the stability and performance of a CT-$\Delta\Sigma$

modulator without too much increasing the amplifier UGBW.

3.2 Amplifier Input Stage Nonlinearity

The integrator model shown in Figure 3.3 is slightly modified to isolate the

amplifier virtual ground node by re-ordering the $A_v(s)\beta(s)$ term, as shown in Figure 3.5.

Gaining access to the node V_x makes it possible to model the non-linear behavior of the

amplifier input stage. The input stage non-linearity stems from the square-law Current-

Voltage equation of the MOS transistors. Figure 3.6(a) shows a differential pair with tail

bias current I_B which is typically used in the amplifier input-stage. Considering a fully

differential design with no mismatch or offset and assuming that all transistors are in

saturation and are biased in strong inversion, the differential output current can be

written as [27]

$$i_{out-diff.} = \frac{v_d I_B}{V_{GS}-V_T}\sqrt{1-\frac{1}{4}\left(\frac{v_d}{V_{GS}-V_T}\right)^2} \approx I_B\left(\frac{v_d}{V_{GS}-V_T}-\frac{v_d^3}{8(V_{GS}-V_T)^3}\right) \quad (3.5)$$
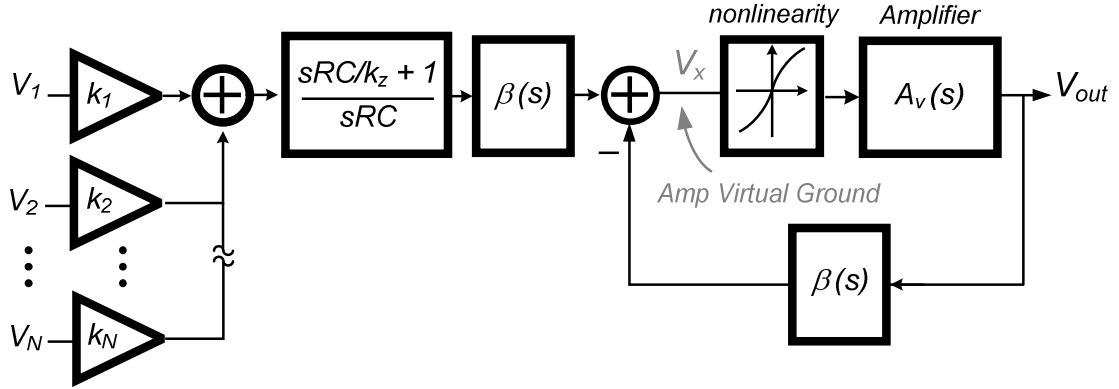
Figure 3.5: Behavioral model for modeling the input stage nonlinearity.

Equation (3.5) assumes weak nonlinearity conditions meaning that distortion is dominated by the third harmonic and the higher order nonlinearities are ignored. The general nonlinear equation can be written as

$$i_{out} = g_1 v_d + g_3 v_d^3 + ... \tag{3.6}$$

By comparing (3.5) and (3.6) the g_1 and g_3 terms are identified as

$$\begin{cases} g_1 = \dfrac{I_B}{(V_{GS} - V_T)} \\ g_3 = \dfrac{-I_B}{8(V_{GS} - V_T)^3} \end{cases} \tag{3.7}$$

Assuming a sine wave input and using (3.6) and (3.7) the third-order harmonic distortion becomes

$$HD3 = \frac{1}{4} \frac{g_3}{g_1} = \frac{1}{32} \left(\frac{v_d}{V_{GS} - V_T} \right)^2 \tag{3.8}$$

Assuming weak nonlinearity conditions and ignoring the high order distortion terms. The above equation provides a first-order estimation of the total harmonic distortion.

A major limitation of the HD3 given by (3.8) is the assumption of quadratic I-V characteristic for the MOS transistors. However in a deep submicron CMOS process,
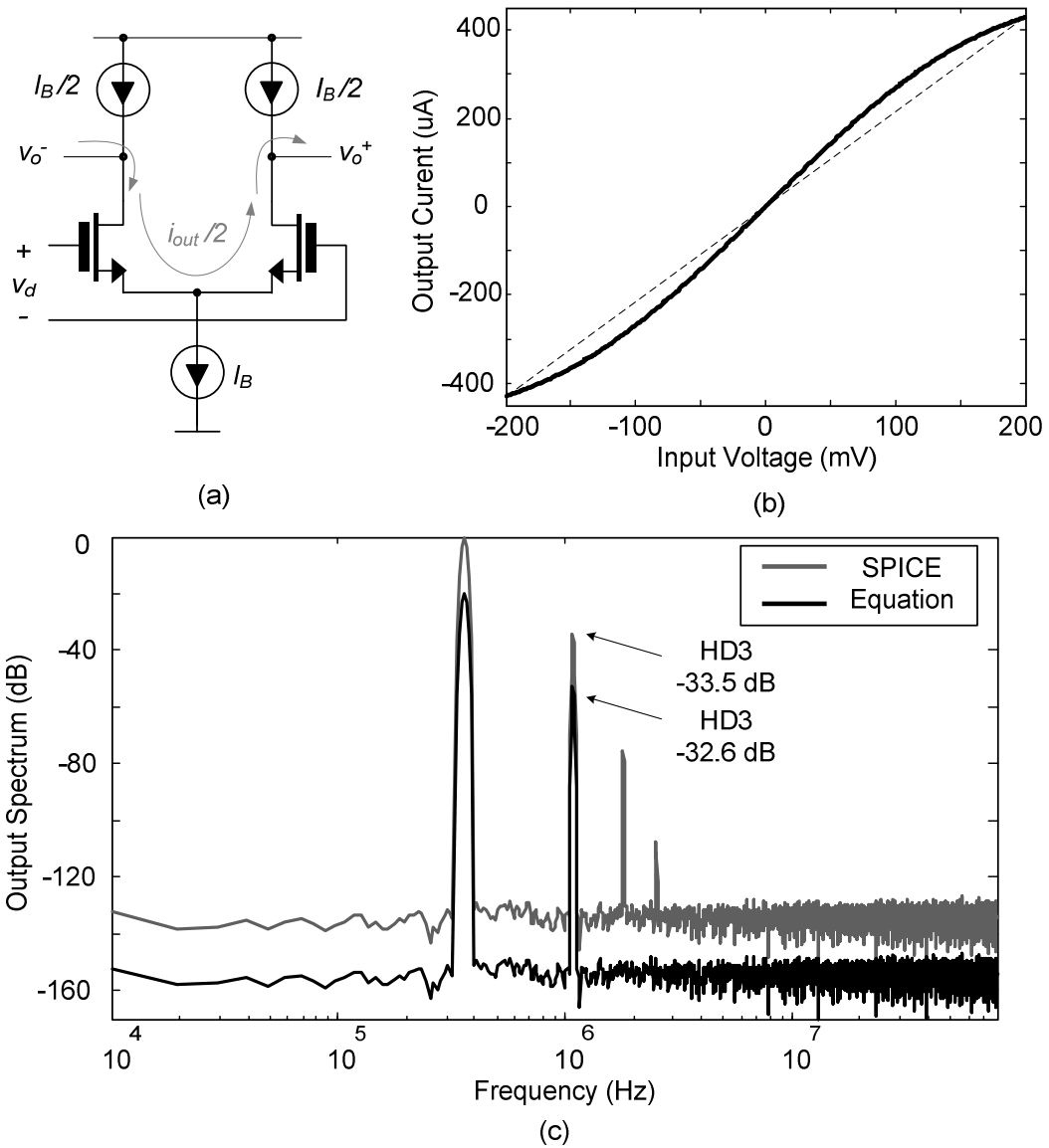
Figure 3.6: (a) A typical input stage differential pair. (b) Simulated V/I transfer curve of the diff. pair using SPICE. (c) Distortion of the output current, SPICE vs. equation.

the quadratic equation does not hold. In this case the designer can use SPICE to generate a table of output current versus input voltage at the bias point of interest I_B. The table can then be ported into MATLAB to compute the linear and nonlinear coefficients using curve fitting. This method provides better correlation between behavioral and circuit level simulations and can predict the total-harmonic-distortion

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Table 3.1: Linear and non-linear coefficients of the input stage G_m.

$i_{out} = g_1 v_d + g_3 v_d{}^3 + g_5 v_d{}^5 + g_7 v_d{}^7 + g_9 v_d{}^9$					
coefficient	g_1	g_3	g_5	g_7	g_9
value	0.0029	-0.0224	0.0584	0.8979	-6.3806

(THD) with better accuracy. Figure 3.6(b) shows the trans-conductance of a PMOS differential pair in a 130nm CMOS process obtained using SPICE simulation. The V_{GS}-V_T of the input transistor was 120mV and the quiescent tail current was 480 uA. The results of a 9th order polynomial curve fitting on the data points of Figure 3.6(b) are provided in Table 3.1. It is noted that all even-order coefficients are zero owing to the differential nature of the circuit.

Figure 3.6(c) shows a comparison between the simulated output spectrums of a differential pair using curve fitting approach versus the approximate computation by equation (3.8). The input signal is the sum of a 100 mV-peak sinewave at 350 KHz and white noise 100 dB below the 100mV full-scale. The equation-based spectrum is intestinally shifted down by 20dB for better visibility. There is a good correlation between the HD3 obtained from curve-fitting on SPICE data and the HD3 estimated by (3.8) although the curve fitting approach is able to predict higher order distortion terms.

Using (3.6) for describing the nonlinear block of the integrator model in Figure 3.5 allows for quick evaluation of the amplifier input-stage nonlinearity in MATLAB. This practice is essential when designing the input differential pair for a given THD target and helps to reduce the power consumption by avoiding the overdesign of the tail bias current.

3.3 Feedback DAC Element Mismatch

A popular topology for implementing feedback DACs in delta-sigma modulators is shown in Figure 3.7. It is based on $M = 2^N$ equally-weighted elements in parallel where the elements are controlled by the received N-bit binary input which gets converted to a 2^N bit unitary scrambled data by a binary-to-thermometer decoder and element selection logic blocks. Also the unitary code can be directly produced by a flash quantizer, which will obviate the need for a binary-to-thermometer decoder. The element selection logic may be used for linearity enhancement purposes by modifying the thermometer code before reaching the DAC. In any case the data received by the M unit-element DAC will be a vector V defined by the following equation

$$\mathbf{V}_{1 \times M}(k) = [\![...v_j...]\!]_{1 \times M} = \left[\!\left[\underbrace{1 \quad ... \quad 1}_{k} \quad \underbrace{-1 \quad \cdots \quad -1}_{M-k} \right]\!\right] \tag{3.9}$$

$$v_j \in \left\{ v_{j \leq k} = 1, v_{j > k} = -1 \right\}$$

The value of each element in **V** is either 1 or -1. A +1 means adding the corresponding element value to and -1 means subtracting it from the output. This definition assumes that the DAC has a fully-differential circuit structure. Unit elements can be made of capacitors, resistors or current-sources depending on the circuit topology. In a real world DAC there will be random mismatch between the actual and nominal (ideal) values of each element. Assuming a normalized value of 1 for each element, the mismatch error can be represented by an $M \times 1$ random vector with Gaussian distribution having a zero mean and standard deviation of σ_{unit}. The MATLAB Statistics Toolbox [28] can be used to generate and store the mismatch vector **W** as

$$\mathbf{W}_{M \times 1} = \text{random}(\, 'normal' \, , 0 \, , \sigma_{\text{unit}} \, , M \, , 1 \,) = \left[\!\left[w_1 \quad ... \quad w_M \right]\!\right]^T \tag{3.10}$$
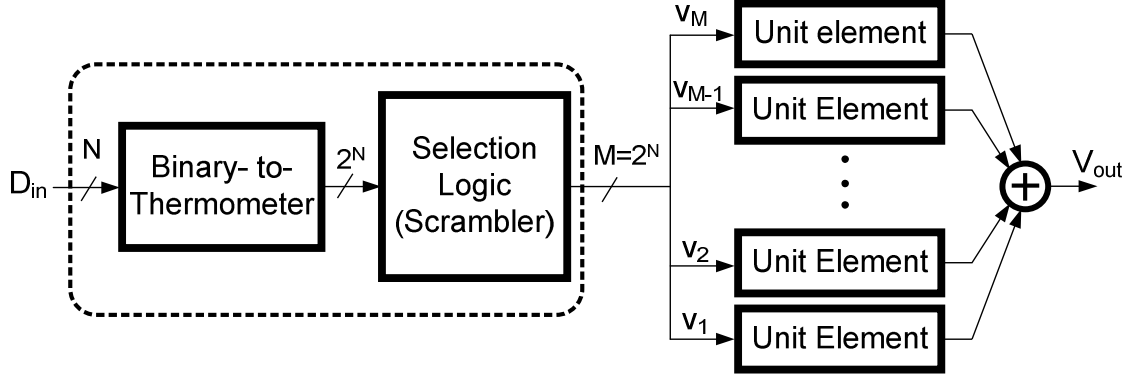
Figure 3.7: A generic unitary DAC structure including the element selection logic.

The output voltage corresponding to the input with decimal value *k* is computed using

$$v_{out}(k) = \frac{VFS}{M}\mathbf{V} \cdot (1 + \mathbf{W}) = \frac{VFS}{M}\left[\underbrace{1 \quad ... \quad 1}_{k} \quad \underbrace{-1 \quad \cdots \quad -1}_{M-k}\right] \cdot \begin{bmatrix} 1 + w_1 \\ \vdots \\ 1 + w_M \end{bmatrix} \quad (3.11)$$

In the above equation *M* is the number of elements, *VFS* is the peak output voltage, w_j is the error in the *j-th* element and **V** is the element selection vector corresponding to input *k*, where $0 \leq k \leq M$. Equation (3.11) can be used for modeling the effect of DAC element mismatch in $\Delta\Sigma$ modulators. In the absence of an effective dynamic element matching scheme, the random mismatch among the units of the main DAC, can distort the $\Delta\Sigma$ modulator output. For example Figure 3.8 shows the output spectrum of a third-order $\Delta\Sigma$ modulator using a 4-bit DAC in the feedback path with 0.1% random mismatch among its 16 unit-elements. The input signal is a -3 dBFS sinewave at 750 KHz while the modulator bandwidth is 5 MHz. The output spectrum shows a 3rd-order harmonic distortion at -78.5 dBFS and the THD is -78 dB. The theoretical standard
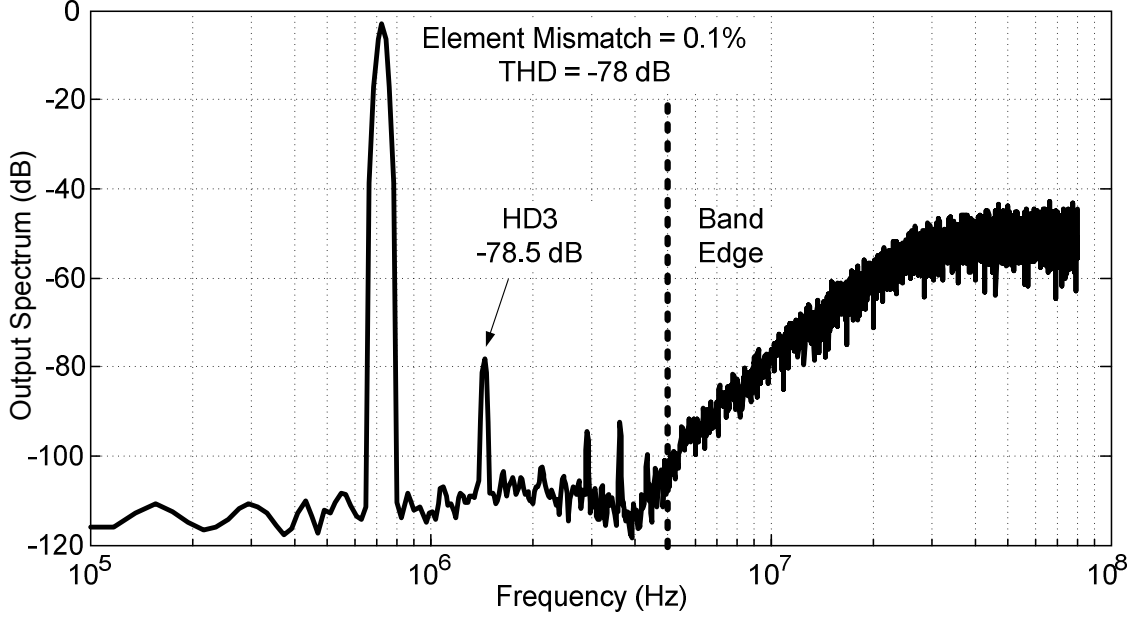
Figure 3.8: Behavioral simulation of DAC element mismatch ($\sigma = 0.1\%$)

deviation of the worst-case error in an *M*-element DAC with unit mismatch σ_{unit} has been derived in the literature [29] as

$$\sigma\left(\frac{\Delta Vo}{VFS}\right)_{worst} = \frac{1}{2\sqrt{M}}\sigma_{unit} \tag{3.12}$$

For M=16 and $\sigma_{unit} = 0.1\%$, the above equation predicts -78 dBFS noise power which is in accordance with the THD number obtained from the behavioral simulation.

3.4 Data Weighed Averaging

Data Weighted Averaging (DWA) is an effective dynamic element matching (DEM) technique which is employed in this work for improving the linearity of the multibit DACs. The DWA algorithm [13] scrambles the received thermometer code in a way that all elements of the DAC are selected an equal number of times over a long run. Figure 3.9 (a) shows the operation of the technique using a 4-bit, 15-unit DAC example.
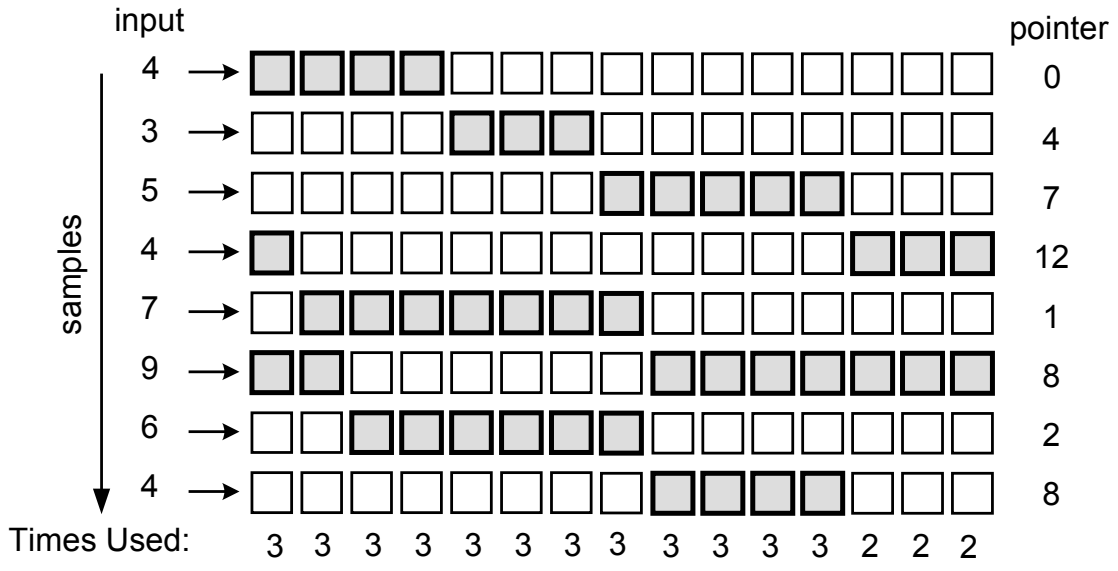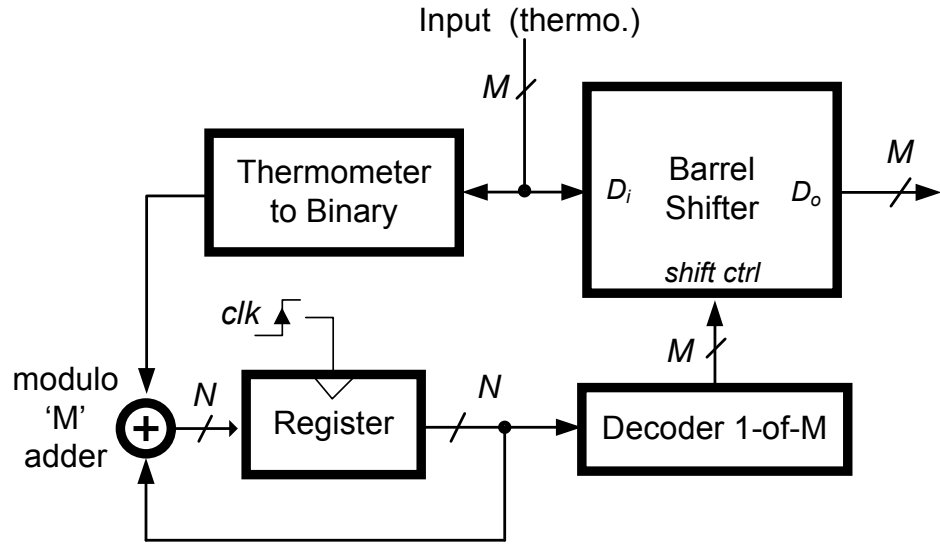
Figure 3.9: (a) DWA operation in a 4-bit DAC. (b) Hardware implementation.

The numbers on the left represent the stream of the incoming data and the numbers at the bottom indicate the number of times that each element is used. Each time k elements are selected starting from element $p+1$ to $p+k$ where k is the input data and $p < M$ is a memory-stored pointer. To be used during the next cycle, the pointer gets incremented

by k to its new value $p+k$ using a modulo 'M' adder to enforce the condition $p < M$. A hardware implementation of the algorithm is depicted in Figure 3.9(b) which includes a barrel shifter (parallel shifter), a 1-of-M decoder, an N bit register, a modulo 'M' adder and a thermometer to binary encoder. At the beginning of each cycle the pointer value is updated as

$$p[n] = \mod(p[n-1] + k[n-1], M) \tag{3.13}$$

where $mod(*, M)$ is the modulo 'M' operation and $k[n-1]$ and $p[n-1]$ are the previous values of the input data and the shit pointer respectively.

The input vector $\mathbf{V}$ to an M-element DAC using DWA algorithm is defined as

$$
\begin{aligned}
\mathbf{V}_{DWA}(k) &= \left[\!\left[...v_j... \right]\!\right]_{1 \times M} \\
v_j &= \begin{cases} +1 & ; \quad p[n] < j \leq \min(p[n] + k[n], M) \\ +1 & ; \quad (1 \leq j \leq \mod(p[n] + k[n], M)) \,\&\, (p[n] + k[n] > M) \\ -1 & ; \quad \text{else} \end{cases}
\end{aligned} \tag{3.14}
$$

where $k[n]$ and $p[n]$ are the current values of the incoming data and the shift pointer, respectively. From a behavioral modeling perspective, the difference between DACs with and without DWA lies in the definition of vector V, as it is evident from the comparison of equations (3.9) and (3.14). Once vector V is defined, the output voltage is produced the same way as a normal DAC (i.e. without DWA) by using equation (3.11). Hence

$$v_{out}(k)|_{DWA} = \frac{VFS}{M} \mathbf{V}_{DWA} \cdot (1 + \mathbf{W}) \tag{3.15}$$

where the mismatch vector $\mathbf{W}$ is given by (3.10).
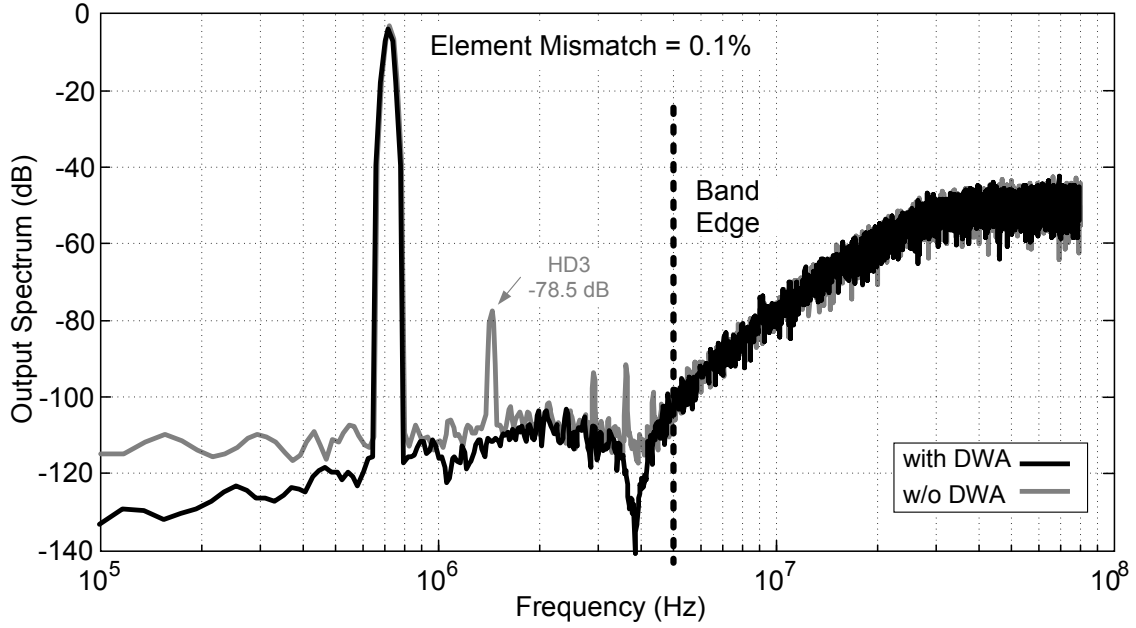
Figure 3.10: Output spectrums with and w/o DWA obtained by behavioral modeling.

A comparison of the ΔΣ-modulator output spectrum with and without DWA is shown in Figure 3.10. The modulator employs 4-bit, 15-element DAC with 0.1% unit element mismatch ($\sigma = 0.001$). The THD of the modulator when DWA is turned off is limited by a strong third-harmonic at -78.5 dB which limits the SNDR performance to 78 dB. However after enabling DWA, the harmonic components drop below noise floor and SNDR performance improves to 87 dB. In this simulation the DAC with DWA was modeled using equations (3.10), (3.13), (3.14) and (3.15), and the one without DWA was modeled using (3.9), (3.10) and (3.11).

3.5 Flash Quantizer

An N-bit flash quantizer is composed of M comparators and M reference levels produced by a resistor string as shown in Figure 3.11(a). Each comparator detects the sign of V_{in}-V_j-ΔV_j, where V_j and ΔV_j are the ideal reference level and the offset error of the j-th comparator respectively. Also depending on the number of comparators, the transfer characteristics of a Flash quantizer can be made mid-rise or mid-tread, as shown in figures 3.11(b) and (c) respectively. The reference levels of mid-rise and mid-tread flash are defined as

$$\mathbf{V}_{M\times 1} = \begin{bmatrix} V_1 & ... & V_M \end{bmatrix}^T$$

$$V_j = \begin{cases} j2^{-N+1} - 1 & ; \quad 1 \leq j \leq 2^N - 1 \quad : \text{mid-rise} \\ j2^{-N+1} - 1 - 2^{-N} & ; \quad 1 \leq j \leq 2^N \qquad : \text{mid-tread} \end{cases} \qquad (3.16)$$

The above equation assumes a normalized full-scale range of +/- 1V for the quantizer. It is also noted that the number of comparators M is 2^N-1 and 2^N in mid-rise and mid-tread cases, respectively. Although the mid-tread flash costs one more comparator to implement, it is preferred over the mid-rise due to its zero gain around the mid-scale and adding one more quantization level.

Assuming negligible mismatch and random errors in the resistor string, the quantizer trip points will be mainly affected by the random offset of the comparators. The comparator offset can be modeled by a set of M random numbers with Gaussian distribution and zero mean. The numbers can be generated using the *'random'* function of the MATLAB Statistics toolbox as

$$\Delta\mathbf{V}_{M\times 1} = \text{random}(\,\text{'normal'}\,,\, 0\,,\, \sigma_{\text{offset}}\,,\, M\,,\, 1\,) = \begin{bmatrix} \Delta V_1 & ... & \Delta V_M \end{bmatrix}^T \quad (3.17)$$
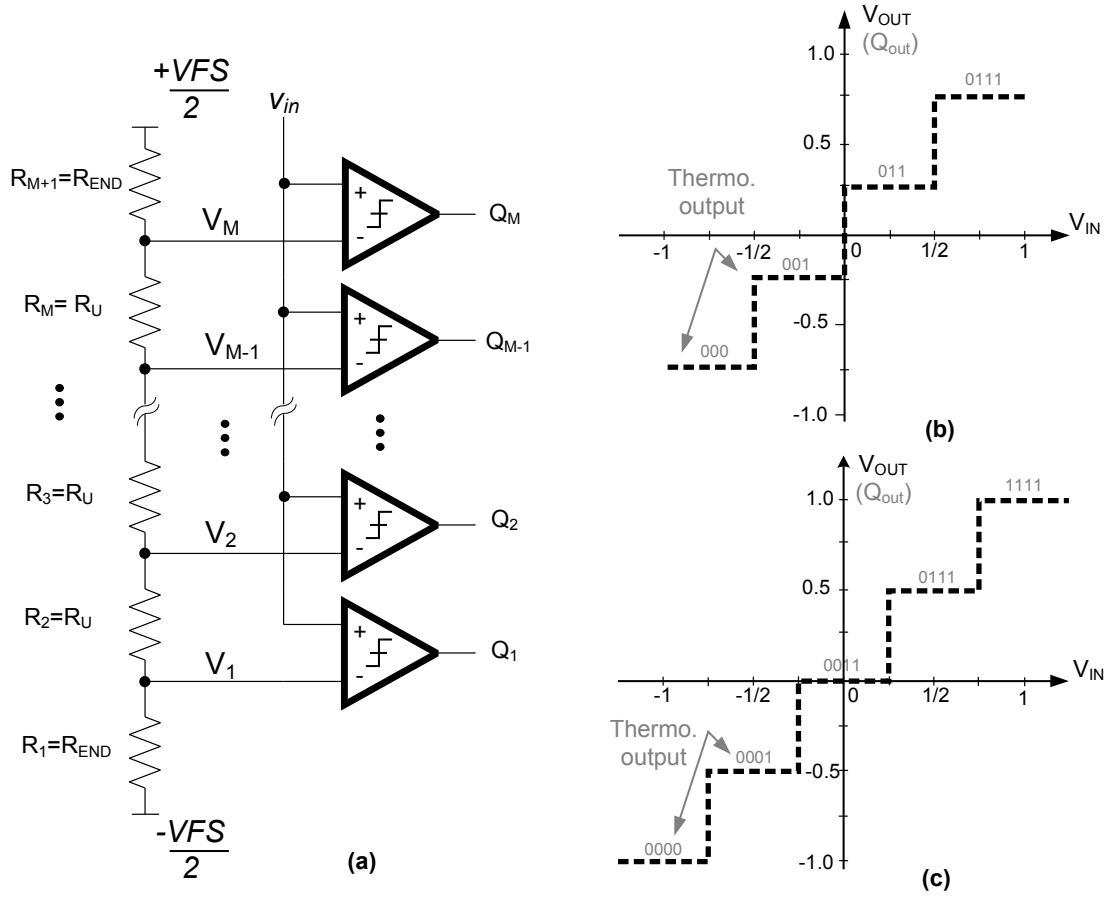
Figure 3.11: (a) Flash quantizer architecture. (b) Mid-rise and (c) Mid-tread transfer characteristics.

In the above equation, σ_{offset} is the standard deviation of comparator's input-referred offset normalized to the 2 V full-scale range (i.e. $\pm$ *VFS/2* $= \pm$ 1 V). The output of the Flash quantizer is an M×1 vector $\boldsymbol{Q}$ computed as

$$\mathbf{Q}_{M\times1}[nT_s] = \begin{bmatrix} Q_1 & \cdots & Q_M \end{bmatrix}^T_{Q_j\in\{1,-1\}} = \text{sign}\left(v_{in}[nT_s] - \mathbf{V}_{M\times1} - \Delta\mathbf{V}_{M\times1}\right) \quad (3.18)$$

The *'sign'* in (3.18) is the zero crossing function with two possible values of +1 or -1 depending on the sign of its argument, while zero is treated as a negative number. Also $v_{in}[nT_s]$ denotes the input voltage at the *n-th* sampling instance.
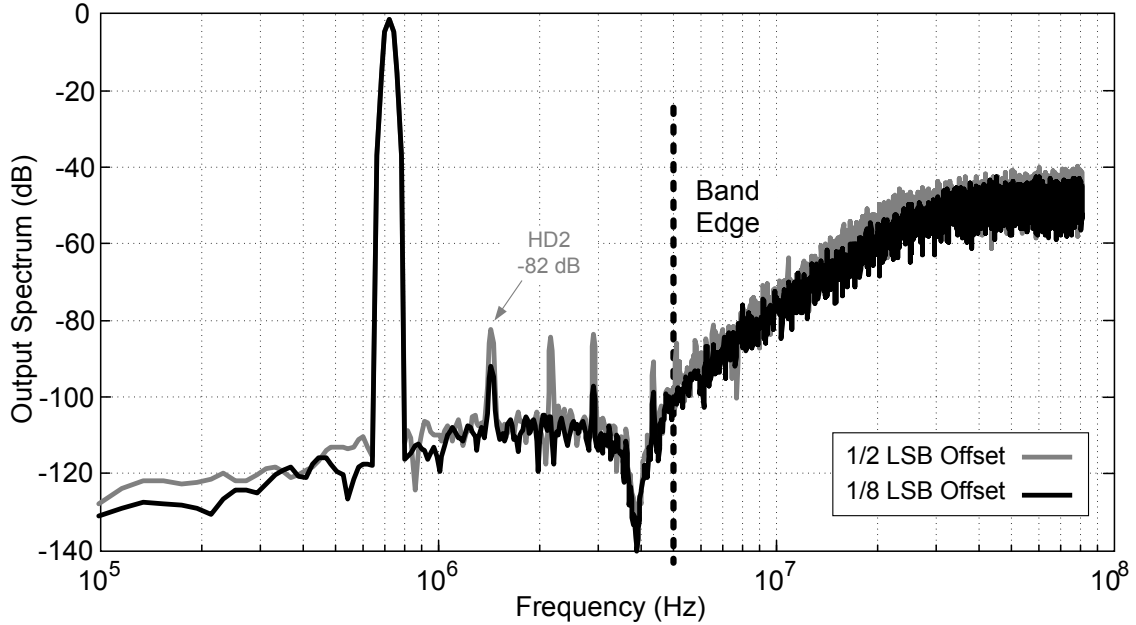
Figure 3.12: Effect of comparator offset in a 3rd-order $\Delta\Sigma$ with 4-bit flash quantizer.

The behavioral model of the flash quantizer is formed around equations (3.16), (3.17) and (3.18) which allow a fast simulation of comparator random offset. As an example we have simulated the effect of 1/2 LSB and 1/8 LSB offset in a third-order $\Delta\Sigma$ modulator using a 4-bit flash quantizer. Figure 3.12 shows a comparison of modulator output spectrum for the two offset standard deviations. The SNDR is 76 dB and 85 dB respectively for 1/2 LSB and 1/8 LSB offset cases, while the ideal case SNDR is 87 dB. In the half-LSB offset case the dominant distortion term is an HD2 at -82 dB. Clearly the flash quantizer is capable of generating strong even harmonics that can severely degrade the THD performance. The even harmonic distortion is attributed to the asymmetrical transfer characteristics of the flash quantizer around its mid-scale which occurs irrespective of the modulator circuit being fully-differential or single-ended.
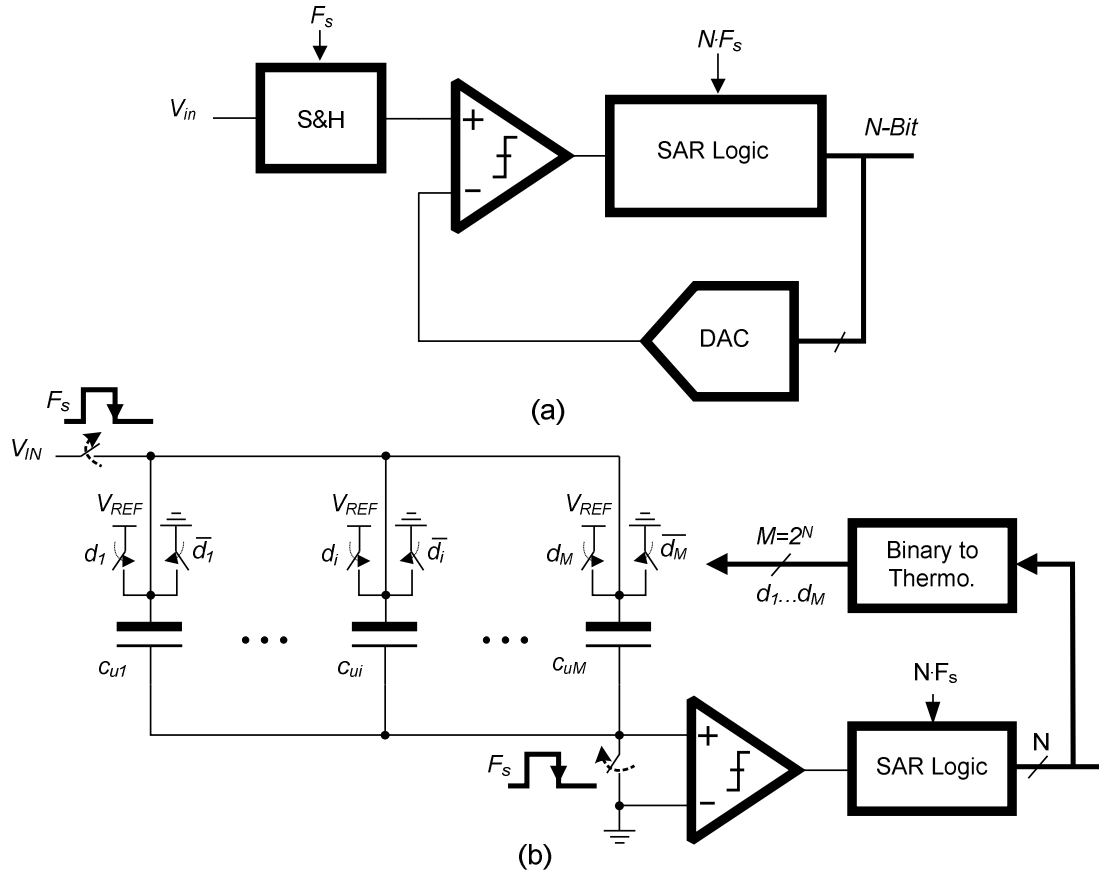
Figure 3.13: (a) General structure of a SAR quantizer. (b) A switched capacitor SAR.

3.6 Successive Approximation Quantizer

The conceptual block diagram of a successive approximation (SAR) quantizer is shown in Figure 3.13(a). An N-bit SAR includes an input sampler, a single comparator, an N-bit feedback DAC and SAR register. A circuit-level implementation using switched-capacitors technique is shown in Figure 3.13(b). This circuit merges the input sample-and-hold and the charge-redistribution SAR DAC into one block. The switched-capacitors DAC is made of 2^N unit capacitors and is controlled by the SAR register. The offset of the comparator causes a DC shift in the quantizer response which does not affect the linearity. However the nonlinearity of the SAR DAC, due to mismatch among

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its unit elements, directly affects the transfer characteristics of the quantizer and is the major cause of signal distortion. Just like the main feedback DAC, the mismatch of a SAR DAC can also be expressed by an M×1 error vector W using (3.10), where $M=2^N$ and N is the quantizer resolution. The actual capacitor array, including mismatch errors, can be represented by an M×1 vector C as

$$\mathbf{C}_{M \times 1} = c_u(1 + \mathbf{W}_{M \times 1}) = c_u \begin{bmatrix} 1 + W_1 & \cdots & 1 + W_M \end{bmatrix}^T \tag{3.19}$$

The SAR quantizer resolves N bits sequentially during N conversion phases. At each phase the SAR register recursively updates the SAR DAC analog output according to its output code $k[n]$ where

$$\begin{cases} k[n] = 2^{N-1} & , \quad n = 1 \\ \\ k[n] = 2^{N-n} + \sum_{j=1}^{n-1} b[j]2^{N-j} & , \quad 2 \leq n \leq N \end{cases} \tag{3.20}$$

In the above equation $b[j]$'s are the bits detected by the comparator prior to the current phase n. The bits are detected by starting from MSB=b_1 at the first phase, and finishing by LSB=b_N at the last. The detection sequence can be expressed by the following recursive equation

$$b[n]_{\in\{0,1\}} = \mathrm{H}[V_{in} + V_{offset} - \frac{V_{ref}}{2^N C_u}(\sum_{i=1}^{k[n]} C_i - \sum_{j=k[n]+1}^{2^N} C_j)] \tag{3.21}$$

In the above, $H[\cdot]$ is the discrete unit step function (i.e. $H[x>0]=1$ and $H[x\leq0]=0$), V_{in} is the sampled input, V_{offset} is the comparator's input-referred offset, $V_{ref}=VFS/2$ is the quantizer reference voltage, C_u is the ideal unit capacitor, and C_i and C_j's are the actual capacitor values from (3.19) which include mismatch. According to (3.21) $b[n]$ depends
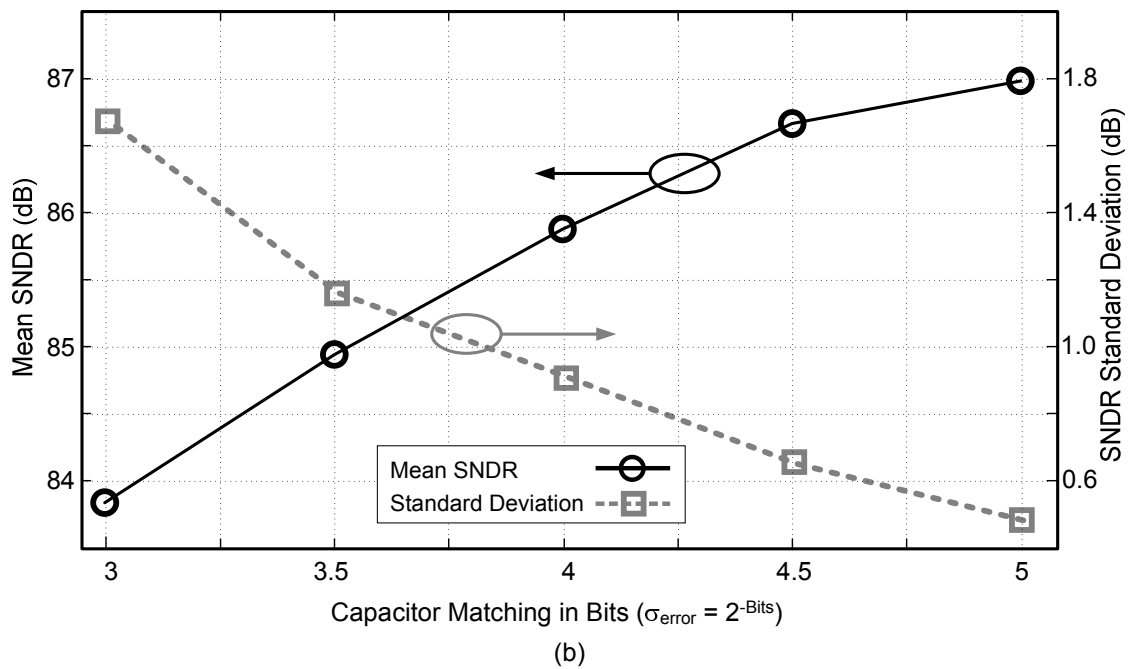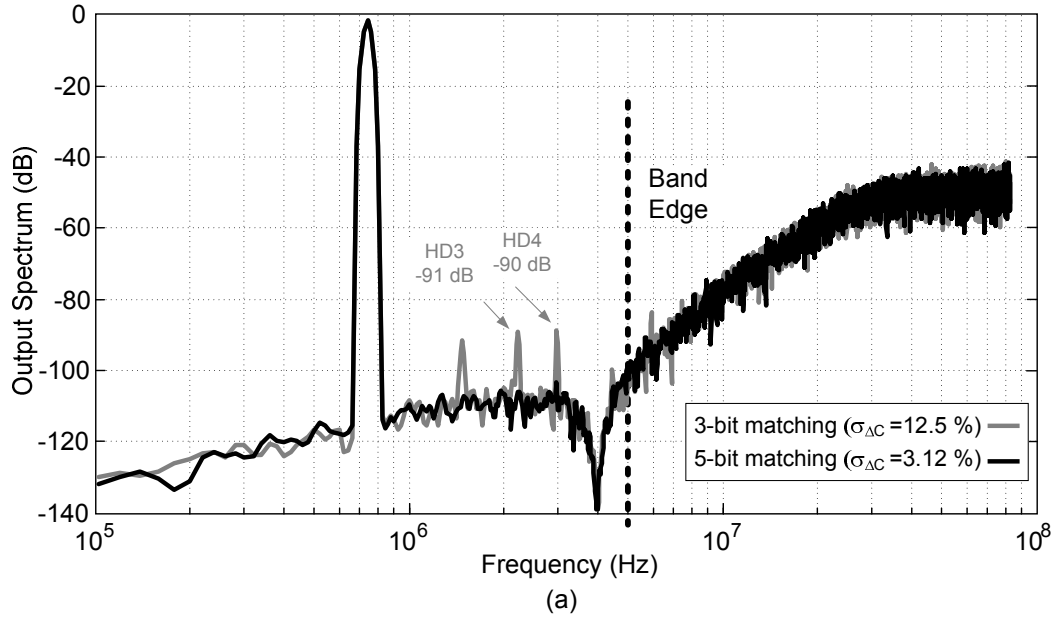
Figure 3.14: Behavioral modeling of a 4-bit SAR in a 3rd-order $\Delta\Sigma$ modulator. (a) Comparison of output spectrums. (b) Performance statistics versus matching.

on $k[n]$ which in turn depends on all previously detected $b[j]$'s ($j \le n\text{-}1$) according to (3.20). At the end of the *N-th* phase the SAR quantizer produces an output code with the following decimal value

$$D_{out} = \sum_{j=1}^{N} b[j]2^{N-j} \qquad (3.22)$$

A behavioral model for the SAR quantizer can be formed using equations (3.10), and (3.19) to (3.22). As an example, a third-order $\Delta\Sigma$ modulator with 4-bit SAR quantizer is simulated for two different capacitor matching levels of 3-bit (i.e. $\sigma_{unit}=2^{-3}$) and 5-bit ($\sigma_{unit}=2^{-5}$). Figure 3.14(a) shows modulator output spectrum versus capacitor matching. The SNDR is 82.5 dB and 86.9 dB for the 3-bit and 5-bit matching respectively while the no mismatch SNDR is 87 dB. Figure 3.14(b) shows the results of a more comprehensive simulation which looks at the statistics of the SNDR performance versus SAR capacitor matching. Each point represents the mean and standard deviation of 100 runs. As expected the average SNDR drops by decreasing the matching levels, whereas the standard deviation of SNDR increases. In other words, the expected minimum SNDR (3σ minimum) decreases at a faster rate when lowering the matching levels.

It is worth noting that the presented SAR modeling considers only the static errors related to element mismatch and aims providing guidelines for component sizing and yield analysis. However, it does not take into account dynamic errors like limited bandwidth and meta-stability of the comparator, or charge injection of the switches. To evaluate the latter error mechanisms we will still rely on SPICE simulations.
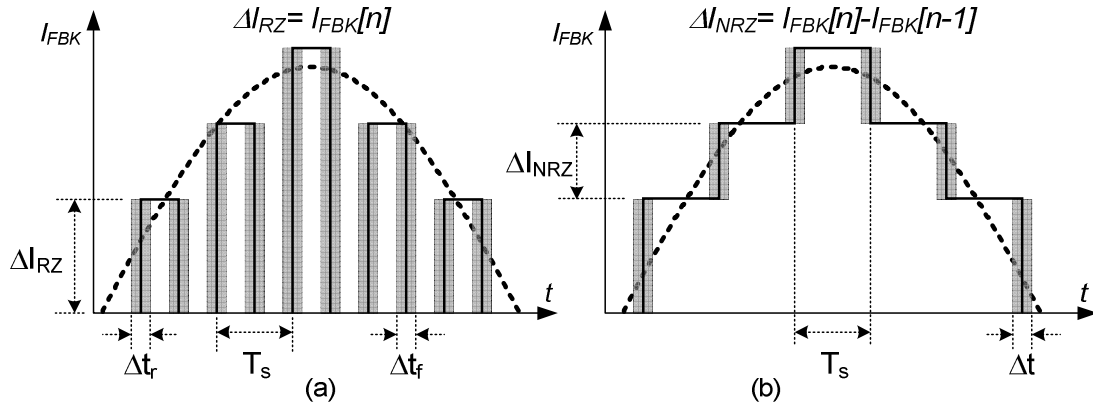
Figure 3.15: Jitter in the feedback DAC (a) RZ waveform; (b) NRZ waveform.

3.7 Clock Jitter

Timing errors in the feedback waveform of a CT-$\Delta\Sigma$ modulator, caused by clock jitter, can result in random fluctuations of the charge stored in the integration capacitors. The net effect of this error is analogous to injecting noise to the modulator input which results in SNR and dynamic range reduction. The effect of clock jitter in CT-$\Delta\Sigma$ modulators has been extensively analyzed in the literature [30-33], where earlier publications [30-31] unanimously concluded the random variation of the feedback pulse width is the major source of the jitter noise. The work in [33] showed that the jitter-induced noise in modulators with NRZ feedback is predominantly determined by the out-of-band behavior of the NTF, thus more aggressive noise shaping automatically exacerbates the jitter sensitivity. In addition to the NTF contribution, a more recent analysis [34] attributed part of the jitter noise to the input signal parameters.

To gain an intuitive understanding of the jitter noise, consider a feedback DAC with current mode output I_{FBK} using RZ and NRZ waveforms as shown in Figure 3.15(a) and (b) respectively. Every cycle the DAC transfers a net charge to the integrat-

ing capacitor which ideally is equal to the area under the feedback waveform, or

$$Q[n] = I_{FBK}[n] \cdot T_s \qquad (3.23)$$

However, in presence of jitter, the transferred charge will deviate from its ideal value by

$$\Delta Q[n] \cong \begin{cases} (I_{FBK}[n] - I_{FBK}[n-1]) \cdot \Delta t[n]; & \text{NRZ DAC} \\ I_{FBK}[n] \cdot (\Delta t_r[n] + \Delta t_f[n]); & \text{RZ DAC} \end{cases} \qquad (3.24)$$

In the above, $\Delta t[n]$ denotes the NRZ timing error while $\Delta t_r[n]$ and $\Delta t_f[n]$ respectively, are the rising and falling edge timing errors of the RZ pulse. Equation (3.24) directly points to some advantages of using multibit NRZ DACs for jitter noise reduction. These benefits can be summarized as, less switching activity and smaller step size. The timing errors of the NRZ waveform happen only once at every cycle, whereas in the RZ case the jitter affects both edges of the clock, as shown separately by Δt_r and Δt_f in Figure 3.15. On the other hand the step size of the NRZ feedback is the difference between two consecutive outputs which tends to remain small owing to the inherent oversampling of $\Delta\Sigma$ modulators. In contrast the RZ step directly follows the modulator output at every cycle hence according to (3.24) larger error charge will be incurred.

In order to evaluate the effect of jitter in the multibit NRZ $\Delta\Sigma$ modulators, one can use the so called *"jitter error sequence"* [32] which essentially is the error charge in (24) normalized to the sampling period

$$\varepsilon[n] = (y[n] - y[n-1]) \cdot (\frac{\Delta t[n]}{T_s}) \qquad (3.25)$$

In the above, *y[n-1]* and *y[n]* are two consecutive outputs of the modulator and $\Delta t[n]$ is the timing jitter corresponding to a Gaussian random process with zero mean and standard deviation $\sigma_{\Delta t}$. Using (3.25), the in-band noise power due to jitter can be

expressed as

$$S_j = \frac{\sigma^2_{\varepsilon}}{OSR} = \frac{\sigma^2(\Delta t/T_s)}{OSR} E\left\{(y[n] - y[n-1])^2\right\}.$$ (3.26)

In the above $(\Delta t/T_s)$ is the normalized clock jitter and *OSR* is the oversampling ratio. Neglecting the input signal contribution to the output step size *y[n]-y[n-1]*, the in-band jitter noise power is derived as [33]

$$S_j = \frac{\sigma^2(\Delta t/T_s)}{OSR} \cdot \frac{VFS^2}{12\pi(2^N - 1)^2} \int_0^\pi \left|(1 - e^{-j\omega})NTF(e^{-j\omega})\right|^2 d\omega$$ (3.27)

In the above equation *VFS* is the modulator full-scale range and *N* is the quantizer resolution in bits. The term under the integral in (3.27) is the product of the first-order high-pass filter *1-z^{-1}* and modulator's NTF, which suggests that the jitter noise is mainly influenced by the NTF response at high-frequencies. In other words a more aggressive noise-shaping with larger NTF out-of-band gain will be more sensitive to clock jitter due to larger steps at its output. Equation (3.25) suggests a quick way of simulating the effect of clock jitter in CT $\Delta\Sigma$ modulators by simply generating the error term $\varepsilon[n]$ in (3.25) and adding it to the feedback path of the modulator.

Figure 3.16 shows such behavioral model [34] which can be easily implemented in SIMULINK environment of MATLAB. In Figure 3.16 the sequence $\left(\Delta t[n]/T_s\right)$ is a discrete Gaussian random variable with zero mean and standard deviation equal to the normalized jitter. Figure 3.17 shows the output spectrum of a third-order $\Delta\Sigma$ modulator subjected to 1% and 0.1% jitter (normalized to T_s). The total in-band noise power, including the -89 dBFS quantization noise, is -66 dBFS and -84.3 dBFS for 1% and 0.1 % jitter, respectively. From these numbers the jitter-induced noise power is found as

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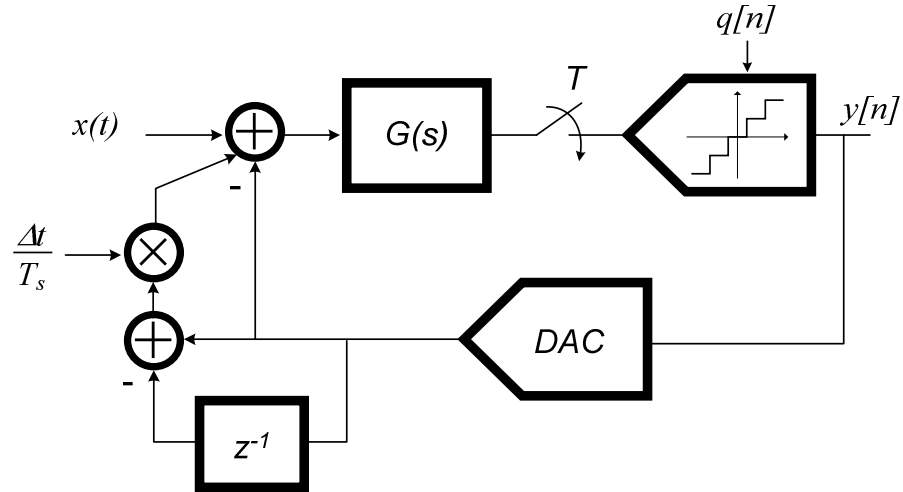
Figure 3.16: A behavioral model for simulating the jitter.
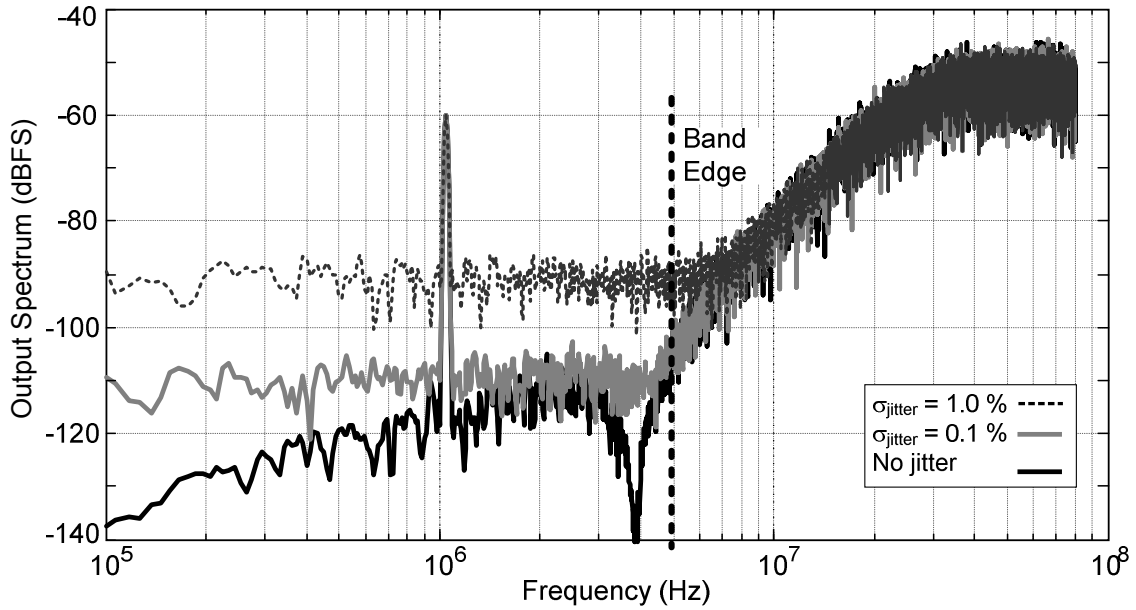
Figure 3.17: Output spectrum of a 3rd-order $\Delta\Sigma$ modulator affected by jitter.

-66 dBFS and -86 dBFS for 1% and 0.1% jitter, respectively.

We compared two commonly used DAC pulses, RZ and NRZ, and mentioned the benefits of using NRZ feedback over RZ from jitter sensitivity perspective. In an alternative method, the NRZ DAC is replaced by a switched-capacitor DAC [14]-[18]. In contrast to the rectangular current pulse of an NRZ DAC, a switched capacitor

produces a current spike that vanishes in a fraction of a sampling period. As a result, the clock jitter has nearly no influence on the amount of transported charge from the switched-capacitor DAC into the integrator. To handle the current spikes produced by the feedback DAC, the bandwidth of the first integrator's amplifier has to be increased to a bandwidth comparable to that of a switched-capacitors $\Delta\Sigma$ modulator. This increases the power consumption of the first integrator.

Another simple and efficient method to relax the clock jitter is to employ a low-pass finite impulse response (FIR) DAC in the feedback path [35]. With an N tap FIR, the quantizer output pulse is spread over N samples and jitter contribution is subsequently averaged over N periods. For an efficient hardware implementation of the analog FIR, the modulator is usually constrained to use single-bit quantization [36-37]. This limitation makes it challenging to implement higher-order and aggressive noise-shaping in FIR based $\Delta\Sigma$ modulators.

3.8 Summary

This chapter presents the behavioral models used to simulate the effect of various non-idealities encountered in CT-$\Delta\Sigma$-modulators, such as, amplifier limited gain-bandwidth product, amplifier input stage nonlinearity, mismatch among the unit elements of the feedback DAC, the comparator offset of a Flash quantizer, element mismatch of a SAR quantizer, and clock jitter. The derived equations and modeling techniques are employed throughout this work in the design and implementation of a 5-bit SAR based CT-$\Delta\Sigma$ modulator a third-order dual-feedback CT-$\Delta\Sigma$ modulator as explained in the following chapters.

CHAPTER 4

SAR BASED CT DELTA-SIGMA ARCHITECTURE

Wireless applications have steadily headed towards higher data rates in recent years while portability has placed a stringent requirement on power consumption. One impact of this trend on receiver design has been the increasing need for low-power wideband A/D converters. Continuous-time Delta-Sigma (CT-$\Delta\Sigma$) modulators have been gaining popularity due to their potential to fulfill these conflicting requirements [1-2]. Owing to the availability of efficient DEM techniques and the ease of implementation of current-mode DACs, single-loop multibit structures have become the architecture of choice in wideband applications [38-45]. Multibit quantization allows for more aggressive noise shaping in higher-order systems and smaller oversampling ratios (OSR). For a given signal bandwidth, a lower OSR translates into a lower clock frequency and thus, results in power savings in both analog and digital blocks. Furthermore, multibit quantization combined with NRZ feedback pulsing significantly relaxes the clock jitter requirement [40-45]. For each additional quantizer bit the feedback step size is halved, which in effect doubles the amount of tolerable jitter. However, each extra bit calls for doubling the number of comparators in a flash quantizer. This causes an exponential growth of power and area. The significance of the quantizer in CT-$\Delta\Sigma$-modulators becomes even more apparent when one takes note of the lower power and area of continuous-time loop filters compared with their switched-capacitor (SC) counterparts. In a CT-$\Delta\Sigma$-modulator, the multibit quantizer makes up a larger portion of the total power and area [46]. Therefore, improving the quantizer can provide for substantial overall improvement in a CT-$\Delta\Sigma$-modulator.

Alternative quantization techniques in $\Delta\Sigma$-modulators have recently started to emerge. The implementation in [47] uses a flash-like tracking A/D with reduced number of comparators and adaptive reference levels. This technique sets severe constraints on the signal bandwidth to make the tracking possible. The SC-modulator in [48] incorporates a two-step flash ADC where quantization time is confined within one half of the clock period.

This chapter will present a CT-$\Delta\Sigma$-modulator architecture based on Successive-Approximations (SAR) quantizer. Also the design and implementation of a first-order modulator based on a 5-bit SAR with delay compensation will be presented. The modulator achieves 62 dB of dynamic-range over the WCDMA bandwidth of 1.92 MHz when clocked at 184.32 MHz. The use of SAR-quantizer stems from the observation that SAR-quantizers are generally quite efficient in terms of power and area. The SAR-quantizer is the only block in the modulator which operates at a higher frequency to achieve a conversion time of less than one sampling period. The quantizer delay is compensated at the system level by including an additional feedback path in the modulator structure. The non-linearity of the feedback digital-to-analog converter (DAC) is reduced using a partial-data-weighted-averaging (P-DWA) technique that takes advantage of the successive approximation algorithm to circumvent the excess loop delay issue caused by the non-zero propagation time of digital blocks. Although the proposed architecture has been implemented as a first-order modulator for proof of concept, it can equally be used in higher-order systems with aggressive noise shaping. The following sections will first provide an overview of the architecture design. Then the implementation details of the first-order 5-bit modulator will be presented.

	Flash	Pipeline	SAR
Power	2^N	>N	1
Speed	1	<1	1/N
PW / Speed	2^N	>N	N
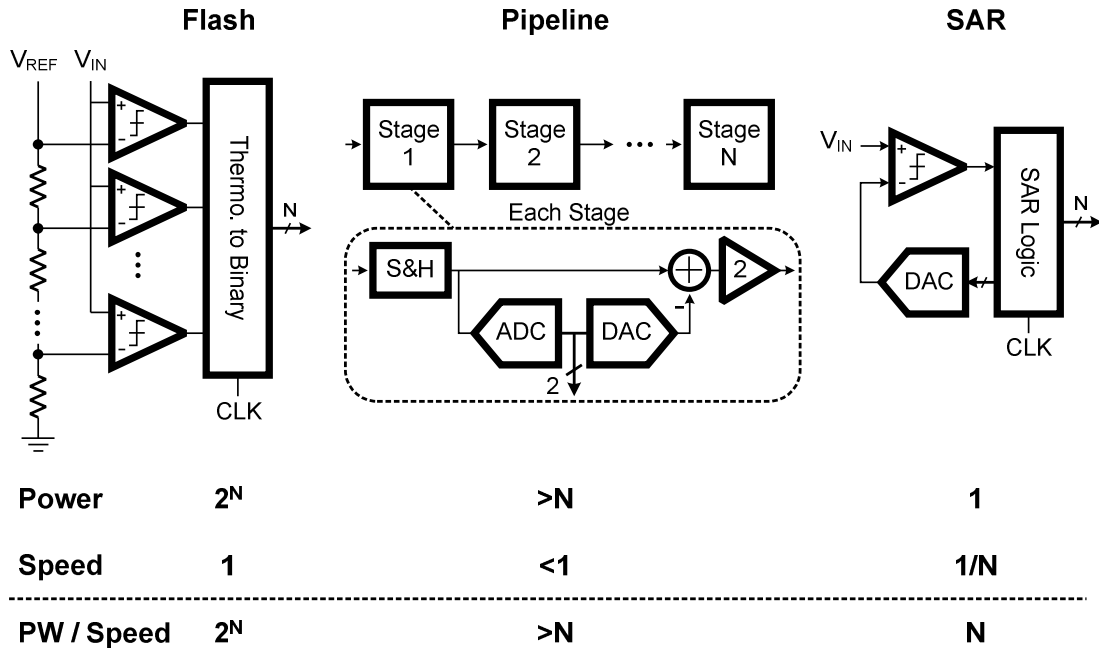
Figure 4.1: Power-speed trade-offs in major A/D converter architectures.

Finally, test and measurement results will be shown.

4.1 Architecture Overview

The comparative study of various ADC architectures in [49] indicates that successive approximation is generally the most energy-efficient A/D conversion technique. In other words, SAR-quantizers provide the lowest power-to-speed ratio among A/D Converters. Figure 4.1 shows power and speed trade-offs for three major A/D architectures. Compared with an N-bit flash quantizer, a SAR-quantizer needs to be clocked N times faster to achieve similar throughput. This results in an N- fold power consumption increase for a single comparator. Assuming that the quantizer power is proportional to the comparator power and the number of comparators, the ratio between
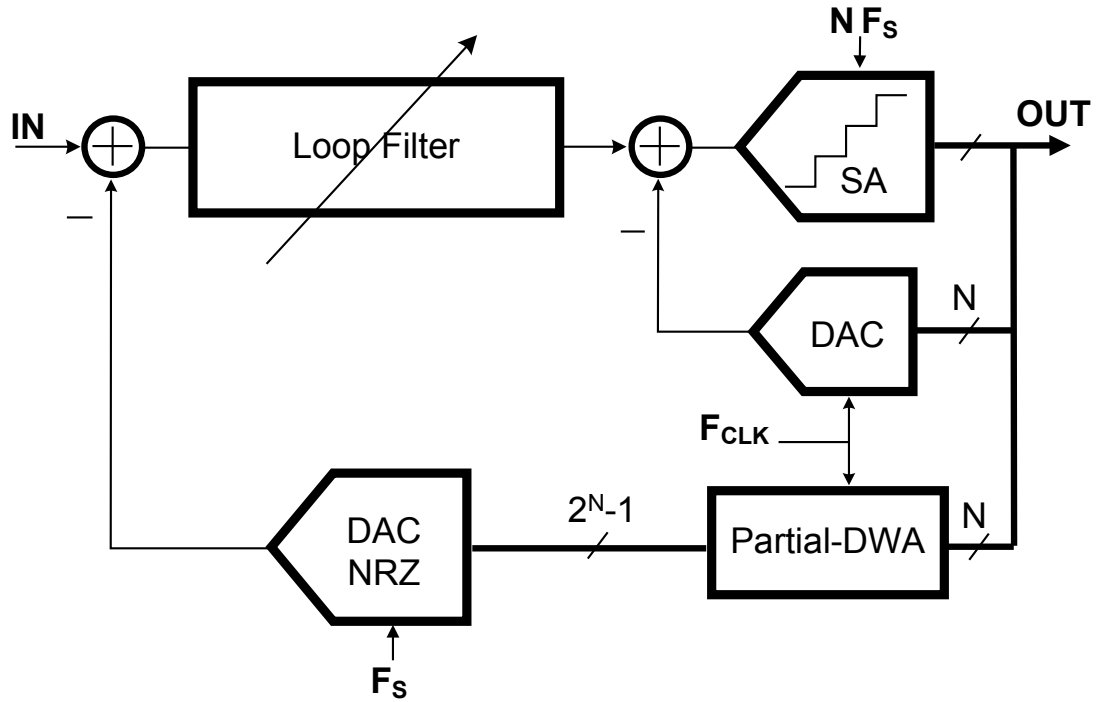
Figure 4.2: Proposed SAR based CT-ΔΣ modulator architecture.

the SAR-quantizer power and the Flash quantizer power will be $N/2^N$. This means that for the same throughput, the SAR-quantizer consumes less power. This ratio becomes more significant as the number of bits increases. The proposed architecture, shown in Figure 4.2, is based on this observation. Since successive approximation A/D conversion causes a delay proportional to the number of bits and the clock frequency, the quantizer needs to be clocked at a higher frequency to keep the conversion time less than one sampling period. This amount of delay can be compensated at the system level by means of an extra DAC which is implemented using the switched-capacitor technique. The main DAC is current-mode and uses the Non-Return-to-Zero (NRZ) pulse scheme for better protection against clock jitter. Partial-DWA is applied only to the main DAC to improve its linearity without causing additional loop delay.
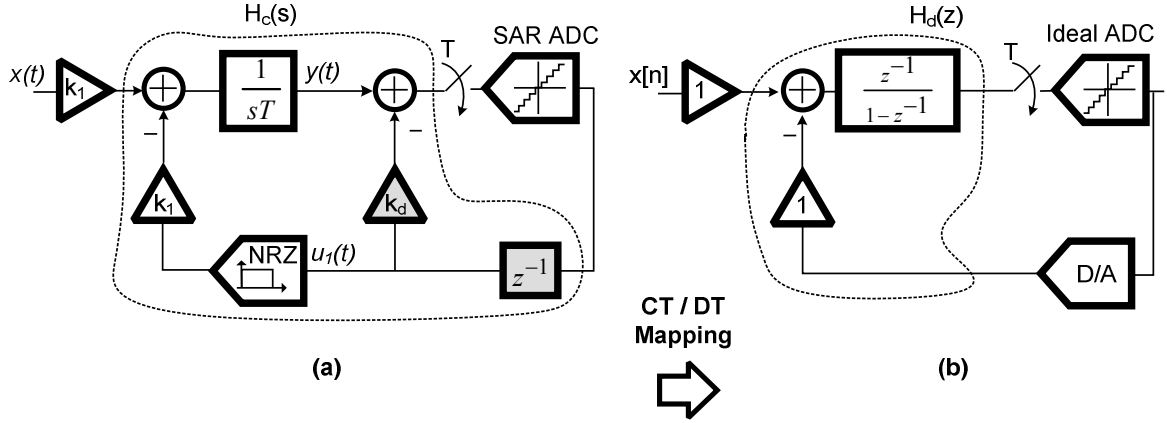
Figure 4.3: (a) First-Order CT prototype ΔΣ modulator with quantizer delay compensation. (b) DT equivalent after discretization.

4.1.1 SAR Latency Compensation

Excess loop delay can cause serious degradation in the performance of CT-ΔΣ-modulators [20]. Flash quantization along with delay compensation is commonly used in CT-ΔΣ modulators to overcome the excess loop delay problem caused by the finite speed of the quantizer [40-45]. An N-bit SAR-quantizer clocked N times faster than the sampling frequency still exhibits a latency of one full sampling period that can be compensated at the system level. The principal approach to delay compensation is to introduce an additional path into the modulator feedback loop [21]. This technique makes it possible to synthesize the desired Noise-Transfer-Function (NTF) when the total loop delay remains within one sampling period. In the case of the first-order system in Figure 4.3(a), the loop transfer function of the system can be written as:

$$H(s) = \left(\frac{k_1}{sT} + k_d \right) e^{-sT} \tag{4.1}$$

In the above equation, k_d is the gain of the delay compensation path and the full-cycle

delay ($e^{-sT} = z^{-1}$) is allocated to the SAR-quantizer. By discretizing the above transfer

function [50] and equating the result with the desired discrete-time loop

filter $H_d(z) = z^{-1}/(1-z^{-1})$, the modulator coefficients are obtained as $k_1 = 1$ and

$k_d = 1$. This delay compensation technique can be applied to any higher-order system

to accommodate the full-cycle conversion time required for the SAR-quantizer.

In the CT-$\Delta\Sigma$ modulator shown in Figure 4.3(a) an outer loop TF $H'_c(s)$ from

DAC input U_1 to the CT filter output Y can be identified:

$$H'_c(s) = \left.\frac{Y(s)}{U_1(s)}\right|_{x(t)=0} \tag{4.2}$$

Design of SAR-based CT-$\Delta\Sigma$ modulator involves finding the delay compensation gain

k_d and the CT transfer function $H'_c(s)$ such that after discretization it will match a DT

transfer function $H'_d(z)$ that satisfies the following equation:

$$H_d(z) = z^{-1} \cdot \left(k_d + H'_d(z)\right) \tag{4.3}$$

where $H_d(z)$ is the ideal DT loop TF related to the target NTF as:

$$H_d(z) = 1 - \frac{1}{NTF(z)} \tag{4.4}$$

In an N-th order modulator, the DT transfer functions $H_d(z)$ and $H'_d(z)$ can be

expressed in general form as:

$$\begin{cases} H_d(z) = \dfrac{b_{N-1}z^{N-1} + \dots + b_1 z + b_0}{z^N + a_{N-1}z^{N-1} + \dots + a_1 z + a_0} \\ H'_d(z) = \dfrac{b'_{N-1}z^{N-1} + \dots + b'_1 z + b'_0}{z^N + a_{N-1}z^{N-1} + \dots + a_1 z + a_0} \end{cases} \tag{4.5}$$

Using (4.3) it can be shown that (see Appendix B) $H_d(z)$ and $H'_d(z)$ have the same

denominators, hence the same a_i coefficients. The gain k_d and numerator coefficients

of $H'_d(z)$ can be obtained from the coefficients of $H_d(z)$ using

$$\begin{cases} k_d = b_{N-1} \\ b'_j = b_{j-1} - a_j b_{N-1}\big|_{j=0...N-1} \end{cases} \tag{4.6}$$

In (4.6) for $j=0$ the b_{j-1} is zero (i.e. $b_{-1}=0$). The final design step involves discretizing

$H'_c(s)$ defined in (4.2), and equating it with $H'_d(z)$. For example in the first order

modulator shown in Figure 4.3, the required NTF is $NTF(z) = 1 - z^{-1}$ which leads to the

DT loop transfer function of $H_d(z) = 1/(z-1)$. Using (4.6), the delay compensation

feedback k_d and $H'_d(z)$ are identified as $k_d = b_0 = 1$ and $H'_d(z) = 1/(z-1)$. Using impulse-

invariant transformation and assuming NRZ DAC the CT equivalent of the $H'_d(z)$ is

$H'_c(s) = 1/sT$, where T is the sampling period. In this example $H'_c(s)$ is the ideal CT

integrator. Appendix-B provides another design example based on the second-order

NTF.

4.1.2 Partial Data Weighted Averaging

Data-Weighted-Averaging (DWA) is a simple, yet effective dynamic element

matching technique that provides a first-order shaping of the DAC element mismatch

[13]. However, the delay of the DWA blocks can add to the total loop-delay budget

and thereby, degrade the modulator performance. Thus, we have opted for a Partial-

DWA (P-DWA) technique in which DEM is performed using only the 4 MSB s of the

codeword generated by the SAR quantizer. Since the SAR-quantizer sequentially

generates the output bits from the MSB to the LSB, the DEM operation can be

performed without additional delay by skipping the LSB bit. In this way, DEM

concurrently proceeds as the SAR-quantizer extracts the LSB. Figure 4.4(a) compares the SNDR versus DAC element mismatch in a 1st-order-5-bit $\Delta\Sigma$-modulator with OSR=48 for three different cases of no DEM, with DWA, and with P-DWA. Compared with full DWA, partial DWA results in an SNDR degradation of less than 3 dB assuming an element mismatch of $\sigma = 2^{-6} = 1.5\%$. This small degradation warrants the use of P-DWA which allows us to avoid the excess loop delay problem and also simplify the DWA circuitry. Figure 4.4(b) shows the output spectrum of the modulator for two different cases with P-DWA and no DEM. The P-DWA algorithm still provides 21dB improvement in SNDR. For further improvement the device matching levels could be increased by a coarse calibration. Figure 4.5(a) and (b) show similar results for a 5-th order modulator with OSR=8. The difference between P-DWA and full-DWA shows a similar trend as the 1st-order case, however due to the lower effectiveness of DEM at low over-sampling ratios, both techniques demand higher initial matching to achieve full noise-shaping performance of the modulator.
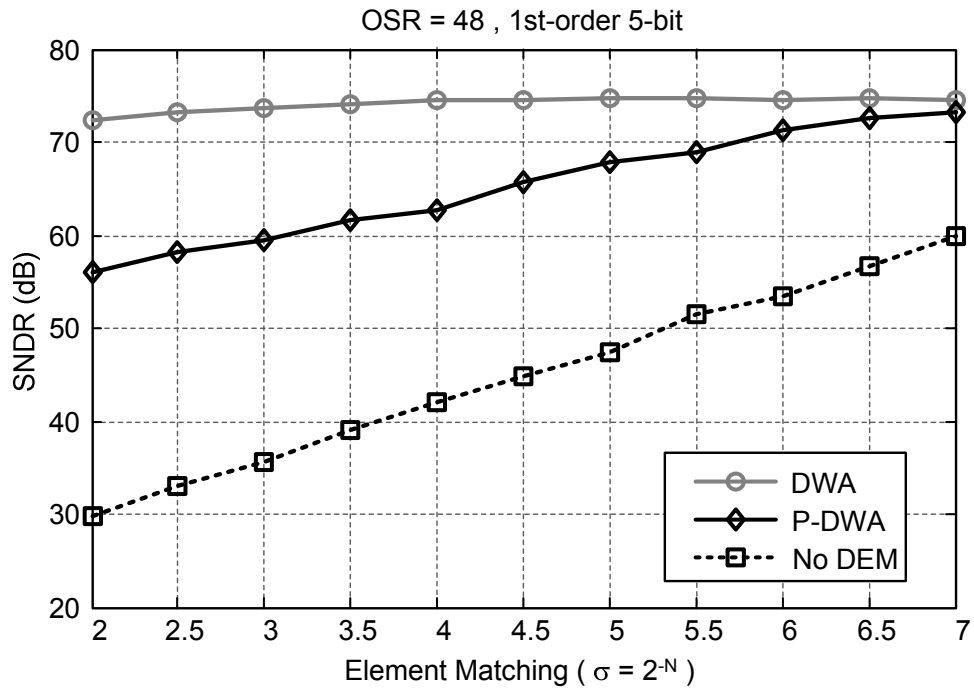
(a)
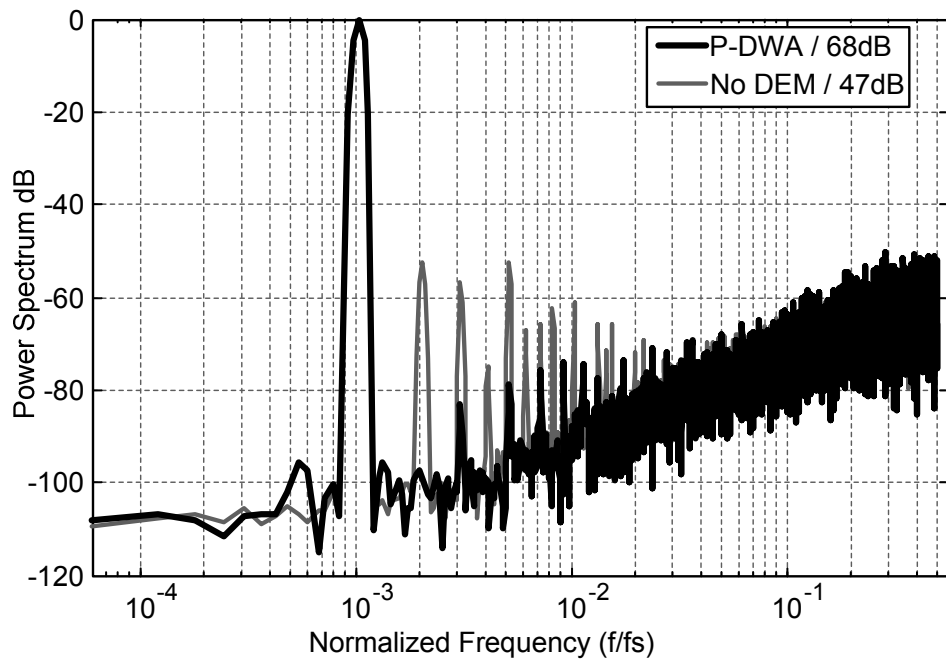
(b)

Figure 4.4: (a) SNDR of a 1st-order $\Delta\Sigma$-modulator at OSR=48 versus element mismatch plotted for DWA, P-DWA, and no DEM ; (b) Output spectrum of the modulator with and without P-DWA.
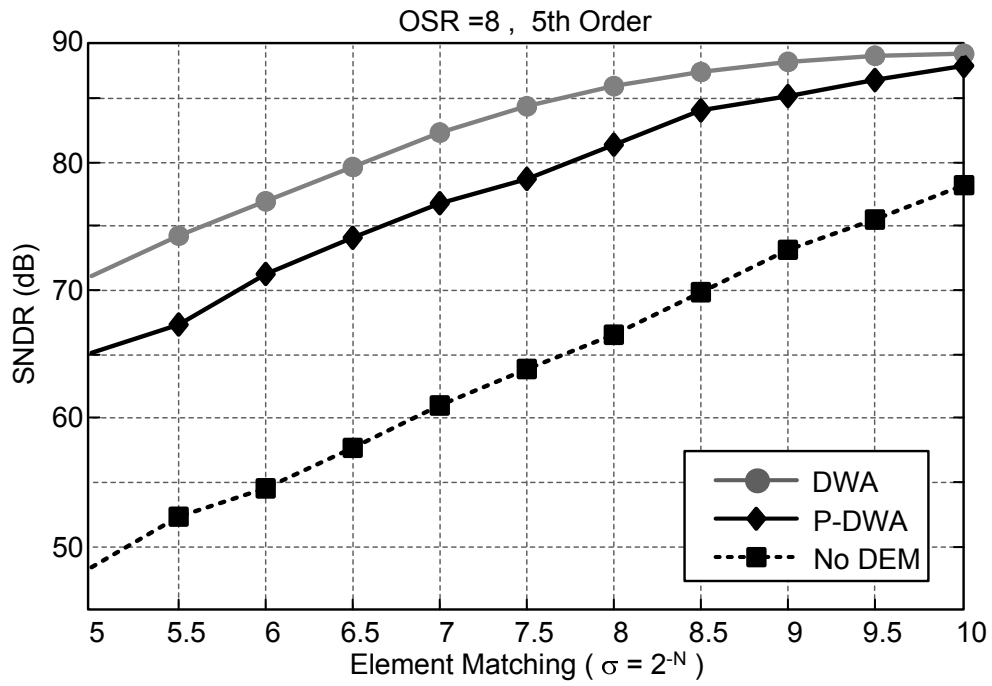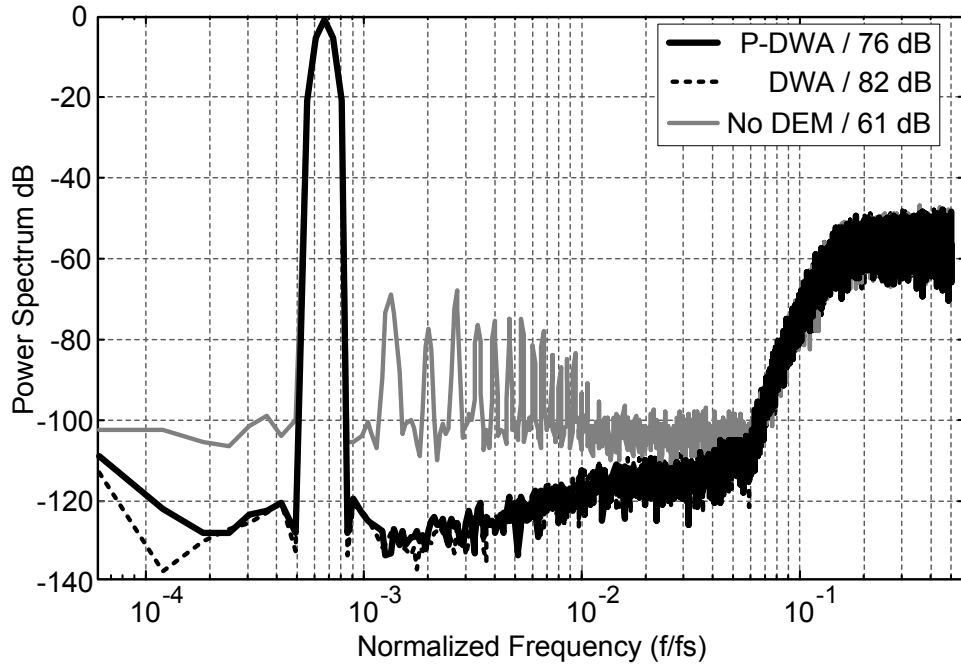
Figure 4.5: (a) SNDR of a 5th-order ΔΣ-modulator at OSR=8 versus element mismatch plotted for DWA, P-DWA, and no DEM ; (b) Output spectrum of the modulator with and without P-DWA.

4.1.3 SAR Quantizer Clock and Timing

A conventional N-bit SAR requires N clock cycles to quantize its input signal. In order to keep the SAR latency less than the modulator sampling period an N times faster clock will be required. In radio applications, such a high frequency clock is usually available on chip; hence there will be no need for external clock sources. Figure 4.6 shows a ring counter-based 6-phase clock generator (i.e. $N=6$) for a SAR quantizer. In this case the input clock is $6.F_S$ where F_S is the modulator sampling frequency. The modulator clock at F_S can be obtained by combining the first three outputs of the ring counter (i.e. *Phi1-Phi3*). Therefore there will be no need for a separate low-frequency clock input. The extra jitter generated by the ring counter and all the logic gates in the F_S path need to be accounted for in order to meet the modulator jitter specification.
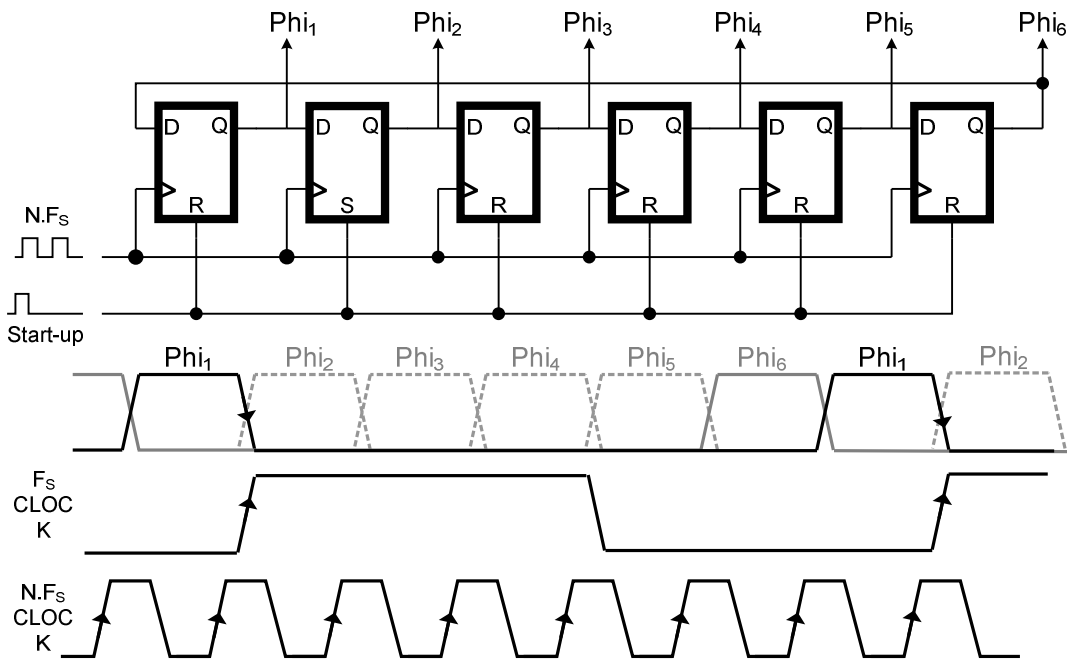
Figure 4.6: SAR quantizer multi-phase clock generation using a ring-counter.

In stand alone ADC applications, due to the high cost of discrete low-jitter clock generators, providing an off-chip high-frequency clock can be expensive. However the modulator clock at F_S can be used with an on-chip frequency multiplier to generate the required SAR clock with frequency $N.Fs$. Figure 4.7(a) and (b) show two different scenarios based on PLL and DLL respectively. In the PLL based method the divide-by-N in the feedback path ensures a frequency $N.Fs$ at the output of the VCO. In the DLL based approach, the negative feedback in the DLL loop tunes an N-tap delay line such that one sampling period of the input clock is divided into N equally spaced phases. The edge combiner logic is then applied to the delay line taps to generate the $N.Fs$ frequency.
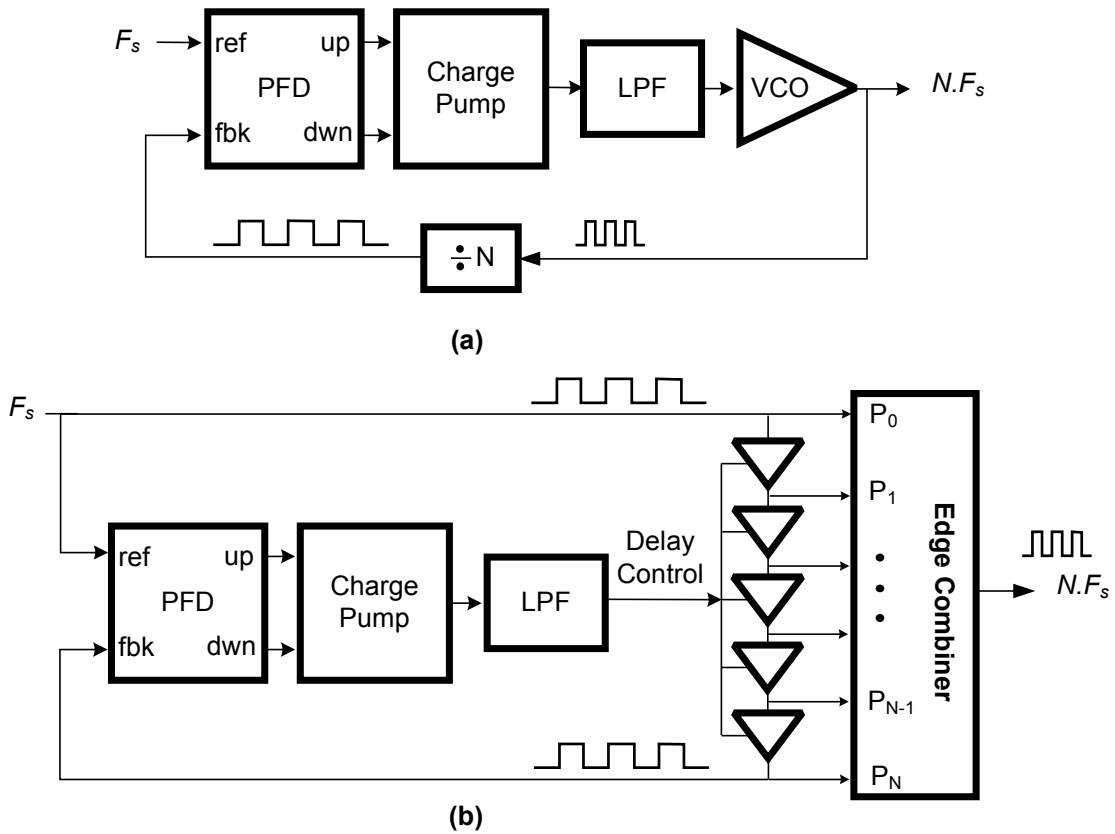
Figure 4.7: On-chip frequency multipliers based on (a) PLL and (b) DLL loops.

Alternatively an asynchronous SAR quantizer can be used that does not require a fast clock and eliminates the need for a PLL or DLL. In this case the asynchronous logic used within the SAR will automatically generate similar N-phase timing signals but with variable pulse widths. The main challenge of using asynchronous SAR lies in its interfacing to the DWA block which has to work synchronously with the modulator loop. However replacing DEM with analog calibration can simplify the timing requirements and allow for the use of asynchronous SAR which has a better potential for high-speed [49].

4.2 A First-Order 5-Bit SAR Based CT-$\Delta\Sigma$ Modulator

The block diagram of the first-order CT-$\Delta\Sigma$-modulator based on a 5-bit delay compensating SAR quantizer is shown in Figure 4.8. The modulator is intended for a WCDMA receiver application with 1.92 MHz signal bandwidth and 60dB dynamic range. The first order NTF of the modulator at OSR of 48 provides sufficient quantization noise attenuation with 10dB extra headroom compared to the target dynamic range. The required 184.32 MHz modulator sampling clock is provided by an external clock source and after on chip buffering is applied to the main 5-bit DAC. The SAR quantizer uses a 6-phase clock for resolving 5-bits. The 5th and 6th timing phases are dedicated to mismatch shaping of the main DAC using Partial-DWA. The 1.1GHz clock of the SAR-quantizer is generated internally from the external clock using an on-chip DLL. The decision to use on-chip frequency multiplier was merely due to practical limitations such as test board design issues. In transceiver applications, a synchronous high-frequency clock is usually available and there is no need for clock multiplication.
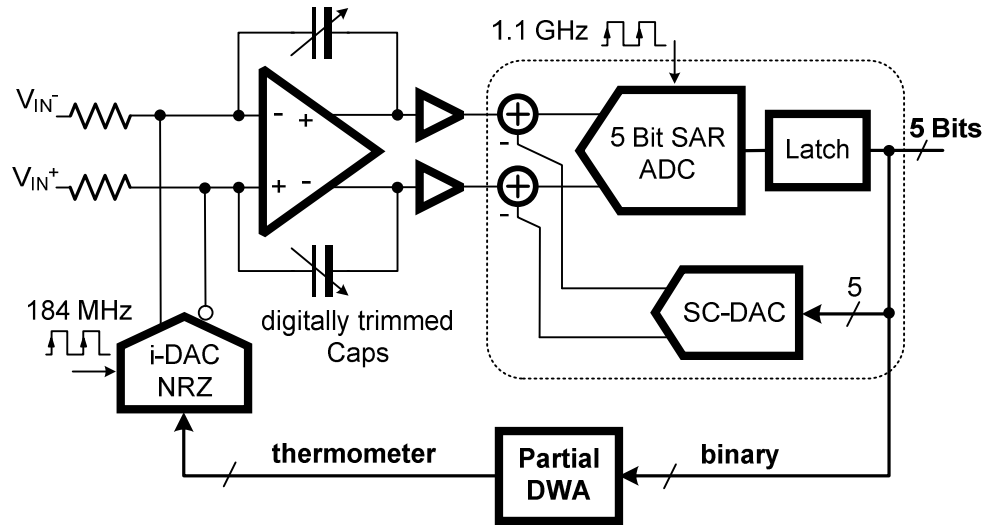
Figure 4.8: Architecture of the first-order 5-bit SAR-CT-ΔΣ modulator.

The required reference voltage for the SAR-quantizer is provided by an external source which is scaled and buffered on the chip prior to being routed to the quantizer. The same reference voltage is used to bias the current-mode DAC to ensure that the DAC gain and the SAR-quantizer gain track each other. Also two open-loop buffers are attached to the integrator outputs to prevent the potential back-propagation of kickback noise from the switched-capacitor SAR-quantizer towards the integrator. These open loop buffers may not be necessary in a higher-order modulator due to improved noise shaping.

4.2.1 Integrator and Amplifier Design

The integrator is implemented using the active-RC technique for high linearity. It also provides a virtual ground to sink the output of the current-mode DAC. Behavioral simulations showed that the system could tolerate up to 30% integrator gain variation without causing more than 4 dB SQNR degradation. Since foundry data indicated an RC-product variation of up to 30%, the integrating capacitors are trimmed to keep the

integrator gain within the acceptable range. A capacitor bank, controlled by an external 2-bit code, is used to keep the integrator gain within 7.5%. This limits the maximum loss in SQNR to less than 1 dB.

The total input-referred noise power of the modulator is derived as

$$P_N \approx 8KTf_B \left[R_{in}(1 + \frac{8}{3}\frac{\hat{V}_{in}}{V_{GST}}) + \frac{2\eta_{th}}{3g_m} \right] + \frac{K_f\eta_f}{C_{ox}^2 WL}\ln(\frac{f_B}{f_u}) \qquad (4.7)$$

In the above equation $\hat{V}_{in}$ is single-ended peak amplitude of the input signal, V_{GST} gate the overdrive of the DAC current source, f_B the signal bandwidth, f_u the lower integration bound for flicker noise, g_m the amplifier input transconductance, W and L the input device sizes and K_f the flicker noise coefficient. Also η_{th} and η_f are thermal noise and flicker noise factors of the opamp, respectively. The terms inside the brackets represent thermal noise contributions of the input resistors, DAC, and the opamp. We assume a current-mode DAC as shown in Figure 4.7(a) that has N-type switched current sources and P-type devices on top providing the common-mode current. The DAC current noise was minimized by maximizing the gate overdrive voltage of the current sources. The amplifier is the major source of flicker noise. Hence a PMOS input differential pair along with source degeneration for NMOS devices is used to minimize the amplifier flicker noise. The entire integrator and DAC were designed for 68dB signal-to-noise-ratio. An important challenge faced in this design is the small amplitude of the input signal which is 150 mV-peak single-ended. The small input amplitude calls for a small input resistor (R_{in}) to meet the noise requirement. A small input resistance, however, adversely affects the integrator linearity. Assuming weakly nonlinear fully
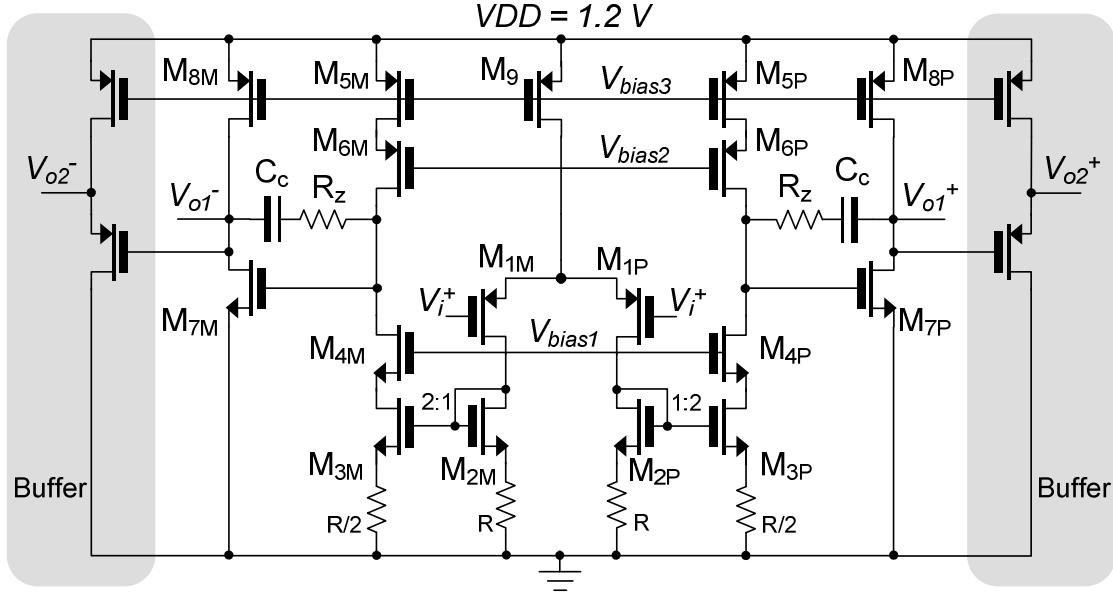
Figure 4.9: Schematic of the fully-differential amplifier with output buffers.

differential amplifier the harmonic distortion due to the opamp is [51]

$$HD3 \approx \frac{\widehat{V}_{in}^{2}}{64 \cdot g_m \cdot R_{in}^{3} \cdot I_D^{2}} \cdot \left(1 + \frac{k_{dac}}{k_{in}}\right) \qquad (4.8)$$

In the above equation k_{in} and k_{dac} respectively are the input and feedback gains of the modulator which are equal in this design. The R_{in} and g_m values are fixed by noise requirements according to (4.7) hence the integrator linearity can be improved only by increasing the amplifier bias current, I_D.

A two-stage amplifier was selected for its larger output swing and better linearity compared with a single-stage amplifier. The schematic of the amplifier is shown in Figure 4.9. The first stage of the amplifier uses a current-mirror with a ratio optimized for best trade-off between current drain, gain-bandwidth and phase margin. To achieve the maximum output swing, the output stage comprises of only two transistors. Instead the output of the first stage which has smaller voltage swing is cascoded to achieve high
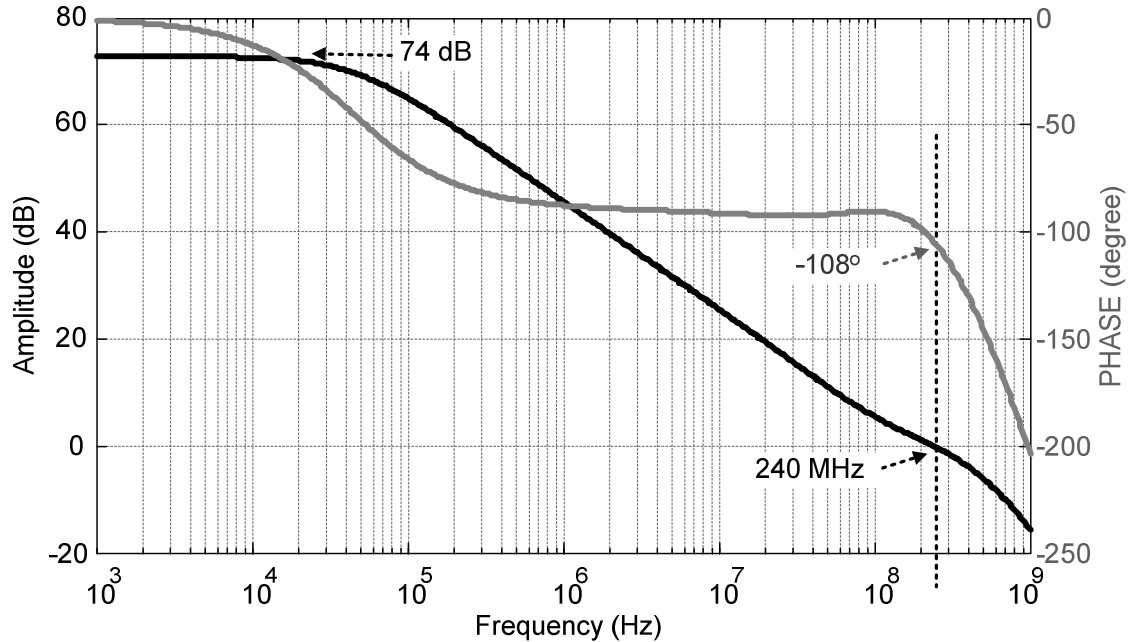
Figure 4.10: Amplitude and phase response of the designed amplifier.

DC gain.

Frequency compensation is done by means of a Miller capacitor and a series resistor to get rid of the right-hand plane zero. The op-amp achieves a DC gain of 74 dB and a unity gain-bandwidth of 240MHz with 72 degrees phase-margin under worst-case conditions. The AC simulation results in Figure 4.10 show the magnitude and phase response of the amplifier. The buffers attached to the integrator outputs, as shown in Figure 4.s 8 and 9 are intended to drive the sample-and-hold (S&H) of the SAR and to isolate the integration capacitor from the switching noise of the SC-quantizer. Low-threshold devices are used in these source-follower stages to minimize the resulting DC level shift. These buffers are placed outside the integrator loop so that their output pole does not affect the integrator loop stability. Also any noise and distortion caused by the buffers will be rejected in the signal band by modulator NTF.

4.2.2 The 5-bit SAR Quantizer

The schematic of the 5-bit SAR quantizer with embedded delay compensation is shown in Figure 4.11(a). The actual circuit is fully-differential, but only a single-ended half-circuit is shown for the sake of simplicity. Two identical Switched-Capacitor DACs (SC-DACs) are implemented. One is part of the SAR-quantizer and the other one is employed for delay compensation. The timing diagram of the circuit is shown in Figure 4.11(b). At the falling edge of $\Phi1$, which corresponds to the rising edge of the 184.32 MHz clock, the input signal is sampled by the SAR DAC. At the same time, the main current-mode DAC in the modulator feedback path is refreshed. The SAR logic uses a six-phase clock for timing and control. An on-chip DLL-based frequency multiplier generates the six-phase timing control signals as well as the 1.1 GHz clock needed for the comparator from the 184.32 MHz input clock.

The 5-bit SC-DAC, depicted in Figure 4.12(a), is a hybrid resistive-capacitive structure [52] where 2 bits are generated by a resistor string and 3 bits by a capacitive network. This strategy requires only 8 unit capacitors and provides a 4X reduction in the total capacitance compared with a purely switched-capacitor implementation. Since the DAC parasitic capacitance appears as the load of the source-follower driving the quantizer, this hybrid structure helps with reducing the power consumption of the source follower. The 3-bit MSB section is thermometer-decoded to reduce possible transition glitches and improve linearity. The switch control logic for one slice is shown in Figure 4.12(b). This circuit arrangement prevents a short circuit between the input and reference signals by adopting a non-overlapping break-before-make switching scheme. Moreover, to perform bottom-plate sampling switch M5 is guaranteed to turn-
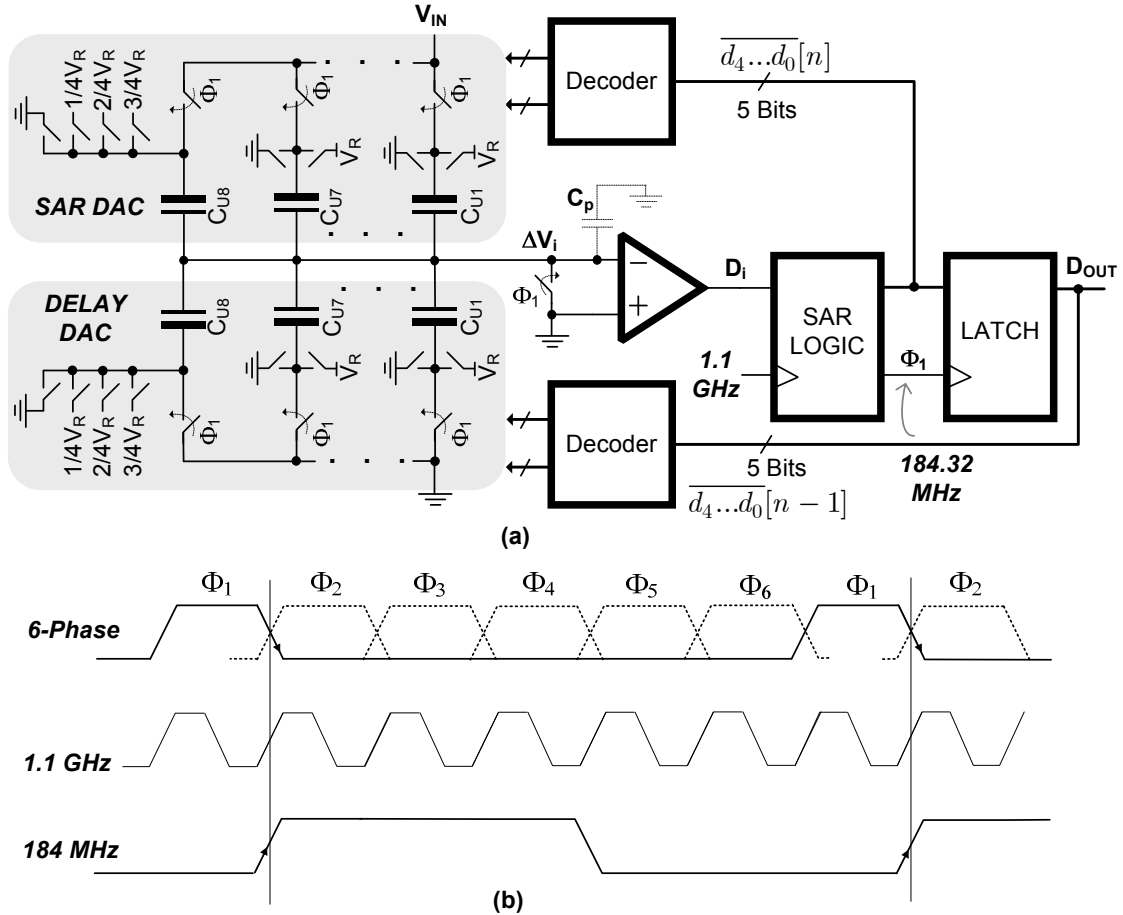
Figure 4.11: **(a)** Schematic of the delay-compensated 5-bit SAR; **(b)** Timing diagram.

off before input switches M1 and M2. The only control signals are $\Phi 1$ and the data lines

coming from the MSB decoder (see Figure 4.13(a)). The SAR logic is built into the 3-

bit binary-to-thermometer decoder by combining the control pulses $\Phi 2$-$\Phi 4$ through the

NOR gates placed at the input. Thus, unknown bits can be set to logic '1' during the

detection phase. The 2-bit LSB section of the DAC uses binary decoding to apply 1 of

the 3 additional reference levels to the last unit capacitor (C_{U8}). Therefore, the last slice

includes three additional CMOS switches, as conceptually illustrated in Figure 4.12(a).
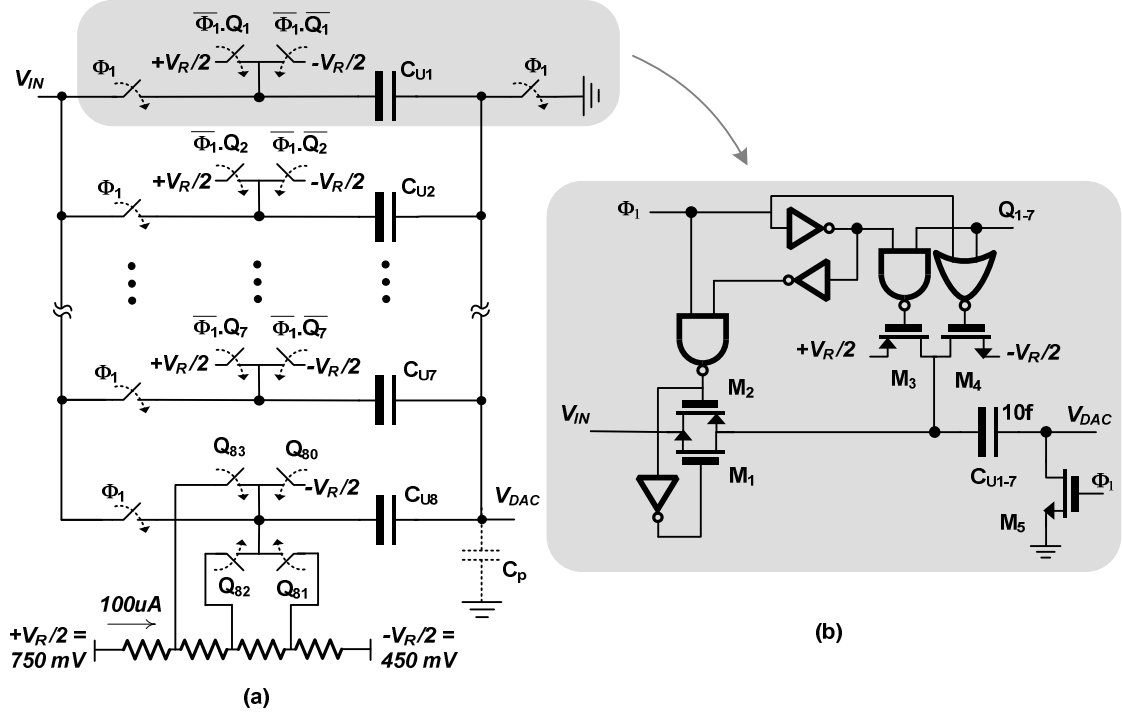
Figure 4.12: (a) Structure of the Split 3bit-2bit SC-DAC, (b) One slice of the MSB section (Cu1 – Cu7) showing the non-overlap switching logic.

The required reference levels are generated by a 4-element resistor string which can be made low-power because of low capacitive load and relaxed 2-bit settling requirements. As shown in Figure 4.13(b), the 2-bit binary 1-of-4 decoder is modified in the same way as the MSB decoder to perform the SAR operations during $\Phi5$-$\Phi6$.

Referring to Figure 4.11 and 4.12(a) the voltage generated by SC-DACs can be related to their input data as:

$$V_{DAC1} = V_R \left[\sum_{i=1}^{3} d_i[n]2^{-i} + \frac{1}{8}\sum_{i=4}^{5} d_i[n]2^{-i+3} \right] \tag{4.9}$$

$$V_{DAC2} = V_R \left[\sum_{i=1}^{3} d_i[n-1]2^{-i} + \frac{1}{8}\sum_{i=4}^{5} d_i[n-1]2^{-i+3} \right] \tag{4.10}$$
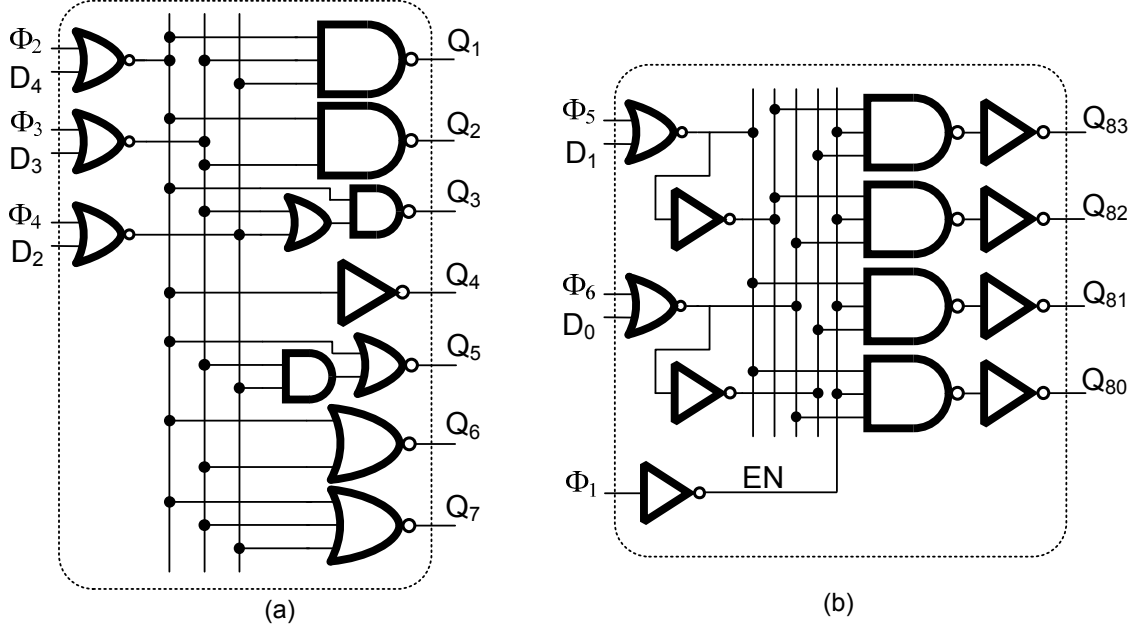
Figure 4.13: (a) 3-bit MSB binary to thermometer SAR-Decoder, (b) 2-bit LSB binary to 1-of-4 SAR-Decoder.

The 5-bit binary code $\overline{d_4...d_0}[n-1]$ of the previous sample is applied to DAC$_2$ (delay-DAC in Figure 4.11). The current binary code $\overline{d_4...d_0}[n]$, under the SAR control, is applied to DAC$_1$ (SAR-DAC in Figure 4.11). Since DAC$_2$ does not use the Φ_2-Φ_6 control signals, the corresponding inputs in its MSB and LSB decoders (see Figure 4.13) are tied to ground. The associated V_{DAC2} voltage will be produced by the falling edge of $\Phi1$. During $\Phi2$-$\Phi6$, while switch M5 is off, charge sharing between the two DACs will generate a voltage at the comparator input as

$$\Delta V_i = \frac{(V_{DAC1} - V_{IN})8C_u}{16C_u + C_p} + \frac{(V_{DAC2} - 0)8C_u}{16C_u + C_p} = -\left[(V_{IN} - V_{DAC2}) - V_{DAC1}\right]\frac{8C_u}{16C_u + C_p} \quad (4.11)$$

The above equation demonstrates the summing operation at the quantizer input through charge sharing. This technique obviates the need for an active adder which would have required an additional amplifier. The price paid for this benefit is extra attenuation by a
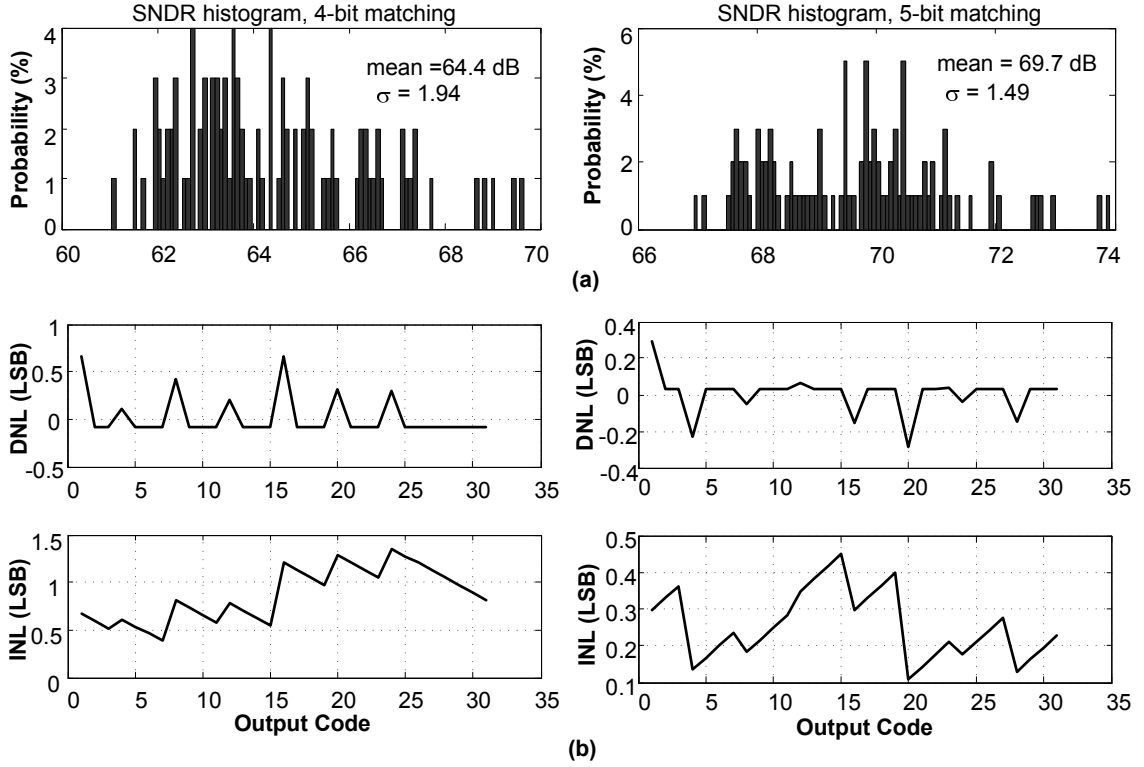
Figure 4.14: (a) 3-bit MSB binary to thermometer SAR-Decoder, (b) 2-bit LSB binary to 1-of-4 SAR-Decoder.

factor of 2 which necessitates a comparator pre-amplifier with higher DC gain.

Mismatch between capacitors used in the SAR quantizer affects mean and standard deviation of the modulator SNDR. Figure 4.14 compares the Monte-Carlo simulation results when the unit capacitors in both switched-capacitor DAC s have 4-bit or 5-bit matching accuracy. It can be seen that 5-bit matching is required to keep the INL well below one LSB and ensure an SNDR of better than 67dB. Using the foundry provided data, the vertical metal-metal capacitors of the SC-DACs were sized to achieve a 5-bit matching accuracy (i.e. mismatch $\sigma = 2^{-5}$).

The comparator and its building blocks are shown in Figure 4.15. It comprises a pre-amp and a current-multiplexed latch. The comparator is clocked at 1.1 GHz and

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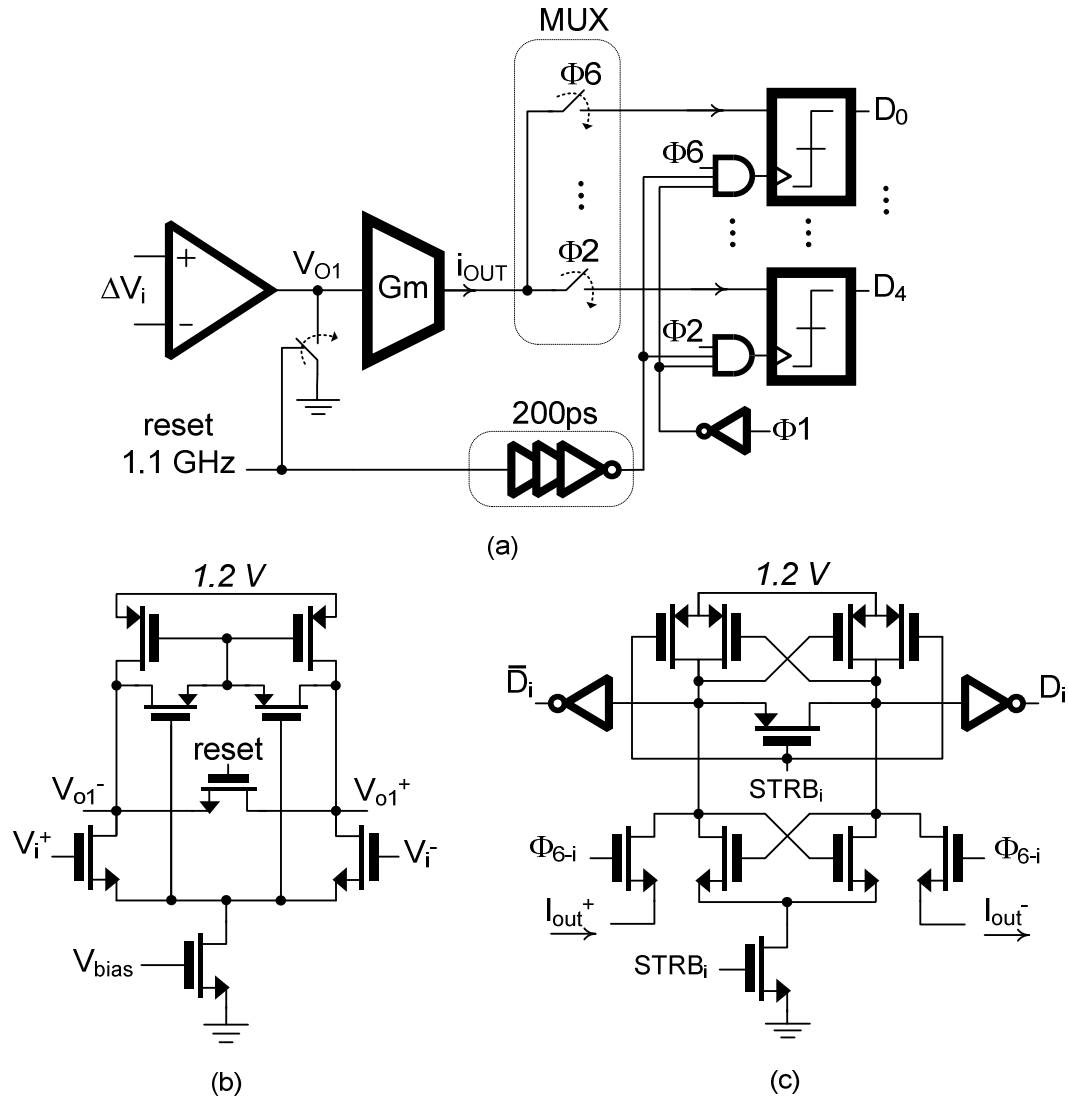
Figure 4.15: (a) Block diagram of the comparator employing time-multiplexed latches. (b) Schematic of the preamp. (c) Schematic of the latch.

resolves a 3.75 mV error voltage in 900 ps. This level of sensitivity is equivalent to $1/4^{th}$ of one LSB of the SAR after taking into account the attenuation of the SC-network. During the first half of each phase, when the SAR-DAC is not fully settled, a reset switch shorts the pre-amp outputs together to prevent the output nodes from moving in the wrong direction. The latch at the comparator back-end consists of five multiplexed regenerative stages with a shared transconductor. Current-mode multiplexing is

performed for high-speed operation. The transconductor stage reduces the kickback noise and converts the pre-amp input voltage into a current. Multiplexing also reduces the capacitive load of the pre-amp and thereby, its static power. Dynamic power is also reduced because the individual latches have a smaller fan-out and only one latch remains active during each phase. The penalty is a variable input-referred offset which can cause nonlinearity if it becomes comparable to the LSB. Simulations indicated a standard deviation of 60 mV for the latch offset. This calls for a minimum pre-amp DC gain of 6.4 to mitigate the problem. The actual pre-amp was designed with a worst-case gain of 10 which provides sufficient margin for safe operation. The combined power consumption of the 5-bit SA-quantizer and the delay compensation DAC is 1.3 mW from a 1.2 V supply when clocked at 1.1 GHz.

4.2.3 Current Mode DAC

The modulator employs an NRZ DAC in its main feedback path. Choice of current-mode design for this DAC simplifies its interfacing to the first integrator, where the amplifier summing nodes provide a low-swing and low-impedance sink for the DAC outputs. Figure 4.16(a) shows the structure of the 5-bit current mode DAC. The current sources are grouped as 15 pairs controlled by the P-DWA, and a single cell controlled by the LSB bit. To minimize the effect of gradient-induced errors, the MSB pairs are laid out in common-centroid form and the LSB cell is placed at the geometrical center of the layout as shown in Figure 4.16(b). Separate supply voltages are used for the input buffers and the switch drivers to avoid trigger time modulation due to supply noise.
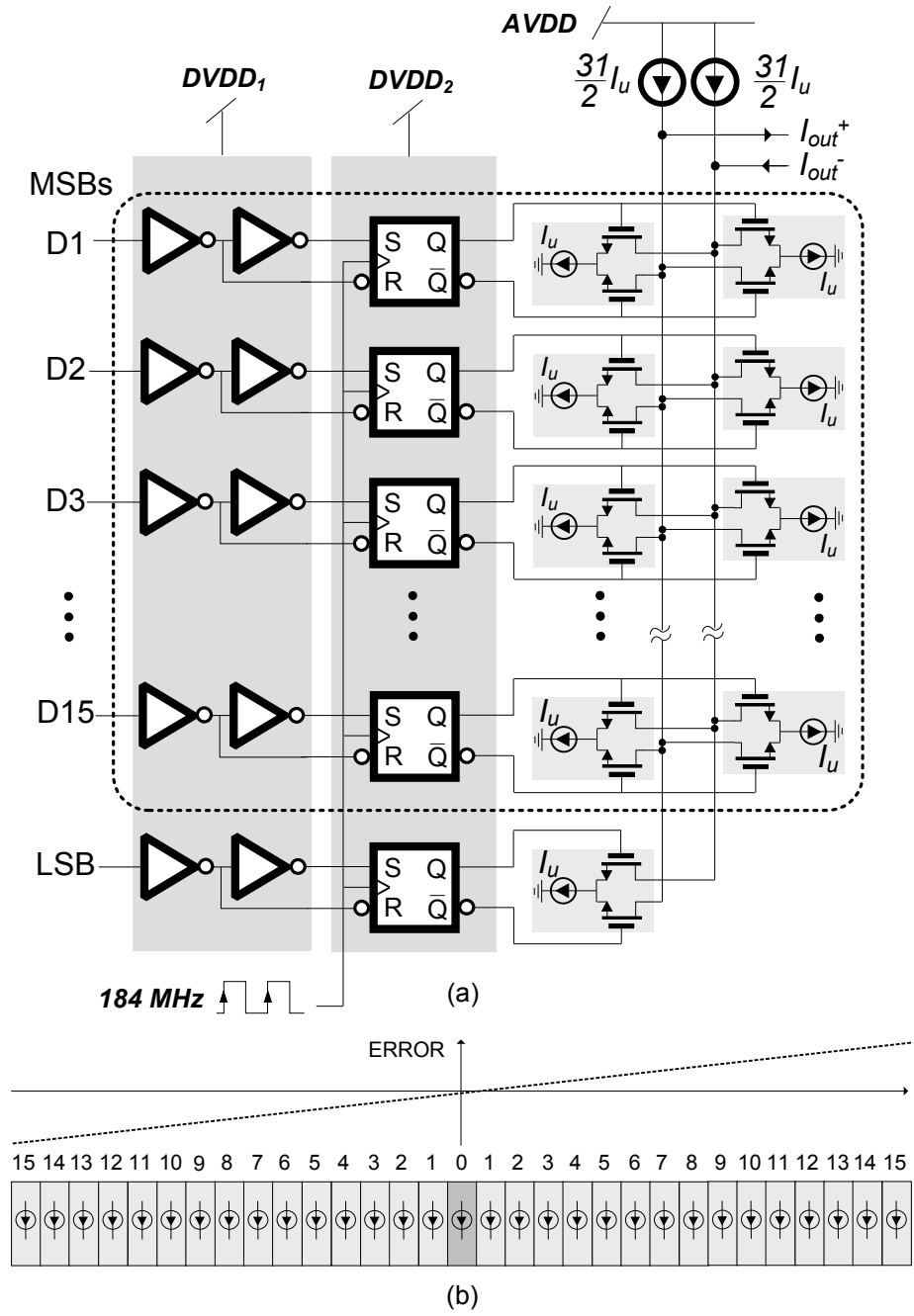
Figure 4.16: (a) Structure of the 5-bit current mode DAC, (b) Common-centroid layout of the current cells to reduce linear gradient errors.

Figure 4.17 depicts a current cell and its switch driver. A cascode current source is used to increase the DAC output resistance and also to shield the large drain capacitance of the current source devices from the opamp inputs.

Figure 4.17: (a) Structure of the 5-bit current mode DAC, (b) Common-centroid layout of the current cells to reduce linear gradient errors.

The current source devices (M_1) are sized for 6-bit matching ($\sigma = 2^{-6}$) using the formula in [53] while taking its noise current into account. A single cascode current mirror is used to bias all current cells. The bias lines are bypassed by two large capacitors to protect them against noise coupling. The DAC bias current is generated from the reference voltage of the quantizer by means of a difference amplifier and a replica of the input resistor (see Figure 4.17). The negative feedback loop forces the unit current to be equal to $I_u = V_{REF} / 32R_{in}$. This guarantees that the quantizer and DAC gains will track each other.

The switch driver generates a high-side crossing pulse for the NMOS current switches to prevent large current glitches. It also ensures an NRZ waveform generation by retaining the data until the next clock edge. The current switch is a pair of minimum-size NMOS transistors (M_4, M_5) operating in the triode region when they are turned on. An identical pair (M_6, M_7) with opposite connections is added for charge injection

cancellation. Since the nodes shown by letter *X* on both pairs (source nodes) track the amplifier's virtual ground voltage, the charge injected by the dummy switches will closely match the charge injected by the main switches. Charge cancellation will thus be limited by random mismatch between the two pairs.

4.2.4 5-bit Partial-DWA Implementation

The architecture design of an N-bit P-DWA for use with N-bit SAR-quantizer is shown in Figure 4.18(a). Since the output of the SAR-quantizer is binary, a binary-to-thermometer decoder must be placed in the feedback path of the $\Delta\Sigma$-modulator. The thermometer output is then applied to a barrel shifter for dynamic element matching. The pointer to the barrel shifter comes from a digital integrator implemented by a modulo-adder ($2^{N-1}-1$) and *N-1* bit register (see Figure 4.18(a)). The implemented 5-bit P-DWA uses a modulo-15 adder and a 4-bit register in its integrator. Also a 4x4 matrix shifter using dynamic logic techniques has been designed for fast response and low-power consumption. The circuit implementation of the barrel-shifter is shown in Figure 4.18(b). In order to keep the area small only a single transistor NMOS device is used as the matrix switch. When Φ_1 is low a pre-charge is applied to the rows, which sets all bit-lines to logic *"1"*. The level-active latches make sure the outputs do not change their states when Φ_1 is low. During Φ_1's high state, the $D_i[15:0]$ inputs are evaluated, which depending on the input level and the shift pointer value, can discharge the corresponding output rows to logic *"0"*. Since the SAR output is latched every cycle, it is ensured that during the evaluation phase, the inputs will show no transition. Each barrel-shifter output is used to control two unit elements of the DAC.
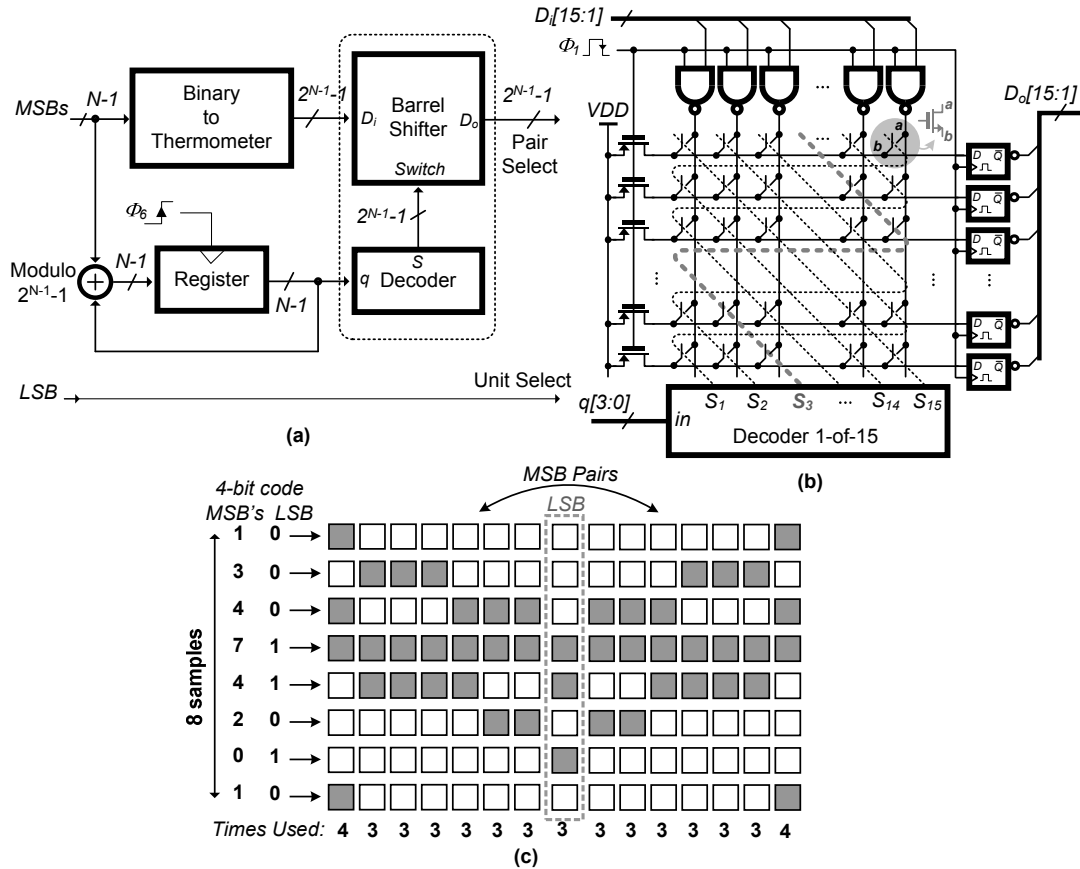
Figure 4.18: (a) Hardware realization of P-DWA for N-bit quantization; (b) Circuit design of a 15x15 matrix shifter (c) P-DWA operation for a 4-bit quantizer case.

The barrel shifter usually dominates the total power and area of a dynamic-element matching block. One benefit of using P-DWA algorithm is that skipping the LSB shrinks the area and power of the digital hardware by nearly a factor of 4.

Figure 4.18(c) shows the operation of the P-DWA block by way of example. In the depicted 4-bit case, three MSBs are sent through the input decoder and barrel shifter to the output to select 7 element pairs, laid out symmetrically around a central LSB unit-element which is directly controlled by the LSB bit. The pairs are rotated by the barrel shifter according to a pointer received from the modulo-accumulator. The rotation ensures that all pairs are used for an equal number of times so that the random
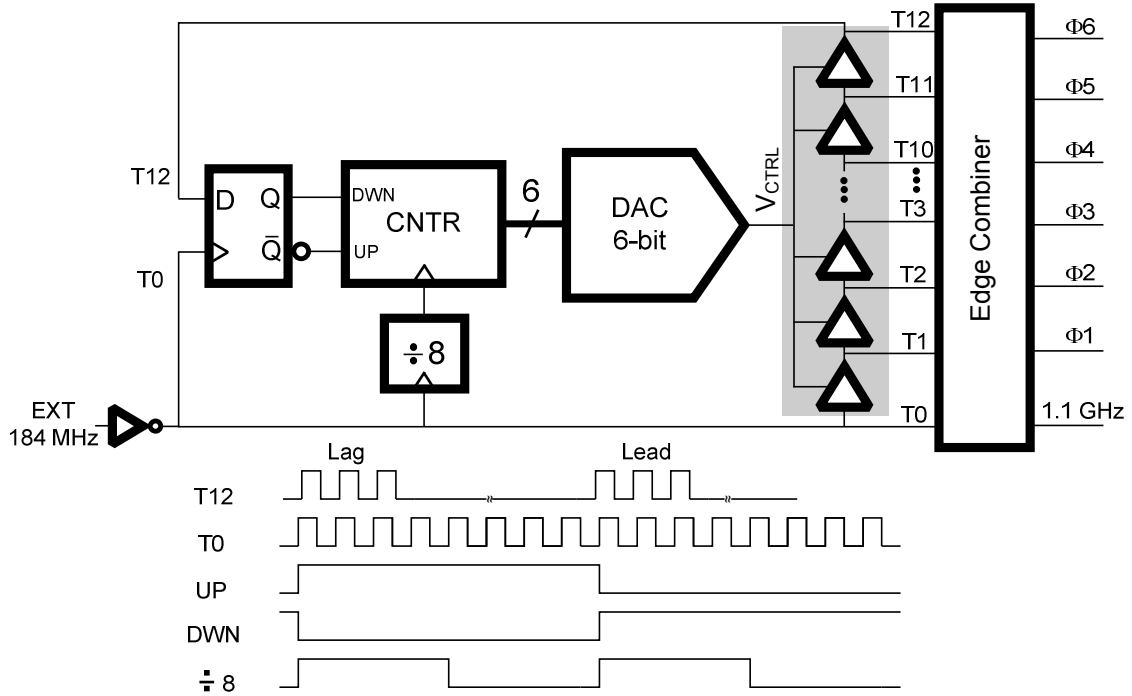
Figure 4.19: Block diagram and timing of the Digital-DLL.

mismatch error is averaged out. The circuit implementation of the 5-bit P-DWA consists

of a 4-bit binary-to-thermometer decoder, a 15x15 matrix shifter, a modulo-15 adder, a

4-bit binary decoder, and a 4-bit register for the shift pointer. The pointer register gets

updated at the rising edge of Φ_6 to ensure that matrix shifter does not see any activity on

its select inputs when it is handling the shift operation during Φ_1 .

4.2.5 Digital DLL

The SAR-quantizer needs a 1.1 GHz clock for its comparator and a six-phase

clock for control and timing. A Digital-DLL similar to [54] was selected for on-chip

generation of the required clocks. The structure and timing diagram of the DLL is

shown in Figure 4.19. It includes a D-FF as phase detector and a 6-bit up/down counter
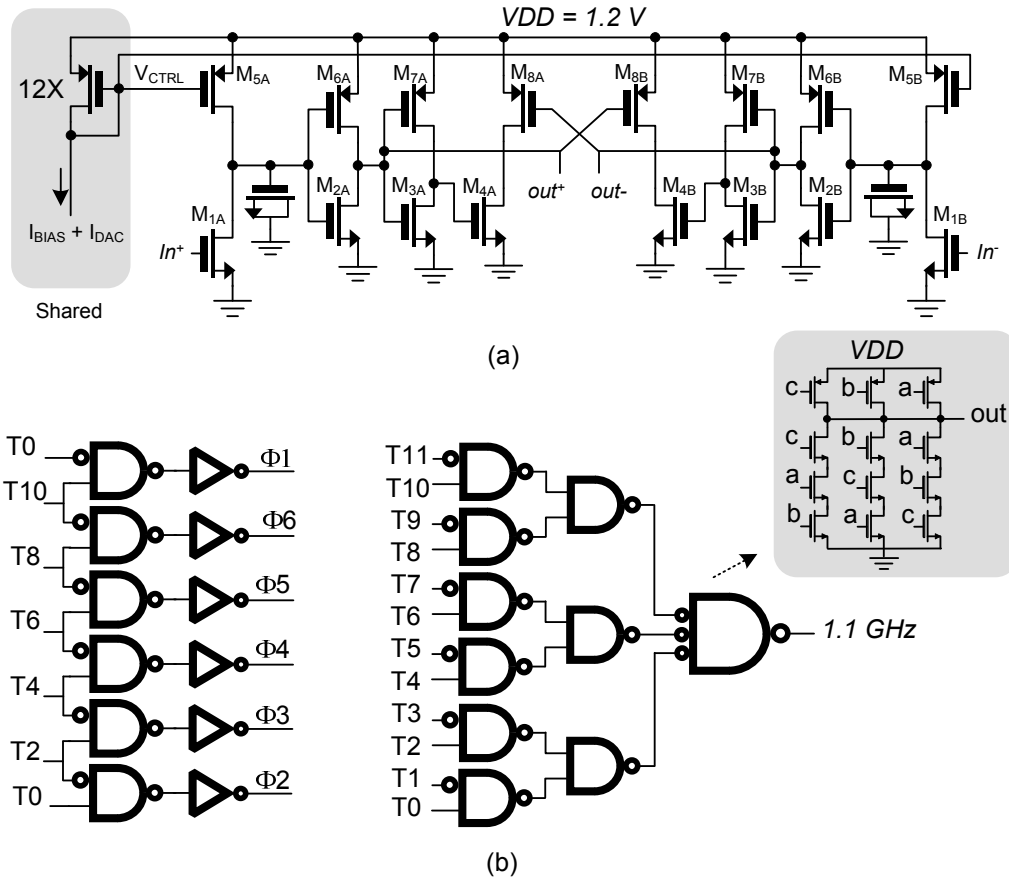
Figure 4.20: (a) Fully-differential variable delay buffer; (b) Gate-level design of the edge combiner.

as loop filter. The 6-bit current-mode DAC generates a bias current for a fully-differential delay element whose delay is inversely proportional to the DAC current.

The delay element is depicted in Figure 4.20(a). The current source devices $M5_{A\text{-}B}$ charge the MOS capacitors by a copy of the DAC current. When one side is charging, the opposite side is reset by the NMOS transistor M_1. When the capacitor voltage reaches the trigger point of the inverter formed by $M_2\text{-}M_6$, the corresponding output drops to *'0'* and the opposite output is simultaneously forced to *'1'* by the cross-coupled PMOS devices $M8_{A\text{-}B}$. Since the rising edge of one side coincides with the falling edge of the other side, there will be no change in the clock duty-cycle caused by unequal

PMOS/NMOS rise and fall times. Even and equal duty cycles for all taps of the delay line feeding the frequency multiplier is necessary to achieve 50% duty cycle at the output. Gate-level design of the edge combiner generating the 6-phase clock along with the frequency multiplier producing the 1.1 GHz clock is shown in Figure 4.20(b). A constant duty-cycle for the 1.1GHz clock requires the propagation delay of the multi-input NAND gates for all the inputs to be identical. This is shown for the 3-input NAND gate in the gray box in Figure 4.20(b). The same requirement needs to be met for the 2-input NAND gates as well.

4.2.6 Test and Measurement Results

The microphotograph of the chip fabricated in a 130 nm CMOS process is shown in Figure 4.21. The chip includes a $\Delta\Sigma$-modulator, a DLL, a reference buffer, and LVDS I/O drivers. All empty areas were filled with de-coupling capacitors. The active area including the $\Delta\Sigma-$modulator and its peripherals is 600 μm x 600 μm. The delay-compensated SA-quantizer occupies 140 μm x 280 μm. The total chip area is 1.1 mm x 1.1 mm. The IC is encapsulated in a QFN 32pin plastic package. All pads have full ESD protection. Separate supply and ground pins are used for analog, digital and I/O. Dedicated bias pins are assigned to the $\Delta\Sigma-$ modulator, DLL and LVDS I/O drivers.

The block diagram of the test setup is shown in Figure 4.22. For all measurements, a 184.32 MHz sine-wave with 0.6V DC offset served as the main clock. The clock pin is terminated by a 50 ohm on-chip resistor. A cascade of three CMOS inverters converts the sine-wave into a square waveform. A single-ended 208 KHz sine-
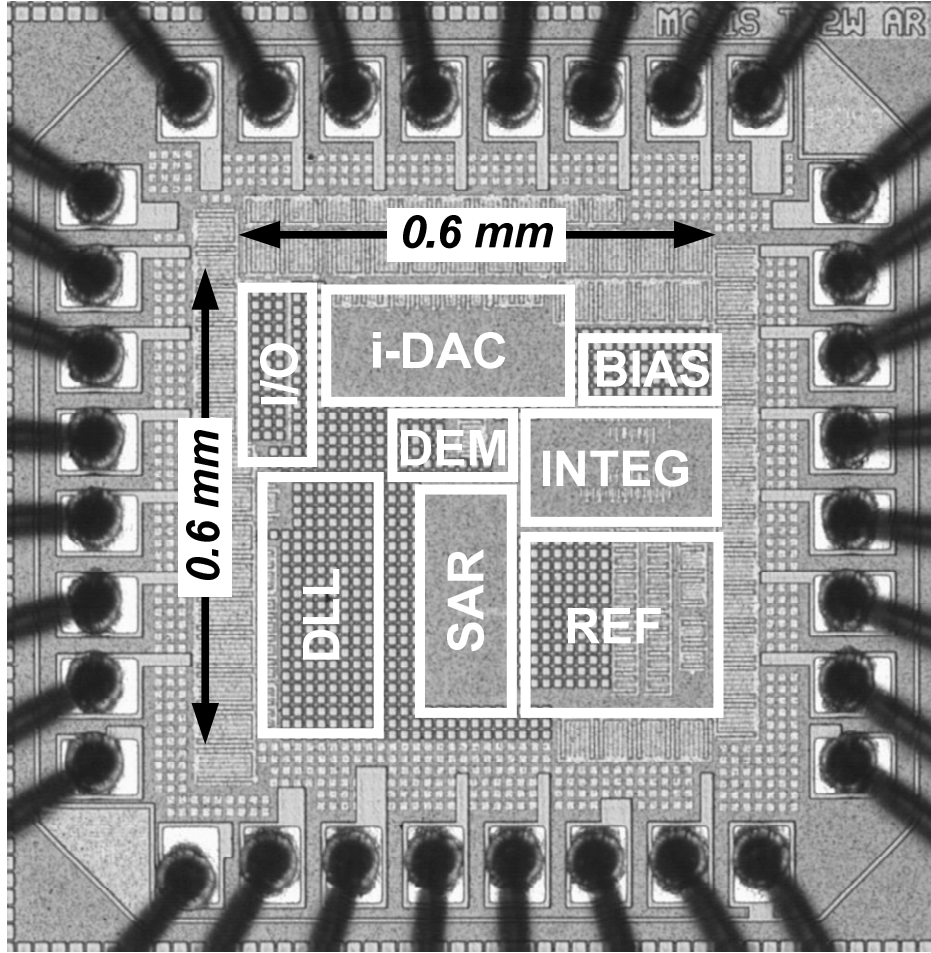
Figure 4.21: Die microphotograph of the 1st-order SAR based CT-$\Delta\Sigma$.

wave filtered by a 6th-order Butterworth passive bandpass filter was used as the signal source. the sine-wave into a square waveform. A single-ended 208 KHz sine-wave filtered by a 6th-order Butterworth passive bandpass filter was used as the signal source. Single-ended to differential conversion was performed with a discrete differential op-amp mounted on the test board. The differential LVDS outputs of the chip were converted to 3.3 V CMOS on the test board before being probed by the logic analyzer. The measured in-band-noise power in the idle mode with inactive P-DWA was -61 dBFS. Upon activating the P-DWA, the in-band noise dropped to -69 dBFS. Figure 4.23
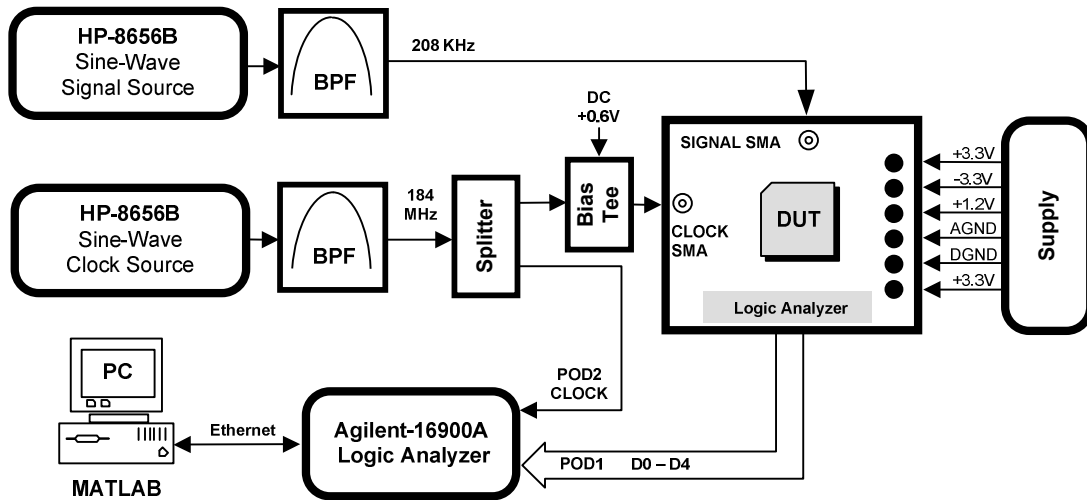
Figure 4.22: Measurement setup for the 1st-order SAR CT-ΔΣ test chip.

shows the output spectrum obtained from a 32K-point FFT for a -6 dBFS input. The strong even-order harmonics observed in the spectrum are related to the pseudo-differential nature of the SC-DACs. Although even-order distortion had been predicted by circuit simulations, it was found to be larger in the measurements. Based on post-fabrication simulations, two potential sources have been identified for this degradation. The first one is that the actual mismatch between the vertical metal capacitors, used in the SA-quantizer and also the delay compensation DAC, may have been larger than what was predicted by the model. The second source is unaccounted timing errors caused by the digital DLL. Figure 4.24 shows the SNR and SNDR versus the input amplitude relative to full-scale. A peak SNR of 65 dB is achieved at -3 dBFS input while a peak SNDR of 59 dB is obtained at -6 dBFS input. The modulator achieves 62 dB dynamic range which is equivalent to about 10 effective-number-of-bits (ENOB) .
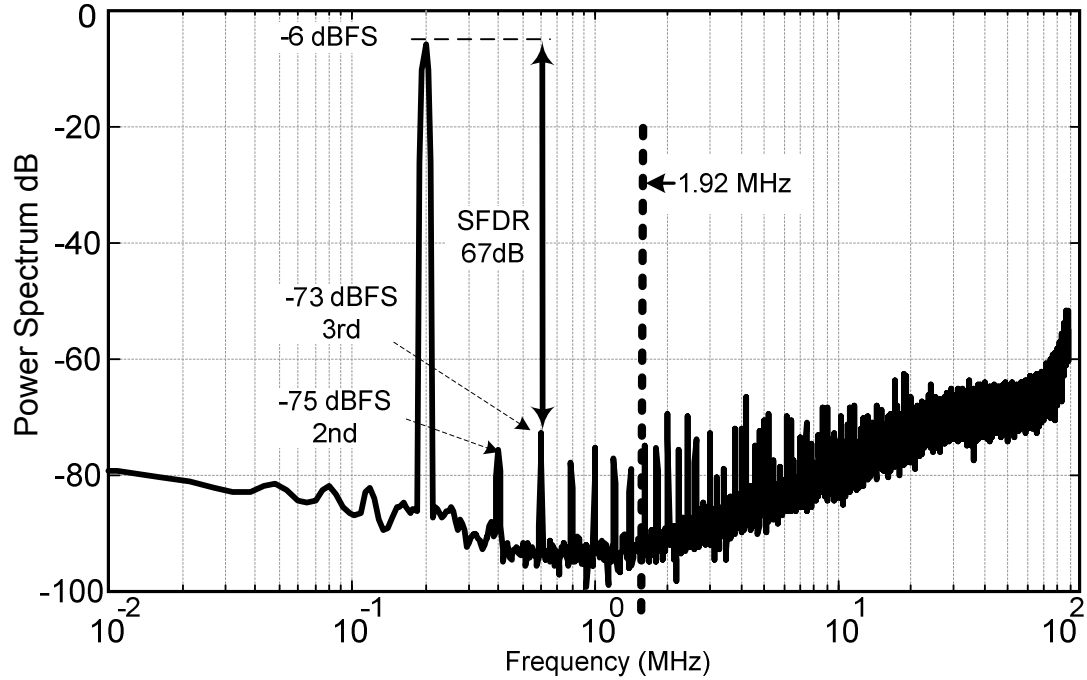
Figure 4.23: Output spectrum of the modulator for a -6dBFS sine wave at 208 KHz.
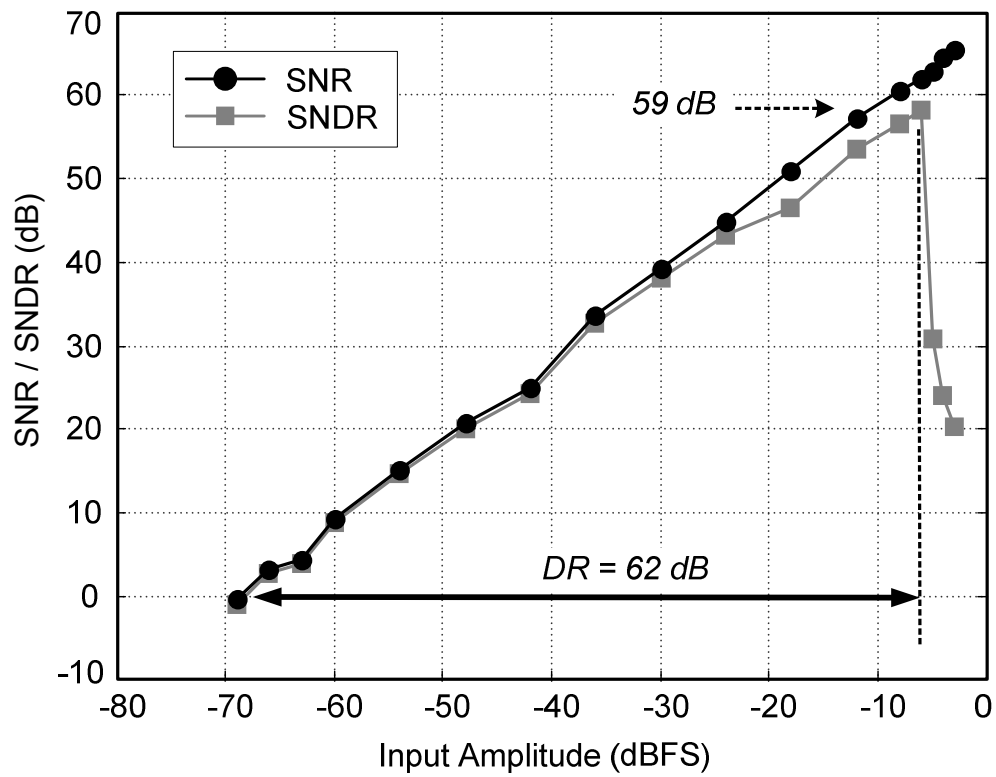
Figure 4.24: Measured SNR/SNDR characteristic of the 1ˢᵗ-order modulator.

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Table 4.1: Performance Summary.

Clock Frequency		184.32 MHz	
Signal Bandwidth		1.92 MHz	
Full Scale Range		+/- 300 mV (differential)	
Peak SNDR		59 dB (at -6dBFS)	
Peak SNR		65 dB (at -3 dBFS)	
Overload Level		-6 dBFS	
In-Band Noise Power (Idle Mode)		-69 dBFS	
Dynamic Range		62 dB = 10 ENOB	
Power Consumption	Analog	2.1 mW	Total = 3.1 mW
	Digital	1.0 mW	(VDD = 1.2 V)
Fabrication Process		130nm 1P8M RF CMOS	
Chip Area (Excluding Pads)		600 μm $\times$ 600 μm (0.36 mm^2)	
FOM*		0.788 pJ/conversion	

* FOM=Power / (2$^.$ BW$^.$2^{ENOB})

The measured current consumptions are 1.75 mA for the analog and 2.5mA for the digital, including the DLL. Post-layout simulations indicate that the DLL's current consumption is 1.67 mA. Hence, the modulator by itself draws 830 μA from the 1.2 V digital supply. Therefore, the modulator consumes 2.1 mW analog power and 1.0 mW digital power, amounting to 3.1 mW total power consumption. This represents a figure - of-merit (FOM) of 0.788 pJ/conversion. The measurement results are summarized in Table 4.1.

4.3 Summary

This chapter presented a CT-$\Delta\Sigma$-modulator architecture based on using delay compensated SAR quantization. Also the design and implementation of a first-order modulator with a 5-bit SAR was presented that uses on-chip frequency multiplier to generate the required high-frequency timing clock. The modulator achieves 62 dB dynamic range over 1.92 MHz signal bandwidth which is 6 dB less than the 68 dB simulated dynamic range. The difference was attributed to the extra mismatch among the vertical metal-metal capacitors of the delay compensating DAC and the SAR quantizer as well as the timing errors contributed by the DLL. The implemented modulator draws 3.1 mW power from a 1.2 V supply and occupies 0.36 mm^2 of die area. The implementation proves the feasibility of high-performance CT-$\Delta\Sigma$-modulators based on high-speed SAR-quantizers. The use of SAR-quantizers with resolutions over 4 bits becomes particularly advantageous in higher-order modulators where finer quantization can be leveraged to design $\Delta\Sigma$-modulators with more aggressive noise transfer functions.

CHAPTER 5

ROBUST STF MODULATOR ARCHITECTURES

Reconfigurable CT-$\Delta\Sigma$ modulators for multi-mode receiver applications that demand higher levels of interference tolerance have recently received increasing attention [14], [55-57]. Switching between different modes in these A/D converters often demands complex and reconfigurable feedback D/A converters that tend to be bulky. As such, multi-bit CT-$\Delta\Sigma$-modulators are often implemented using the feedforward topology which uses a single feedback path. However a typical feedforward CT-$\Delta\Sigma$ modulator shows an undesirable out-of-band peaking in the Signal-Transfer-Function (STF) [41]. This drawback is particularly troublesome in wireless applications where, in the presence of strong out-of-band blockers, any peaking in STF translates into a reduction in dynamic range. Furthermore, feedforward CT-$\Delta\Sigma$ modulators exhibit significantly lower anti-aliasing than feedback modulators. The solution proposed in [58] aims to tackle the STF peaking problem by means of a passive RC low-pass filter in the forward path and an active high-pass filter in the feedback path of the modulator. In addition to the need for an extra amplifier, this method trades the Noise Transfer Function (NTF) of the modulator versus its STF. In this chapter we will propose two new CT-$\Delta\Sigma$ modulator topologies; one with dual feed-in and another with dual feedback that both allow for implementing a low-pass STF without constraining the NTF.

In the following sections we will first show how a conventional feedforward modulator can be modified to avoid peaking in its STF. Then, we will compare the robustness of the proposed dual feed-in and the dual feedback structures versus the peaking-free feedforward modulator. Finally, we will show the design, implementation

and measurement results of a third-order, 4-bit dual-feedback modulator that achieves 76 dB of dynamic range over 5 MHz signal bandwidth while providing 70 dB of anti-aliasing and a peaking-free STF.

5.1 STF Behavior in CT-$\Delta\Sigma$

Figures 5.1(a) and (b) respectively show the well known feedback and feedforward CT-$\Delta\Sigma$ modulator architectures [8]. Third-order systems have been chosen merely as an example. In general, both topologies need N continuous-time integrators (i.e., $N=3$) for N-th order noise shaping while local resonant feedback paths $g_1...g_M$ ($M \leq N/2$) are used for optimal placement of the zeros of the noise transfer function (NTF). The feedback architecture can include $N+1$ feed-in paths $b_1... b_{N+1}$, and it needs $N+1$ feedback paths $a_1... a_{N+1}$, where the last feedback is used for excess-loop-delay (ELD) compensation [21]. The feedback architecture is commonly implemented with $b_1=a_1$ and $b_2...b_{N+1}=0$ [59] which results in a low-pass STF with no out-of-band peaking, as shown in Figure 5.2. The price paid for this desirable characteristic is an increase in integrator output swings due to the addition of the feedback signal to all internal nodes. This implies that low-gain integrators with large integration capacitors are required to avoid clipping. Using extra feed-in paths b_i ($i=2... N+1$) reduces the signal swings at the integrator outputs, but it causes an unwanted STF peaking similar to a feedforward structure. In principal, the feedforward architecture requires only one overall feedback path. Low-swing feedforward architectures often use a direct feed-in path $b_{N+1}=b_1$ to make the voltage swings inside the loop filter smaller and less
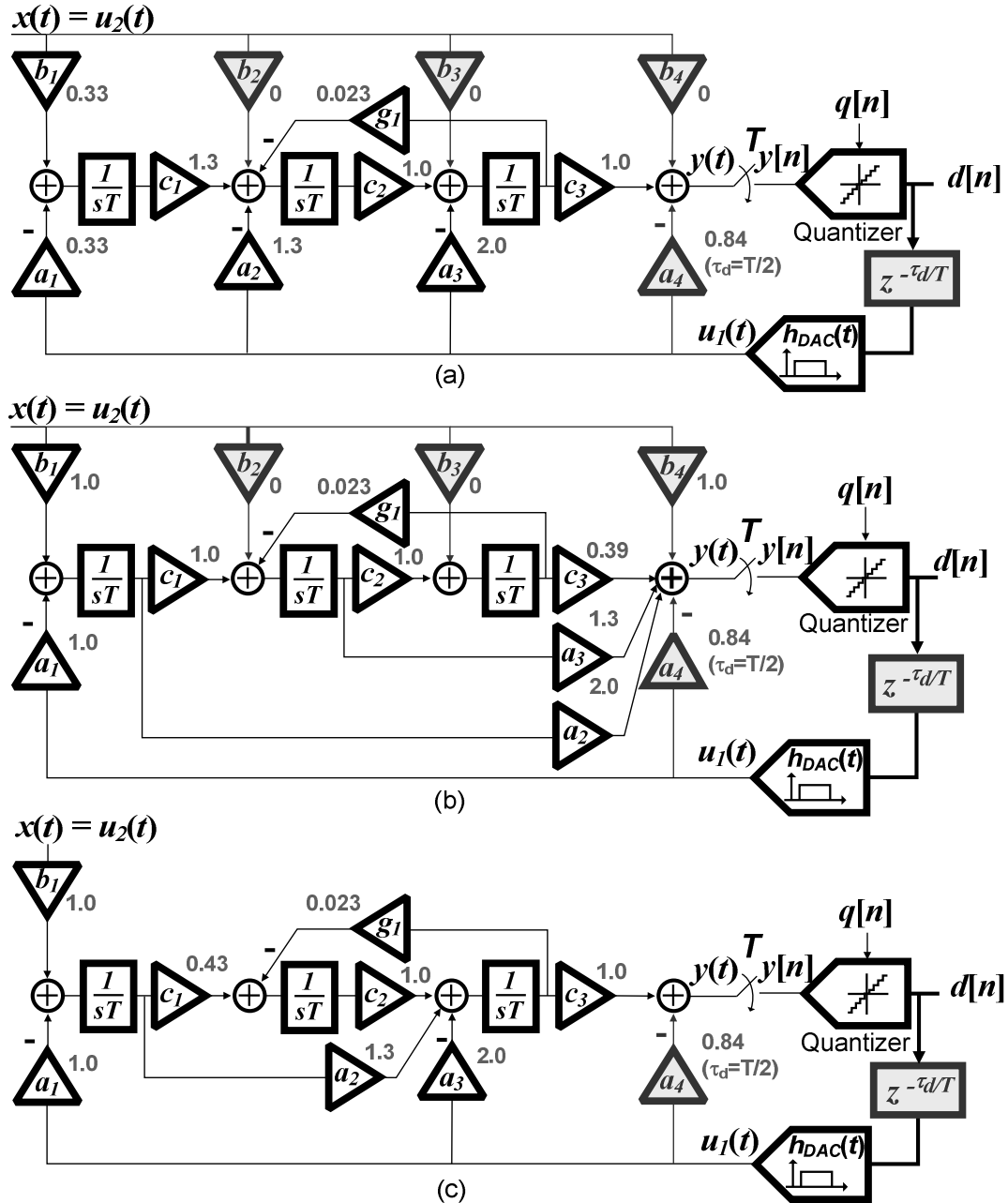
Figure 5.1: Prior art: (a) Third order feedback (b) feed-forward and (c) feedback-feedforward CT-$\Delta\Sigma$ modulator architectures.

dependent on the input signal [60]. The remaining feed-in coefficients i.e., $b_2...b_N$ (shown in gray) are typically zero. The price paid for lower voltage swings in a feedforward modulator is an unwanted STF out-of-band peaking and reduced anti-aliasing. As a compromise between integrator swings and STF filtering, a combination
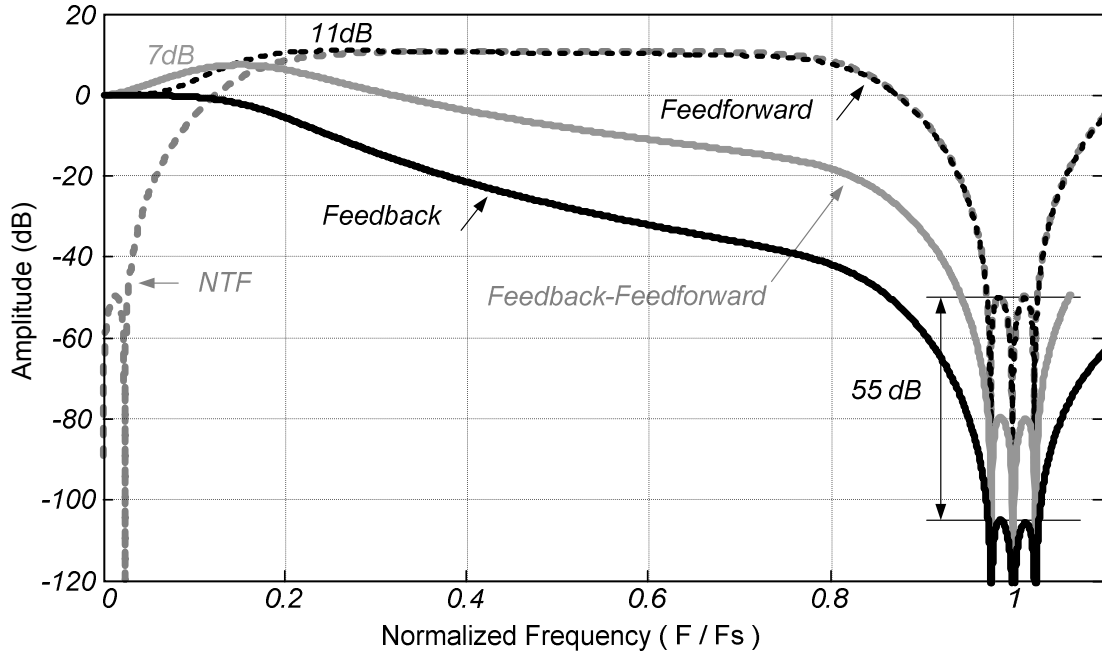
Figure 5.2: A third order NTF shown with STF's of feedback, feedforward, and feedback-feedforward CT ΔΣ topologies.

of feedback and feedforward topologies has been proposed in [61]. This structure as shown in Figure 5.1(c) improves the anti-aliasing, but does not fully eliminate the STF peaking.

The STF of feedback, feedforward and combined feedback-feedforward architectures is shown in Figure 5.2 for comparison, assuming all have identical NTF. The corresponding coefficients are included in Figure 5.1. The STF of the feedforward modulator shows significantly less anti-aliasing filtering than the other two architectures. It also shows 11dB of STF out-of-band peaking. This extra gain may lead to clipping and system overload if strong out-of-band signals are present at the input. The STF of the structure in Figure 5.3(c) provides 30 dB more anti-aliasing than the feedforward and shows 5dB less STF peaking, however, the peaking starts at a lower frequency. The feedback modulator shows the best STF without any peaking and with

monotonic roll-off that can be leveraged to simplify the base-band filter design in a receiver application. It also provides 55 dB more anti-aliasing than the low-swing feedforward structure.

In wireless applications, peaking in the STF of the CT-ΔΣ modulators can effectively degrade the dynamic range of the receiver. This dynamic range penalty due to STF peaking can potentially outweigh the merits of the low-swing architectures.

5.1.1 STF Analysis

In a CT-ΔΣ-modulator the signal is filtered by the loop filter before being sampled by the quantizer. This provides inherent anti-aliasing which is well documented in the literature [17], [62]. In any single-loop modulator, including those shown in Figure 6.1, two transfer functions can be identified within the modulator. The feedback path transfer function from DAC output $u_1(t)$ to the sampler input $y(t)$ defined as

$$LF(s) = \frac{Y(s)}{U_1(s)}\bigg|_{U_2(s)=0} \tag{5.1}$$

and the forward path transfer function from the modulator input $u_2(t)$ to the sampler input $y(t)$ defined as

$$FF(s) = \frac{Y(s)}{U_2(s)}\bigg|_{U_1(s)=0} \tag{5.2}$$

Figure 5.3(a) shows the linearized model of a CT-DS modulator which includes the transfer functions defined in (5.1) and (5.2). The feedback path transfer functions define the noise- shaping of the modulator. This becomes clear if we replace the CT loop-filter

(a)

(b)
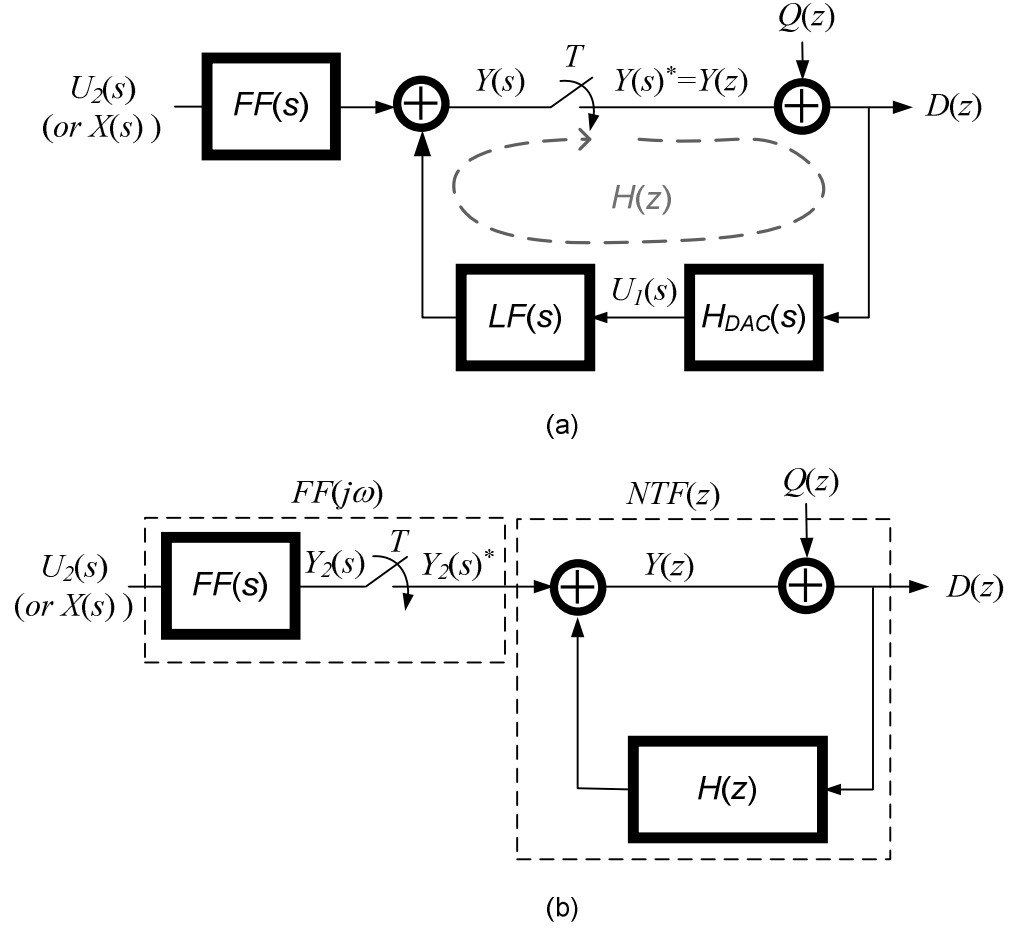
Figure 5.3: (a) Linearized model of a CT $\Delta\Sigma$ modulator, (b) Linearized model with the inner loop replaced by the DT equivalent loop-filter H(z).

with an equivalent discrete-time loop transfer function $H(z)$ as shown in Figure 5.3(b).

Using this model the loop filter $H(z)$ can be related to noise transfer function as

$$NTF(z) = \frac{1}{1 - H(z)} \qquad (5.3)$$

Since the input of the CT loop filter is a series of DT impulses, the Impulse-invariant-transformation is commonly used to map $LF(s)$ to $H(z)$ [17], [63-64]

$$H(z) = \mathcal{Z}\left\{\mathcal{L}^{-1}\left\{LF(s) \cdot H_{DAC}(s) \cdot e^{-s\tau_d}\right\}\big|_{t=nT}\right\} \qquad (5.4)$$

where $Z\{.\}$ and $L^{-1}\{.\}$, respectively, denote the Z and the inverse Laplace transforms, τ_d
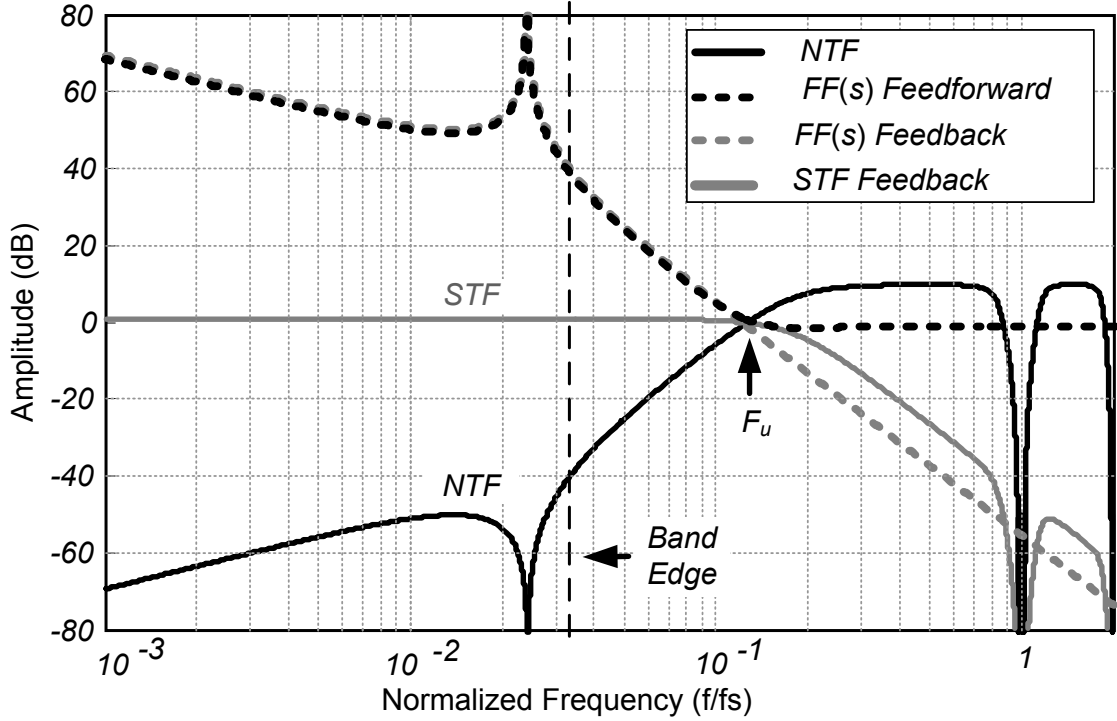
Figure 5.4: STF and NTF of a sample third-order CT ΔΣ modulator shown with the pre-filtering TF, FF(s). The FF(s) of a low-swing feed-forward modulator is shown for comparison.

is the excess-loop-delay and $H_{DAC}(s)$ is the Laplace transform of the DAC waveform. It is noted that the $H_{DAC}(s)$ in (5.4) indicates that the shape of the feedback signal needs to be taken into account. This can be achieved using the pre-computed mapping tables for return-to-zero (RZ) and no-return-to-zero (NRZ) DAC waveforms [17], [20] or through the generalized method described in [50].

Also using Figure 5.3(b), the Signal Transfer Function (STF) from the CT input $u_2(t)$ to the DT output $d[n]$ can be expressed in terms of the modulator NTF and the forward path filter $FF(s)$ as [65]

$$STF(j\omega) = FF(j\omega)NTF(e^{j\omega T}) \tag{5.5}$$

Equation (5.5) is plotted in Figure 5.4 for a third-order low-pass ΔΣ modulator with

over-sampling-ratio (OSR) of 16. The forward path transfer function is shown for conventional feedback and low-swing feedforward modulators. The $FF(s)$ of the conventional feedback modulator of Figure 5.1(a) is a third-order all-pole transfer function which is obtained in terms of the modulator's coefficients as

$$FF(s)_{FBK} = \frac{b_1 c_1 c_2 c_3}{s(s^2 + g_1 c_2)}$$
(5.6)

Also, from Figure 5.1(b) the pre-filtering of the low-swing feedforward topology with $b1=b4$ and $b_2=b_3 = 0$ is :

$$FF(s)_{FFW} = \frac{b_1[s^3 + a_2 s^2 + (c_2 g_1 + a_3 c_1)s + c_2(a_2 g_1 + c_3 c_1)]}{s(s^2 + g_1 c_2)}$$
(5.7)

A normalized sampling period of $T=1$ is used in deriving (5.6) and (5.7) for the sake of simplicity.

It is seen that the transfer functions $FF(s)$ in both feedback and feedforward structures have identical denominators. The poles of $FF(s)$ always coincide with the zeros of $NTF(z)$ and cancel out each other. In this example, the sole pole of $FF(s)$ at DC corresponds to a zero in the NTF at DC and the conjugate imaginary poles of $FF(s)$ at $\pm j\sqrt{g_1 c_2}$ correspond to the NTF's conjugate zeros on the unit circle. As a result, the STF exhibits a flat in-band frequency response. On the other hand, the difference between feedback and feedforward structures lies in the numerator of $FF(s)$. According to (5.7) the transfer function $FF(s)$ of the low-swing feedforward modulator has three zeros and its high frequency gain approaches b_1 ($b_1=1$ in the graph of Figure 5.3). These zeros limit the high frequency role-off of $FF(s)$, and when combined with the NTF's out-of-band gain, they cause the STF to exhibit out-of-band peaking. In order to show

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the effect of the zeros, the *FF*(*s*) of the feedback-feedforward modulator in Figure 5.1(c) is obtained as

$$FF(s)_{FBK-FF} = \frac{b_1 a_2 c_3 s + b_1 c_1 c_2 c_3}{s(s^2 + g_1 c_2)} \tag{5.8}$$

Clearly in (5.8) the order of the numerator of *FF*(*s*) is reduced compared to (5.7) which results in improved STF anti-aliasing and reduced peaking. The STF peaking, shown in Figure 5.2, arises from the non-zero first-order term in (5.8) which can not be canceled in this specific architecture.

For an STF with unity in-band gain, the magnitude of *FF*(*s*) at low frequencies is the inverse of the magnitude of *NTF*(*z*). Figure 5.5 indicates that this relationship holds up to F_u where the magnitude of NTF crosses 0 dB. Beyond this point, the NTF shows an out-of-band gain which depends on the aggressiveness of noise shaping. A higher SQNR corresponds to a more aggressive noise shaping with a larger maximum out-of-band gain which can eventually translate into a larger peaking in the STF of the low-swing feedforward or feedback-feedforward modulators.

The relationship between the NTF unity-gain frequency F_u and the oversampling ratio (OSR) is plotted in Figure 5.4 for different modulator orders. F_u is normalized to the signal bandwidth F_b to show the relative location of the NTF unity-gain frequency with respect to the band edge. It is assumed that all the NTFs are Chebyshev type-II with optimized zeros [8], [66] and have 10 dB of maximum out-of-band gain. Increasing the order of the modulator or decreasing the OSR pushes the unity frequency F_u closer to the signal band. Therefore, high dynamic range and low-OSR modulators using the low-swing feedforward topology tend to cause a more serious STF
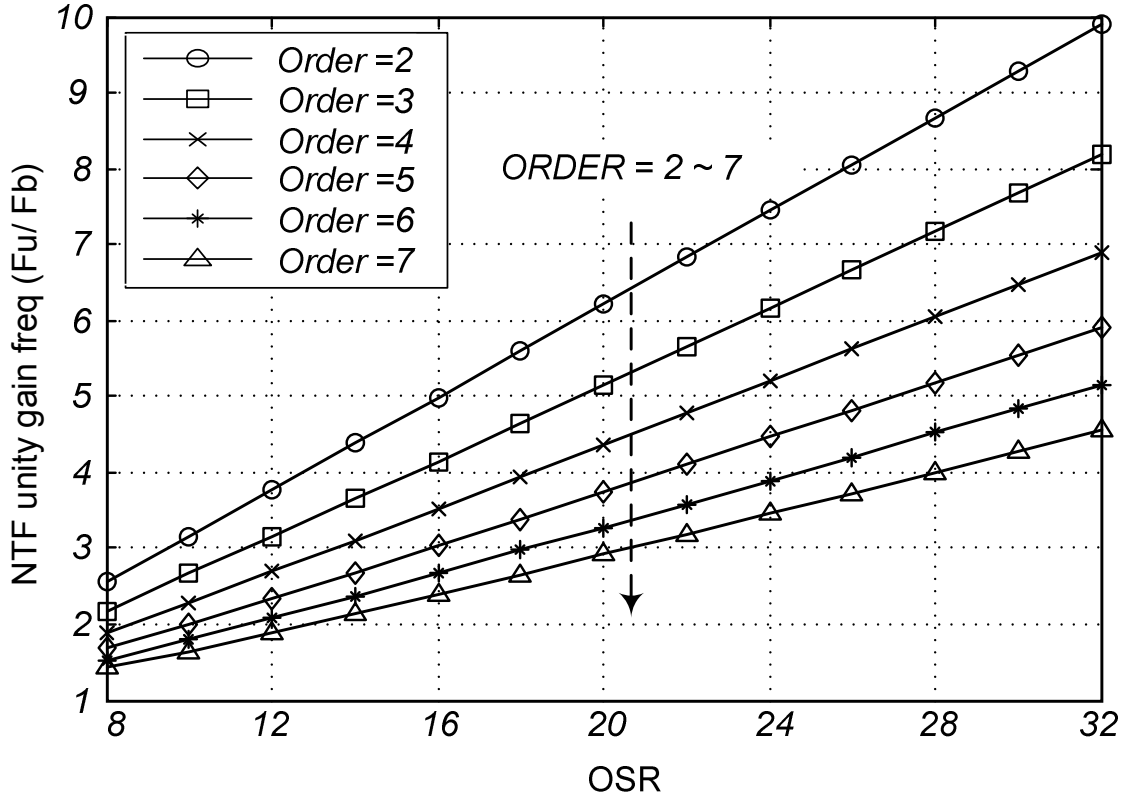
Figure 5.5: NTF unity gain frequency normalized to signal bandwidth F_b, versus OSR for different modulator orders.

peaking problem. In wireless applications, close-in peaking in the STF would require more front-end filtering to prevent a strong adjacent or next channel interferer from saturating the modulator. In contrast, equation (5.6) indicates that $FF(s)$ in the case of the feedback modulator is an all-pole transfer function. This interesting property stems from the fact that there exists a single path between the input and the output of the modulator. The magnitude of $FF_{FBK}(s)$ keeps rolling off as frequency increases. Consequently, not only does the STF become free of peaking, but it achieves 55 dB of additional anti-aliasing near the sampling frequency F_s. In summary, comparing equations (5.6), (5.7) and (5.8) reveals that the key to a peaking-free STF is to make the forward path transfer function $FF(s)$ an all-pole filter.

5.1.2 Design Methodology for Peaking-Free STF

Most design methodologies discussed in the literature aim to synthesize a CT loop filter with a single input path (b_1) which, upon discretization, realizes a desired prototype $NTF(z)$ [20], [50], [63-64]. Since all the coefficients of the system are derived uniquely to achieve a certain NTF, the STF becomes merely a by-product of the design process with no control upon it. In what follows, we discuss a design methodology in which the NTF and the all-pole $FF(s)$ of a CT-$\Delta\Sigma$ modulator are simultaneously synthesized so that a peaking free low-pass STF is obtained. To this end, we consider an Nth-order feedforward modulator similar to the one shown in Figure 5.1(b) with non-zero feed-in coefficients b_2, b_3, ... b_N in addition to the input path gain b_1. The extra feed-in coefficients provide the additional degree of freedom necessary to eliminate peaking in the STF. The first step in the design process is to select an NTF and then apply (4) to obtain the corresponding DT loop filter $H(z)$. The next step is to synthesize a CT loop filter $LF(s)$ which upon time-discretization, described by equation (5.3), will equate $H(z)$. This computation can readily be performed for an NRZ DAC using the 'd2c' function of MATLAB Control Toolbox [67]. Doing so, we obtain a CT loop filter in the numerical form as

$$\widehat{LF}(s) = \frac{-N_1(s)}{D(s)} = \frac{-(\beta_{N-1}s^{N-1} + ... + \beta_1 s + \beta_0)}{s^N + \alpha_{N-1}s^{N-1} + ... + \alpha_1 s + \alpha_0} \tag{5.9}$$

A powerful method to derive the transfer functions $FF(s)$ and $LF(s)$ is the state-space formulation [68]. In this method the eigenvalues of the state matrix of the system are unique. Thus the transfer functions $FF(s)$ and $LF(s)$ necessarily have identical denominators denoted by $D(s)$ in (5.9). On the other hand, the numerator of $FF(s)$ can

generally be a polynomial of the same order as $D(s)$. Therefore, the general form of the feedforward filter $FF(s)$ can be written as

$$\widehat{FF}(s) = \frac{N_2(s)}{D(s)} = \frac{\gamma_N s^N + \gamma_{N-1} s^{N-1} + \dots + \gamma_1 s + \gamma_0}{s^N + \alpha_{N-1} s^{N-1} + \dots + \alpha_1 s + \alpha_0} \qquad (5.10)$$

In the previous section, it was mentioned that the key for avoiding peaking in the STF and achieving a monotonic roll-off is an all-pole $FF(s)$. This requires all the terms in the numerator of $FF(s)$ except γ_0, to be zero; i.e.,

$$\gamma_N = \gamma_{N-1} = \dots = \gamma_1 = 0 \qquad (5.11)$$

It should be emphasized that the goal here is to eliminate the zeros of $FF(s)$ by nulling out the non-constant terms in (5.10) rather than pole-zero cancellation. The value of γ_0 can be linked to the DC gain of the STF. To this end, we note that at low frequencies the DT loop filter $H(z)$ approaches the CT loop filter $LF(s)$ such that at DC they become identical. Therefore, replacing $H(z)$ with $LF(s)$ in (5.4) and substituting the result into (5.5) yields

$$STF(s) \overset{s \to 0}{\approx} \frac{FF(s)}{1 - LF(s)} \qquad (5.12)$$

Using (5.9) and (5.10) in the above equation, the condition for 0 dB DC gain is derived as

$$\lim_{s \to 0} \frac{N_2(s)}{N_1(s) + D(s)} = 1 \qquad (5.13)$$

This condition leads to the following equation for γ_0

$$\gamma_0 = \beta_0 + \alpha_0 \qquad (5.14)$$

In order to calculate the modulator coefficients, we need to obtain the parametric transfer functions $LF(s)$ and $FF(s)$ in terms of the unknown coefficients of the CT modulator. The state-space equations of the system are written as

$$\begin{cases} \dot{x} = \mathbf{A}x + \mathbf{B}[U_1 \quad U_2]^T \\ Y = \mathbf{C}x + \mathbf{D}[U_1 \quad U_2]^T \end{cases} \tag{5.15}$$

where each state x corresponds to an integrator output, Y is the input of the sampler, U_1 is the D/A converter output and U_2 is the modulator input. The parametric transfer functions corresponding to the U_1 and U_2 inputs are defined as

$$\mathbf{G}(s) = \left[\frac{Y(s)}{U_1(s)} \quad \frac{Y(s)}{U_2(s)} \right]^T \tag{5.16}$$

where $\mathbf{G}(s)$ is given by the following equation

$$\mathbf{G}(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D} \tag{5.17}$$

The parametric transfer functions $LF(s)$ and $FF(s)$ are respectively derived from the first and second rows of $\mathbf{G}(s)$ computed in (5.17). Subsequently a system of non-linear equations is constituted by equating the parametric transfer functions with $\widehat{LF}(s)$ in (5.9) and $\widehat{FF}(s)$ in (5.10), and adding the constraints (5.11) and (5.14). Solving this system of equations eventually provides the numerical values of all the coefficients. This procedure can easily be programmed in a symbolic analysis software package. The number of equations and the number of unknowns depends on the order of the system and the topology of the modulator. For example an Nth-order feedforward modulator with $N/2$ resonators, for N even, leads to $2N+N/2+1$ equations and $3N+N/2+1$ unknowns. This provides N additional degrees of freedom that can be used to scale the integrator gains and thereby, optimize the voltage swings of the integrators. This step involves system level transient simulations and adjustment of the integrator gains in an iterative process.

One can note that the peaking elimination technique explained so far relies fundamentally on equation (5.11) and allows for computing the modulator coefficients in a way that the non-constant terms in the numerator of *FF*(*s*) are canceled out. As a result, any deviation of the coefficients that violates (5.11) will cause peaking in the STF and also degradation in anti-aliasing. Therefore, the STF of such a feedforward structure is sensitive to random and systematic component variation [69]. This shortfall has been the main motivation here to develop two novel CT-ΔΣ modulator architectures with significantly less STF sensitivity to component variations while preserving some advantages of the conventional feedforward structure.

5.1.3 Lowpass Feeforward Design Example

Suppose that we desire to implement a feedforward CT-ΔΣ modulator with low-pass STF and 89 dB of SQNR at OSR of 16. Assuming a 4-bit quantizer, the following third-order inverse Chebyshev NTF was found to meet the design specification:

$$NTF(z) = \frac{(z-1)(z^2 - 1.977z + 1)}{(z - 0.3474)(z^2 - 0.6295z + 0.2935)}$$

(5.18)

From (5.3) the corresponding DT loop filter is obtained as:

$$H(z) = \frac{2(z^2 - 1.232z + 0.449)}{(z-1)(z^2 - 1.977z + 1)}$$

(5.19)

Using (5.19) and (5.4) and assuming an NRZ DAC waveform and total excess-loop-delay of $\tau_d = T/2$, the DT transfer function *H*(*z*) is mapped to the following CT loop-filter:

$$\widehat{LF}_d(s) = \frac{-(0.8374s^3 + 1.984s^2 + 1.321s + 0.4342)}{s^3 + 0.0231s}$$

(5.20)

According to (5.10), (5.11) and (5.14) the required prefiltering transfer function is

$$\widehat{FF_d}(s) = \frac{0.4342}{s^3 + 0.0231s} \qquad (5.21)$$

For the third-order feedforward topology shown in Figure 5.1(a) the state space matrices of the modulator are

$$\text{feed-forward} \begin{cases} \mathbf{A} = \begin{bmatrix} 0 & 0 & 0 \\ c_1 & 0 & -g_1 \\ 0 & c_2 & 0 \end{bmatrix} & \mathbf{B} = \begin{bmatrix} -a_1 & b_1 \\ 0 & b_2 \\ 0 & b_3 \end{bmatrix} \\ \mathbf{C} = \begin{bmatrix} a_2 & a_3 & c_3 \end{bmatrix} & \mathbf{D} = \begin{bmatrix} -a_4 & b_4 \end{bmatrix} \end{cases} \qquad (5.22)$$

Using (5.16) and (5.17) the parametric transfer functions $LF(s)$ and $FF(s)$ are found as

$$\begin{cases} \dfrac{Y(s)}{U_1(s)} = LF(s) = \dfrac{-(K_3 s^3 + K_2 s^2 + K_1 s + K_0)}{s(s^2 + c_2 g_1)} \\[4mm] \dfrac{Y(s)}{U_2(s)} = FF(s) = \dfrac{L_3 s^3 + L_2 s^2 + L_1 s + L_0}{s(s^2 + c_2 g_1)} \end{cases} \qquad (5.23)$$

The parametric equivalents of K_i and L_j coefficients and the set of equations to be solved are given in Table 5.1. Three additional equations specify the value of the scaling coefficients c_1, c_2, and c_3. These coefficients control the signal swing at the integrator outputs and hence can be used to cope with headroom limitations in a low-voltage design. In this example we iteratively settled on $c_1=0.5$, $c_2=1$ and $c_3=2$ based on behavioral simulations. It should be noted that the choice of these coefficients affects the value of the other coefficients, but does not alter the NTF and STF of the CT modulator. Therefore, we end up with a set of 9 equations and 9 unknowns which once

$$\text{solved yields} \begin{cases} a_1 = 0.39 & a_2 = 5.11 & a_3 = 6.71 & a_4 = 0.84 \\ b_1 = 0.39 & b_2 = -0.58 & b_3 = 0.95 & b_4 = 0 \\ c_1 = 0.5 & c_2 = 1 & c_3 = 2 & g_1 = 0.023 \end{cases}$$

Table 5.1: LF(s) and FF(s) Coefficients of the Feedforward Topology

term	Parametric Equivalent	In (9), (10)	Value
K_3	a_4	β_3	0.8374
K_2	$a_2 a_3$	β_2	1.984
K_1	$a_1 a_3 c_1 + a_4 c_2 g_1$	β_1	1.321
K_0	$a_1 c_2 (c_1 c_3 + a_2 g_1)$	β_0	0.4342
L_3	b_4	γ_3	0
L_2	$b_1 a_2 + b_2 a_3 + b_3 c_3$	γ_2	0
L_1	$b_1 c_1 a_3 + b_2 c_2 c_3 + g_1 (b_4 c_2 - b_3 a_3)$	γ_1	0
L_0	$b_1 (c_1 c_2 c_3 + a_2 c_2 g_1)$	γ_0	0.4342
---	$c_2 g_1$	α_1	0.0231

5.1.4 Effect of Random Coefficient Mismatch

Coefficient values in a CT-ΔΣ-modulator can exhibit large variations due to the dependence on the absolute values of two different components like R and C, or G_m and C in the case of active-RC or G_m-C implementations, respectively. To avoid instability caused by excessive component variations, CT-ΔΣ modulators usually employ on-chip tuning to keep the coefficients close to their nominal values [70]. Nonetheless, random coefficient mismatch can still persist and affect the modulator transfer functions.

In the previous section the methodology for implementing a low-pass STF by way of coefficient cancellation was explained. In the case of the feedforward topology, like in the design example, extra feed-in paths were employed to null out the non constant terms of the $FF(s)$ numerator, L_1 to L_N . However such all-pole-made $FF(s)$ will still carry an inherent numerator order of N in an N-*th* order modulator. Consequently any deviation of the coefficients from their nominal values can uncover
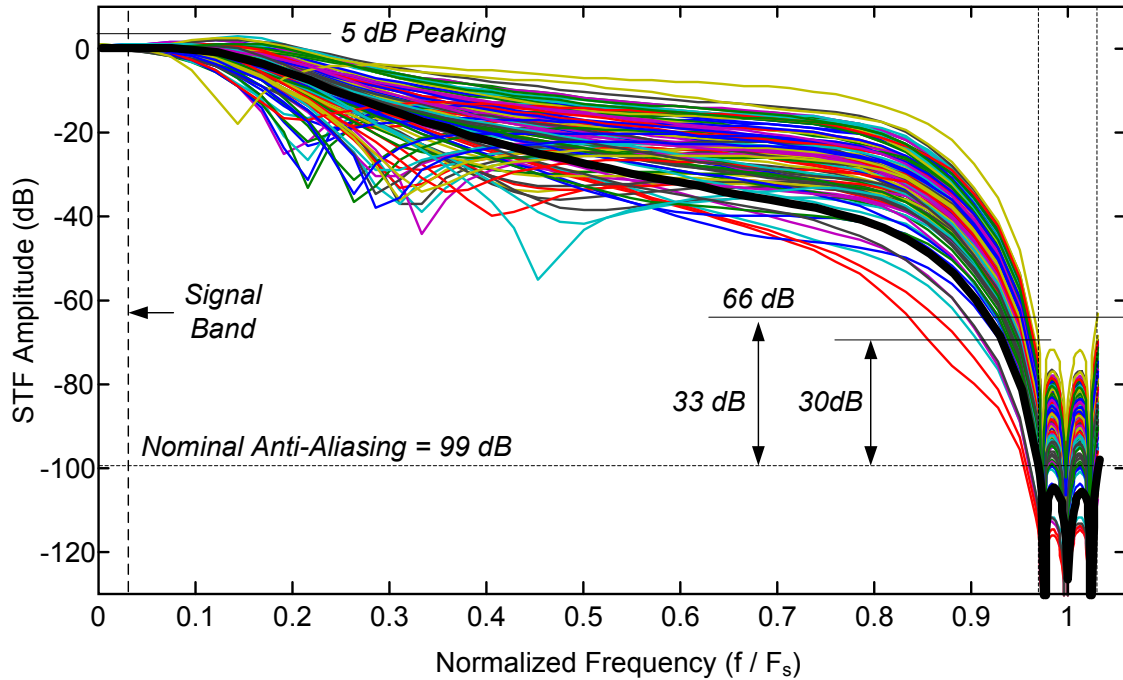
Figure 5.6: Monte-Carlo simulation results showing the effect of 2% mismatch ($\sigma = 0.02$) on the STF of a 3rd-order feedforward CT-$\Delta\Sigma$ modulator.

the hidden zeros of the *FF(s)* and cause significant variability in the STF magnitude response.

Figure 5.6 shows the results of a Monte-Carlo simulation with 1000 runs performed on the feedforward modulator of the design example when the mismatch standard deviation (σ) is 2% . The mismatch effect is manifested as unwanted STF peaking at low frequencies and degraded anti-aliasing in the vicinity of the sampling frequency. In the 1000 runs performed, the maximum deviation from the 99 dB nominal anti-aliasing was 30 and 33 dB at the low and high sides of the alias-band respectively. Also the largest out-of-band peaking was 5 dB across the runs.

More information about the mismatch effect can be extracted from individual histograms of amplitude variation at each frequency point. Considering the 2%
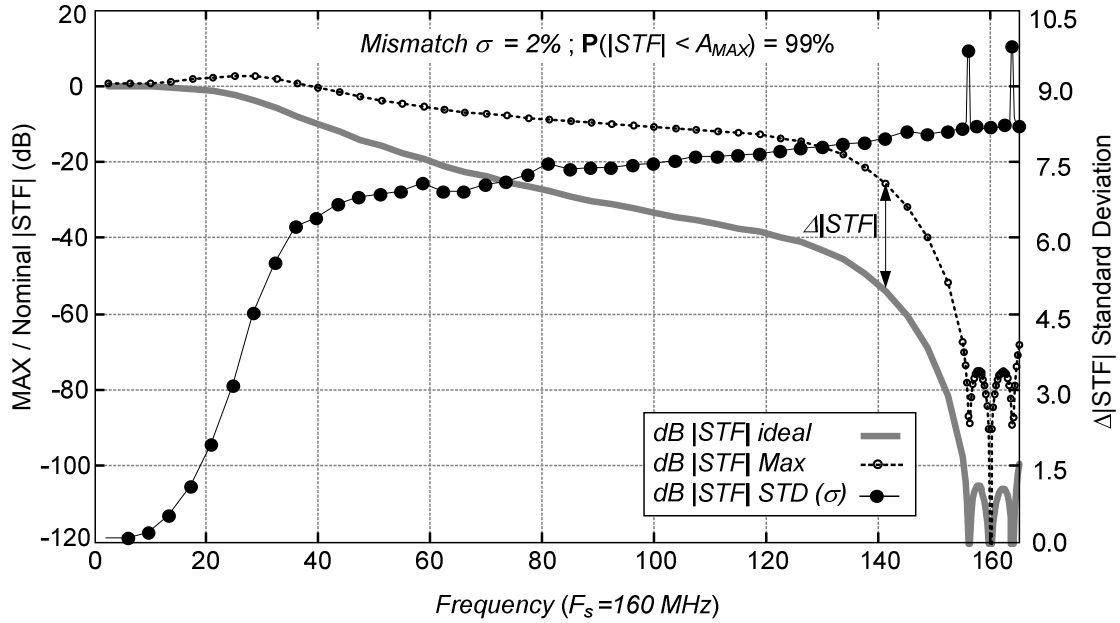
Figure 5.7: Nominal & Maximum (99% probability) STF amplitude (Right Axis); and STF amplitude standard deviation (Left Axis) for 2% mismatch.
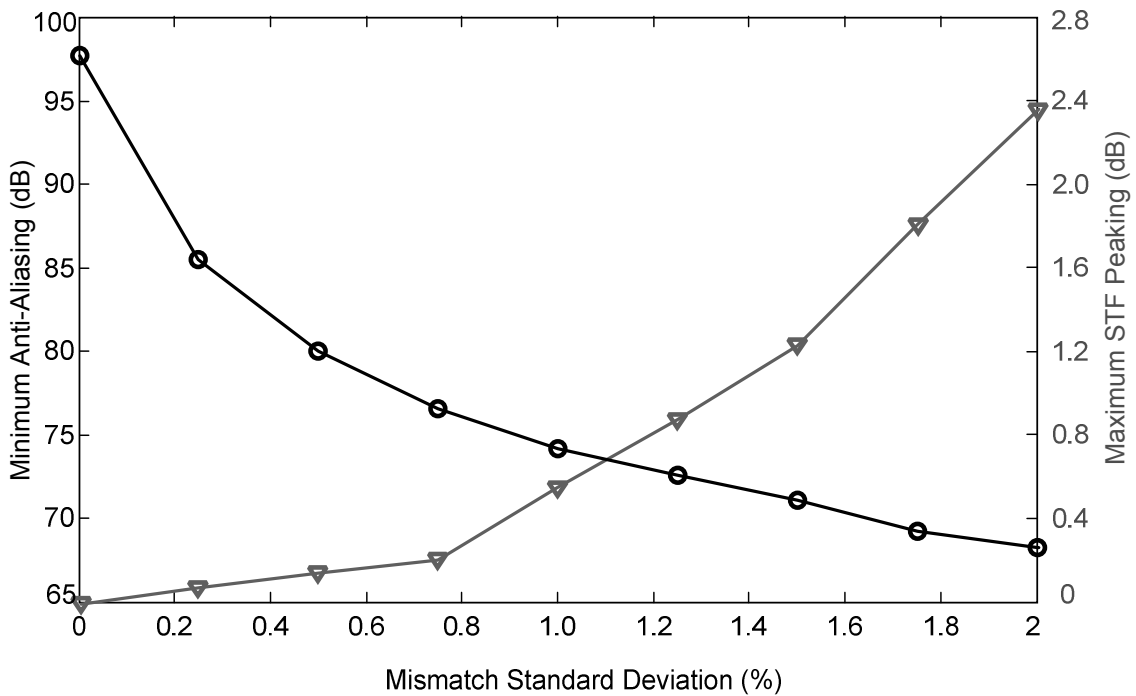
Figure 5.8: Worst-case (with 99% certainty) STF peaking and anti-aliasing versus coefficient mismatch in the 3rd-order feedforward modulator.

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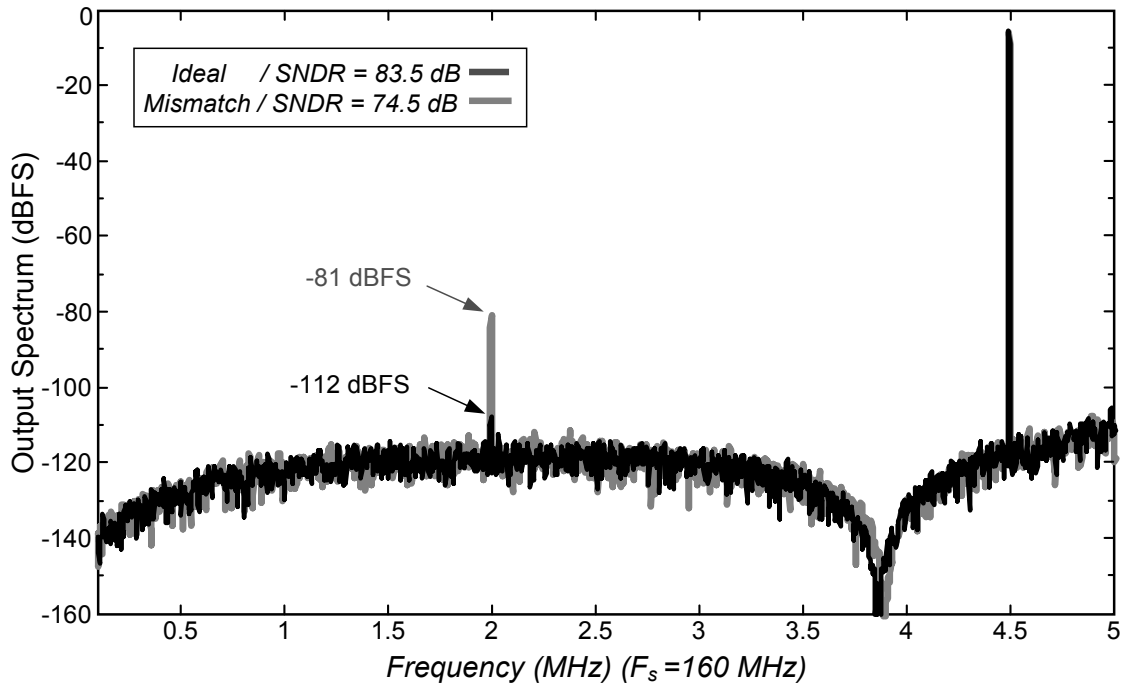
Figure 5.9: Output spectrum of a low-pass STF feedforward modulator in presence of 2% coefficient mismatch.

mismatch case, a compilation is provided in Figure 5.7 which shows the maximum STF amplitude (with $\mathbf{P}(|STF| < A_{MAX}) = 99\%$) and the standard deviation of dB-magnitude variations. With 99% certainty, the STF anti-aliasing and out-of-band peaking are no more than 69.5 dB and 2.2 dB respectively when coefficient mismatch is 2% . Similar data is shown in Figure 5.8 when mismatch standard deviation is varied from 0 to 2% . According to these results the STF of the feeforward topology shows strong sensitivity to the random mismatch and can be degraded by 24 to 44 dB for the anti-aliasing and by 1 to 11 dB for the out-of-band peaking when mismatch is varied from 1% to 10% .

A worst-case scenario output spectrum of the 3rd-order feedforward modulator is shown in Figure 5.9 when STF is affected by the 2% mismatch and anti-aliasing is maximally degraded. The input signal comprises two -6 dBFS tones at 4.5 MHz and 162

MHz and the sampling frequency is 160 MHz. The ideal and worst case anti-aliasing at 162 MHz are 106 dB and 76 dB according to Figure 5.7 data. Hence the down converted alias tone at 2 MHz is 30 dB stronger when mismatch is present, degrading the SNDR from 81 dB to 74.5 dB.

In multi-standard transceiver applications, unless higher-order prefiltering is in place, the alias band of the CT-$\Delta\Sigma$ modulator can include strong tones. Immunity against these tones requires a peaking free STF with robust anti-aliasing. However the conventional feedforward topology is prone to sever anti-aliasing degradation by random variations of the coefficients and even a small mismatch as 1% can degrade anti-aliasing by more than 20 dB (see Figure 5.8). It is difficult to achieve better matching levels even with best layout practices. Therefore an ideal topology for receiver applications should have an STF with low sensitivity to mismatch. In the following sections we will introduce two novel architectures that can provide a low-pass STF with reduced sensitivity to component mismatch.

5.2 The Dual-Feedback Architecture

The proposed dual-feedback modulator architecture is depicted in Figure 5.10(a) for the case of a third-order system. This topology provides a low sensitivity STF by using fewer coefficients for the synthesis of an all-pole $FF(s)$ and at the same time reduces the number of inherent zeros in the $FF(s)$ by means of the second feedback path. The dual-feedback idea can easily be extended to the modulators of higher order by creating N-2 feedforward paths $cf_1...cf_{N-2}$ from the output of the first integrator to the input of all subsequent integrators except the second, as shown in Figure 5.10(b) for a
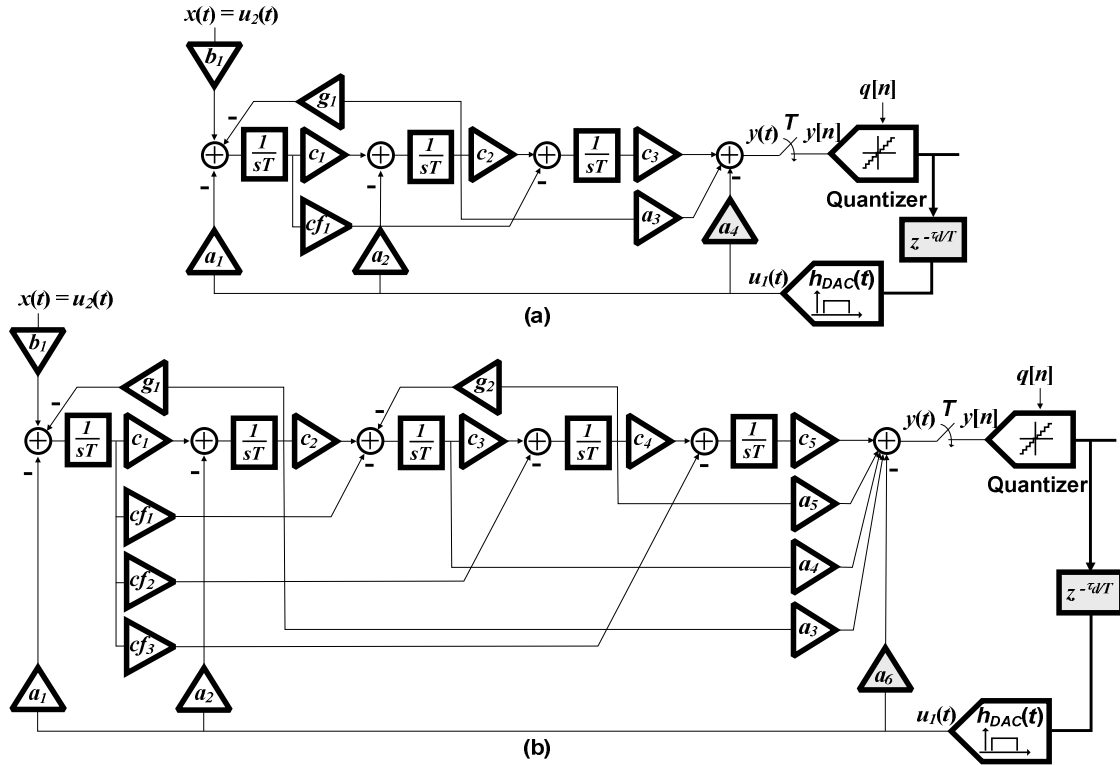
Figure 5.10: The dual-feedback architecture with ELD compensation; (a) a third-order example; (b) a fifth-order example.

fifth-order example. The extra $cf_1...cf_{N-2}$ feedforward paths are essential to the synthesis of an all-pole $FF(s)$. For any order, the modulator requires a single input path and two feedback paths and allows for the synthesis of a robust low-pass STF without compromising the NTF. The second D/A has relaxed noise and linearity requirements since its noise and non-linearity will be first-order shaped by the first integrator. The direct feedback a_{N+1} (i.e. a_4 in Figure 5.10(a)) provides a classical solution for the ELD problem common to all CT modulators using NRZ DACs [21]. The coefficients $c_1...c_N$ are mainly used to scale the output swings of the integrators.

In the third-order dual-feedback modulator of Figure 5.10(a), the state-space matrices of the system are

$$\text{dual-feedback}\begin{cases} \mathbf{A} = \begin{bmatrix} 0 & -g_1 & 0 \\ c_1 & 0 & 0 \\ -cf_1 & c_2 & 0 \end{bmatrix} & \mathbf{B} = \begin{bmatrix} -a_1 & b_1 \\ -a_2 & 0 \\ 0 & 0 \end{bmatrix} \\[2em] \mathbf{C} = \begin{bmatrix} 0 & a_3 & c_3 \end{bmatrix} & \mathbf{D} = \begin{bmatrix} -a_4 & 0 \end{bmatrix} \end{cases} \tag{5.24}$$

Using (16) and (17) the parametric $LF(s)$ and $FF(s)$ transfer functions become

$$\text{dual-feedback}\begin{cases} LF(s) = \dfrac{-(K_3 s^3 + K_2 s^2 + K_1 s + K_0)}{s(s^2 + c_2 g_1)} \\[2em] FF(s) = \dfrac{L_1 s + L_0}{s(s^2 + c_2 g_1)} \end{cases} \tag{5.25}$$

with the parametric equivalents of K_i and L_j given in Table 5.2. The denominators in (5.25) show a DC pole and conjugate imaginary poles at $\pm j\sqrt{g_1 c_1}$. In Figure 5.10(a), the resonant path (i.e., g_1) is built around first and second integrators so that the last integrator can also be used as an analog summer.

In general the numerator order of $FF(s)$ in an N-th order dual-feedback modulator is *N-2*. Thus one can immediately expect lower STF sensitivity compared to a feedforward structure with $FF(s)$ numerator of order N (see (5.7) and (5.23)) .

5.2.1 Dual-Feedback Design Example

Applying the proposed peaking-free STF design methodology to the modulator of Figure 5.10(a), the coefficient values can be computed for the NTF in (5.18). The first few steps involve computing the numerical $FF(s)$ and $LF(s)$ transfer functions and is identical to the feedforward design example in (5.20) and (5.21) respectively. The set of equations to be solved is given in Table 5.2. Three additional equations specify the value of the scaling coefficients c_1, c_2, and c_3. as $c_1 = 0.5$, $c_2 = 1$ and $c_3 = 2$ determined

Table 5.2: LF(s) and FF(s) Coefficients of the Dual-Feedback Topology

term	Parametric Equivalent	In (9), (10)	Value
K_3	a_4	β_3	0.8374
K_2	$a_2 a_3$	β_2	1.984
K_1	$a_1(a_3 c_1 - c_3 cf_1) + a_2 c_2 c_3 + a_4 c_1 g_1$	β_1	1.321
K_0	$a_1 c_1 c_2 c_3 + a_2 g_1 c_3 cf_1$	β_0	0.4342
L_1	$b_1(a_3 c_1 - c_3 cf_1)$	γ_1	0
L_0	$b_1 c_1 c_2 c_3$	γ_0	0.4342
---	$c_1 g_1$	α_1	0.0231

from behavioral simulations. Hence we end up with a set of seven equations and seven

unknowns which once solved yields

$$
\begin{cases}
a_1 = 0.39 & a_2 = 0.65 & a_3 = 3.04 & a_4 = 0.84 \\
b_1 = 0.43 & cf1 = 0.76 & g_1 = 0.05 \\
c_1 = 0.5 & c_2 = 1 & c_3 = 2
\end{cases}
$$

5.3 The Dual Feed-In Architecture

The proposed dual feed-in architecture is shown in Figure 5.11 using third and

fifth order examples. Without compromising the NTF, this topology allows for the

synthesis of an all-pole *FF(s),* and hence a peaking-free low-pass STF, by using only

one extra feed-in path for arbitrary modulator order. Compared to the conventional

feedforward structure, the STF sensitivity to mismatch is slightly lowered due to a

reduction in the number of feed-in paths. Also similar to the dual-feedback case, there

are *N-2* inter- stage feedforward paths marked by *cf$_1$...cf$_{N-2}$* which extend from the

output of the first integrator to the input of all subsequent integrators except the second.
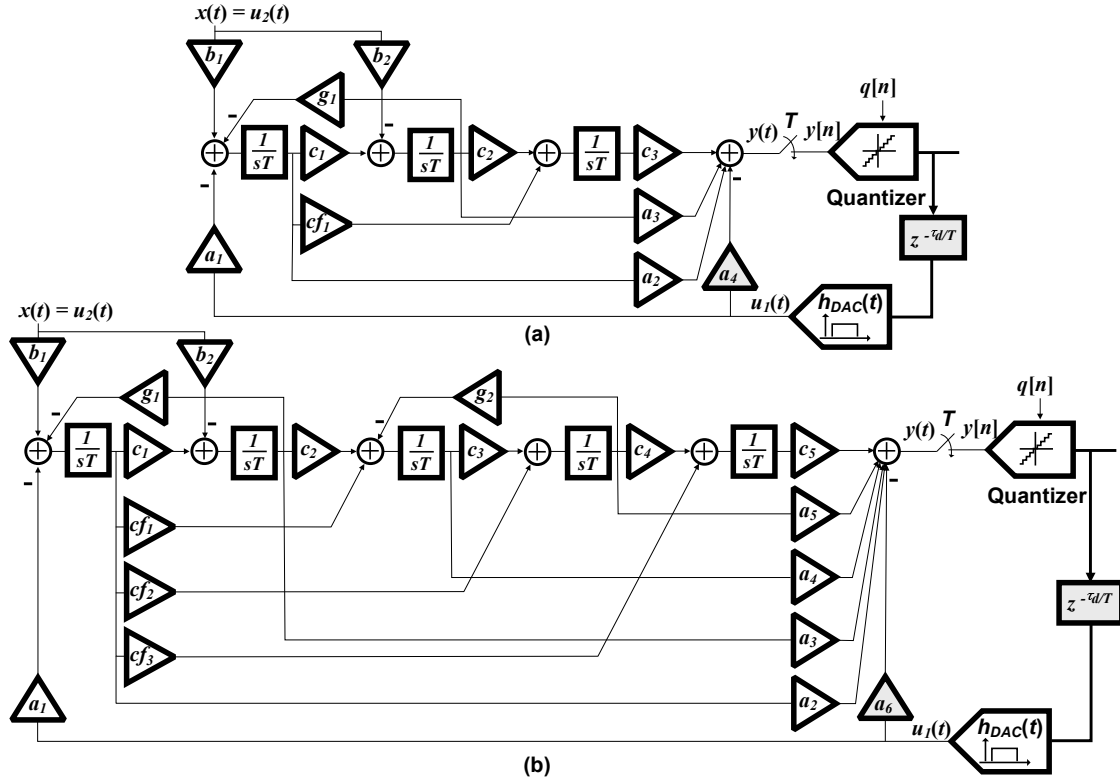
Figure 5.11: The dual feed-in architecture with ELD compensation; (a) a third-order example; (b) a fifth-order example.

The $cf_1...cf_{N-2}$ coefficients along with the second feed-in coefficient b_2 are essential to the synthesis of an all-pole $FF(s)$. Compared to the dual-feedback topology, the feedback is replaced by a feedforward path a_2 that links the fist integrator output to the quantizer input. Needing a single feedback DAC along with the low-pass STF feature makes the architecture an attractive choice for multi-mode and reconfigurable receiver applications. The added noise by the extra feed-in path is negligible due to a first-order noise shaping provided by the first integrator. The direct feedback a_{N+1} (i.e. a_4 in Figure 5.11 (a)) is used for ELD compensation and is common to all CT-$\Delta\Sigma$ architectures. Similar to feedforward and dual-feedback topologies, the $c_1...c_N$ coefficients are used mainly for scaling the output swings of the integrators. In the dual feed-in prototype

Table 5.3: LF(s) and FF(s) Coefficients of the Dual Feed-In Topology

term	Parametric Equivalent	In (9), (10)	Value
K_3	a_4	β_3	0.8374
K_2	$a_1 a_2$	β_2	1.984
K_1	$a_1(a_3 c_1 + c_3 cf_1) + a_4 c_1 g_1$	β_1	1.321
K_0	$a_1 c_1 c_2 c_3$	β_0	0.4342
L_2	$b_1 a_2 - b_2 a_3$	γ_2	0
L_1	$b_1(a_3 c_1 + c_3 cf_1) - b_2(c_2 c_3 - a_2 g_1)$	γ_1	0
L_0	$b_1 c_1 c_2 c_3 + b_2 g_1 c_3 cf_1$	γ_0	0.4342
---	$c_1 g_1$	α_1	0.0231

shown in Figure 5.11(a), the state-space ABCD matrixes of the system are

$$
\text{dual feed-in} \begin{cases} \mathbf{A} = \begin{bmatrix} 0 & -g_1 & 0 \\ c_1 & 0 & 0 \\ cf_1 & c_2 & 0 \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} -a_1 & b_1 \\ 0 & -b_2 \\ 0 & 0 \end{bmatrix} \\ \\ \mathbf{C} = \begin{bmatrix} a_2 & a_3 & c_3 \end{bmatrix} \quad \mathbf{D} = \begin{bmatrix} -a_4 & 0 \end{bmatrix} \end{cases}
\tag{5.26}
$$

Using (5.16) and (5.17) the parametric *LF(s)* and *FF(s)* transfer functions are derived as

$$
\text{dual feed-in} \begin{cases} LF(s) = \dfrac{-(K_3 s^3 + K_2 s^2 + K_1 s + K_0)}{s(s^2 + c_2 g_1)} \\ \\ FF(s) = \dfrac{L_2 s^2 + L_1 s + L_0}{s(s^2 + c_2 g_1)} \end{cases}
\tag{5.27}
$$

The parametric equivalent of K_i and L_j terms is given in Table 5.3. The denominators in (5.27) show a DC pole and conjugate imaginary poles at $\pm j\sqrt{g_1 c_1}$. Also the resonant path through g_1, as shown in Figure 5.11(a), is built around the first and second integrators so that the last integrator can be optionally used as an analog summer.

5.3.1 Dual Feed-In Design Example

Applying the proposed peaking-free STF design methodology to the prototype modulator of Figure 5.11(a), the coefficient values are computed for the NTF in (5.18). The few initial steps until computing the numerical $FF(s)$ and $LF(s)$ transfer functions are identical to the feedforward design example in (5.20) and (5.21), respectively. The set of equations to be solved are listed in Table 5.3. Like the previous design examples, three more equations specify the value of the scaling coefficients c_1, c_2, and c_3. We iteratively settled on $c_1=0.5$, $c_2=1$ and $c_3=2$ based on integrator output swings obtained from behavioral transient simulations. Hence we end up with a set of 8 equations and 8 unknowns which once solved yields

$$\begin{cases} a_1 = 0.434 & a_2 = 4.57 & a_3 = 2.73 & a_4 = 0.84 \\ b_1 = 0.38 & b_2 = 0.65 & g_1 = 0.05 & cf1 = 0.82 \\ c_1 = 0.5 & c_2 = 1 & c_3 = 2 \end{cases}$$

5.4 STF Sensitivity Comparison

In the previous sections we discussed the effect of mismatch on STF peaking and anti-aliasing in a feedforward structure. The dual-feedback and dual feed-in topologies use less feed-in coefficients or have a reduced-order $FF(s)$ numerator, which promises a more robust STF. The Monte-Carlo simulation results in Figure 5.12 provide a comparison of the STF sensitivity among the proposed architectures. Assuming 2% coefficient mismatch and 99% yield ($\mathbf{P}(|STF|{<}x){=}0.99$), Figure 5.12(a) shows the worst-case STF amplitude versus frequency. Careful examination of the STF in the vicinity of the sampling frequency reveals an anti-aliasing degradation of, respectively,
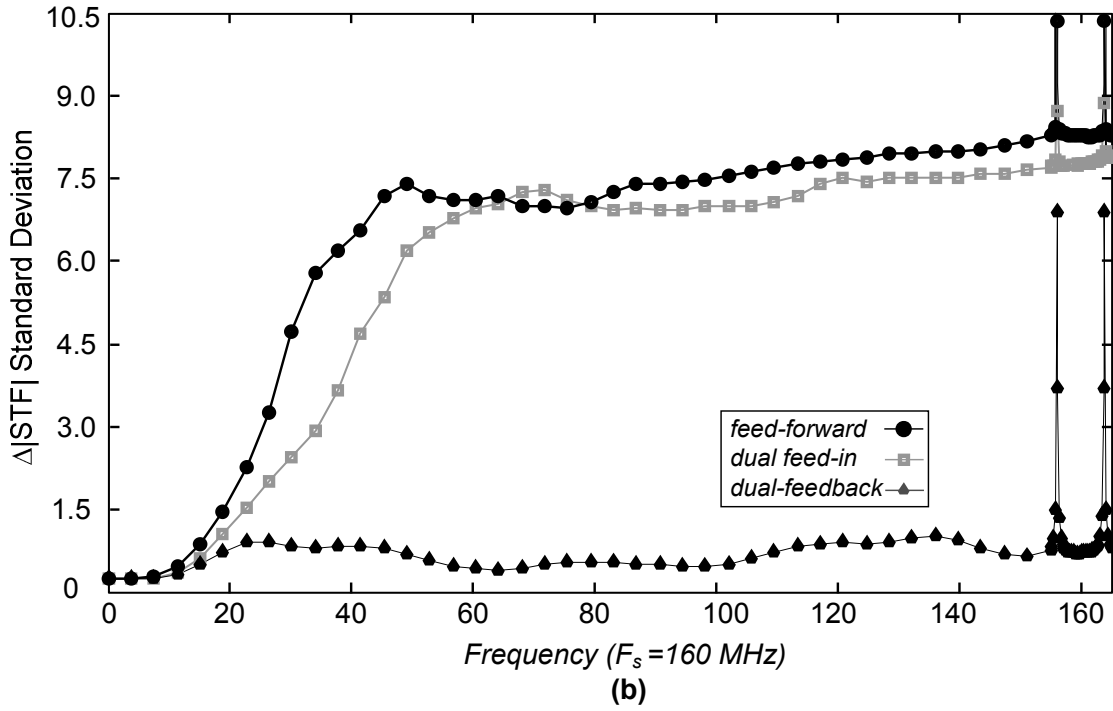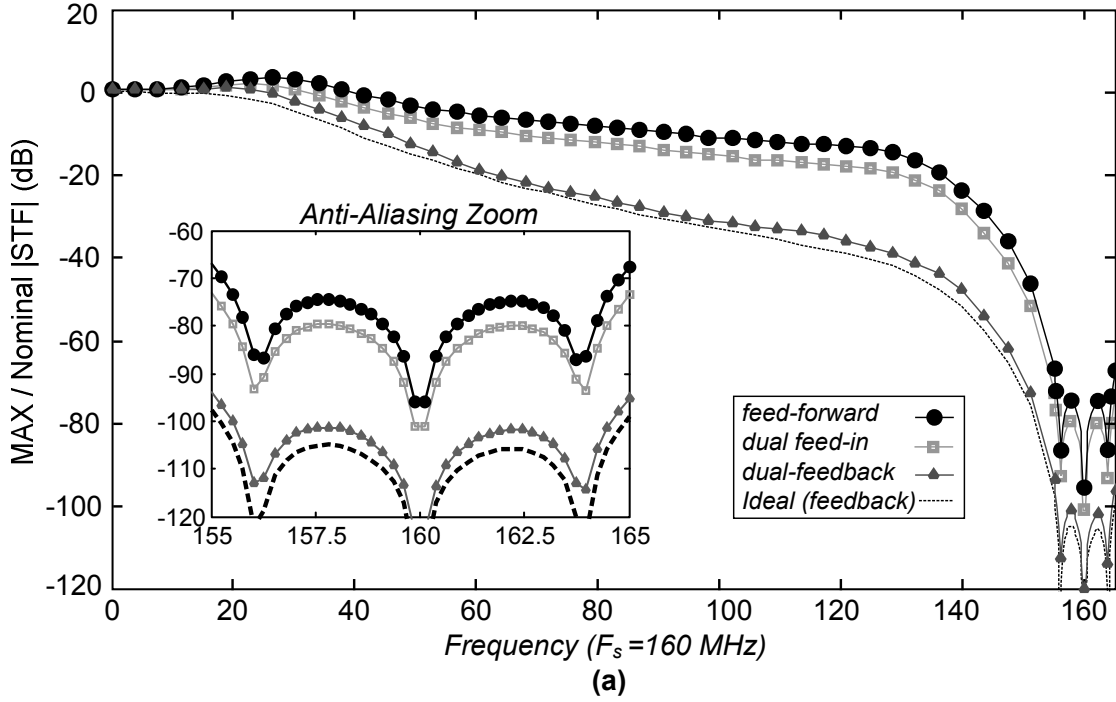
Figure 5.12: STF sensitivity comparison when mismatch σ = 2% (a) worst-case STF magnitude response; (b) Standard deviation of Δ|STF|.

4 dB and 27 dB from the expected 99 dB for the dual-feedback and dual feed-in

modulators while the feeforward modulator exhibits a 32 dB degradation. Moreover the

worst-case STF peaking stays below 1 dB and 2 dB, respectively, for the dual-feedback and dual feed-in structures while the feedforward modulator can show up to 4 dB of peaking. Figure 5.12(b) compares the standard deviation of the STF of these modulators due to component mismatch versus frequency. Except for frequencies corresponding to the notches of the STF, the STF of the dual-feedback modulator exhibit less than 1 dB variation over the entire frequency range from DC to the sampling frequency. The dual feed-in structure which uses only a single DAC in its feedback path provides slightly better STF behavior than the feedforward modulator, particularly at lower frequencies. This helps the modulator to withstand larger out-of-band blockers in a receiver application, when compared to the feedforward structure. Clearly the dual-feedback structure provides the lowest sensitivity STF and best filtering performance, although at the expense of an extra feedback DAC.

5.5 Analog Summer Elimination

CT-$\Delta\Sigma$ modulators using feeforward, dual-feedback or dual feed-in structures, as respectively shown in Figures 5.1(b), 5.10(a) and 5.11(a), require an explicit analog summer before the quantizer. This block requires an extra amplifier to implement and can demand significant bandwidth and power consumption due to the small feedback factor seen by the opamp. In the proposed dual-feedback and dual feed-in structures the adder can be eliminated by performing both the integration and summation operations in the third stage of the modulator. This can be achieved only if the signals carried through the direct feedback paths a_4 and the feedforward paths a_3 (and a_2 in dual feed-in) are differentiated prior to being applied to the third integrator. Since the feedback

(a)

(b)
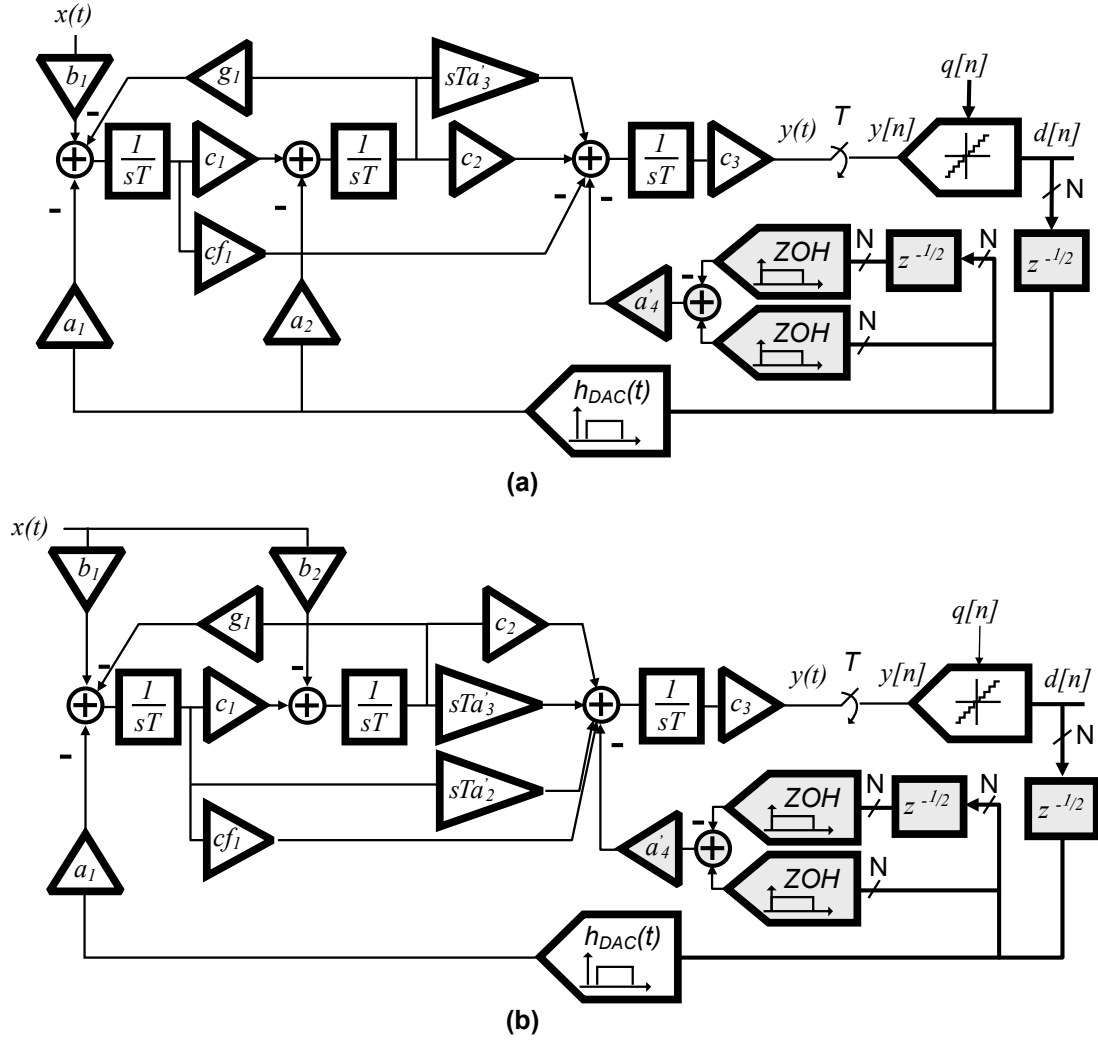
Figure 5.13: (a) Dual-feedback and (b) dual feed-in architectures modified for analog summer removal.

signal is inherently discrete-time, it can be differentiated using a semi-digital DT differentiator with a transfer function of the form [71]

$$TF(z) = 1 - z^{-\tau/T} \quad ; \quad (\tau \le T - \tau_d) \tag{5.28}$$

In this case the direct feedback a_4 in Figures 5.10(a) and 11(a) should be replaced with $a'_4 = (a_4/c_3) \cdot (1 - \tau_d/T)^{-1}$ as shown in Figure 5.13. The operation of the DT differentiator can be explained intuitively using Figure 5.14(a). The ideal NRZ pulse
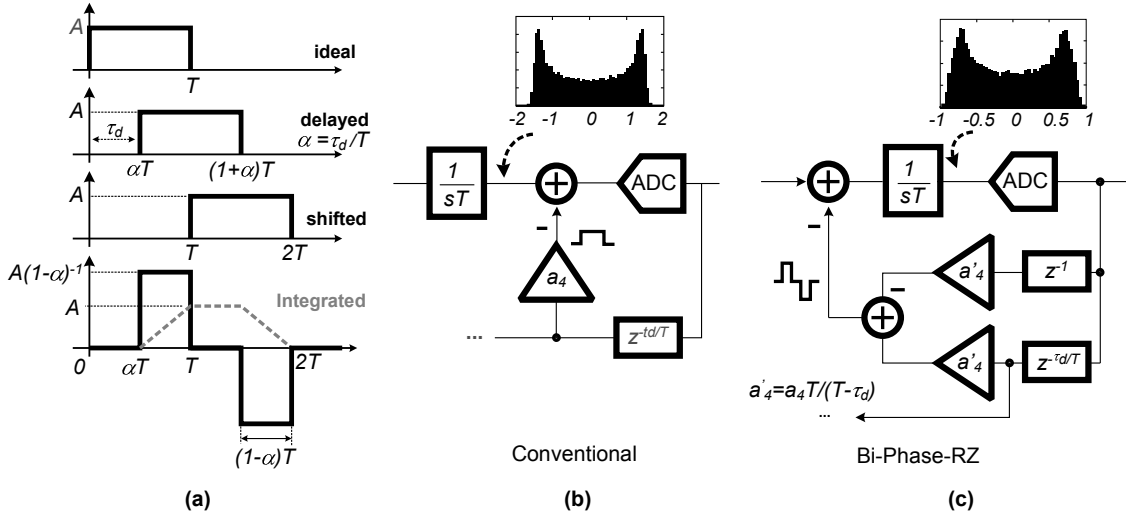
Figure 5.14: (a) Dual-feedback and (b) dual feed-in architectures modified for analog summer removal.

has amplitude A and duration of one sampling period (T). Subject to an ELD equal to τ_d, the ideal waveform will be delayed by αT where $\alpha = \tau_d / T$ is the normalized delay. Subtracting the T-shifted quantizer signal from the original output results in a return to zero pulse that extends to the next sample by a negative sign, and we will refer to this waveform as bi-phase-return-to-zero (bi-phase-RZ). The integration of this pulse using the last stage of the loop-filter produces a trapezoidal signal that flattens during the return-to-zero intervals, and its net effect on the integrator state gets reset to zero at time $2T$. At the sampling instance the peak of the trapezoid will be equal to A provided the amplitude of the bi-phase-RZ pulse is multiplied by $(1-\alpha)^{-1}$ before being applied to the last integrator. In other words the original feedback a_4 should be scaled by $(1-\tau_d/T)^{-1}$. Due to the sharing of the c_3 gain with integrator output, further scaling by $1/c_3$ will be required to keep the state of the quantizer input unchanged, leading to a total scaling of

$$a'_4 = (a_4 / c_3) \cdot (1 - \tau_d / T)^{-1}.$$

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An important benefit of the DT differentiator approach is a two-fold reduction in the last integrator's output swing as shown by the histograms of the state variables in Figures 5.14(b) and (c). It is also noted that the gain c_3 can be built into the quantizer. Particularly a $c_3>1$ further reduces the last integrator output swing which can be beneficial in a low-voltage design. However this would set more stringent requirements on the quantizer design because the comparators would need to resolve smaller voltages. The comparator challenge in most cases is easier to manage than the headroom limitation which is a fundamental issue in low-voltage designs. The subtraction in (5.28) is implemented simply by connecting the two current-mode NRZ DAC outputs together with opposite polarities.

Differentiation in the feedforward paths can be carried out by replacing the constant gain block a_3 (and a_2 in dual feed-in) with sTa'_3 (and sTa'_2 in dual feed-in) as shown respectively for the adder-less architectures in Figure 5.13(a) and (b). In an active-RC implementation, the differentiator path with sTa'_3 scaling factor is realized by a capacitive input with a value of a'_3C_f when C_f is the integration capacitor. This will increase the noise gain of the last integrator and will reduce its closed loop bandwidth. It should be noted that in the adder-less topologies of Figure 5.13, any latency originated from the limited bandwidth of the last integrator, will be directly added to modulator ELD which can harm the performance. One way to alleviate this problem is to increase the feedback factor of the last integrator by proper choice of the modulator coefficients, where the relationship can be approximated as

$$\beta_{sum} \approx \left(2 + \sum_{j=M}^{N} \frac{a_j}{c_N} \right)^{-1} \qquad (5.29)$$

In the above a_j s are feedforward coefficients values and c_N is the last integrator output scaling factor, N is the modulator order and the architecture-dependent parameter $M \leq N$ is respectively 3 and 2 for the dual-feedback and dual feed-in structures of Figure 5.13. Assuming the ELD compensation uses current mode DACs to implement the DT differentiator, the gain $a_{\cdot 4}$ will not affect the feedback factor. Equation (5.29) clearly shows that when $c_N > 1$, building the last integrator gain into the quantizer increases the feedback factor. This involves a trade-off between relaxing the open loop bandwidth of the last amplifier and more stringent requirements on the comparators of the quantizer. For example the choice of $c_3=2$ can be justified only if the power saving in the last integrator, by allowing the use of a slower amplifier, outweighs the power increase in the flash quantizer by cutting the LSB size in half which lowers the tolerable offset by a factor of two.

CHAPTER 6

A THIRD-ORDER DUAL-FEEDBACK CT DELTA-SIGMA MODULATOR, DESIGN AND IMPLEMENTATION

This chapter describes the design of a third-order CT-$\Delta\Sigma$ modulator, implemented for proof of concept, based on the proposed adder-less dual feedback architecture in Figure 5.13(a). The design goals were 76 dB dynamic range (DR) over 5 MHz signal bandwidth, 60 dB minimum anti-aliasing and no STF peaking. The NTF and STF of the design example in section 5.2.1 with *OSR=16* and using a 16-level quantizer meet the noise shaping and anti-aliasing targets. The modulator NTF provides an ideal SQNR of 87.7 dB which leaves sufficient margin for the targeted dynamic range, after taking into account the circuit noise and non-idealities. The final block diagram of the system including the signal levels and coefficient values is shown in Figure 6.1. By simply decreasing the flash ADC's reference level by a factor of 2, the $c_3=2$ coefficient (see Figure 5.13(a)) is built into the quantizer in order to relax the third integrator GBW requirements by increasing its feedback factor.
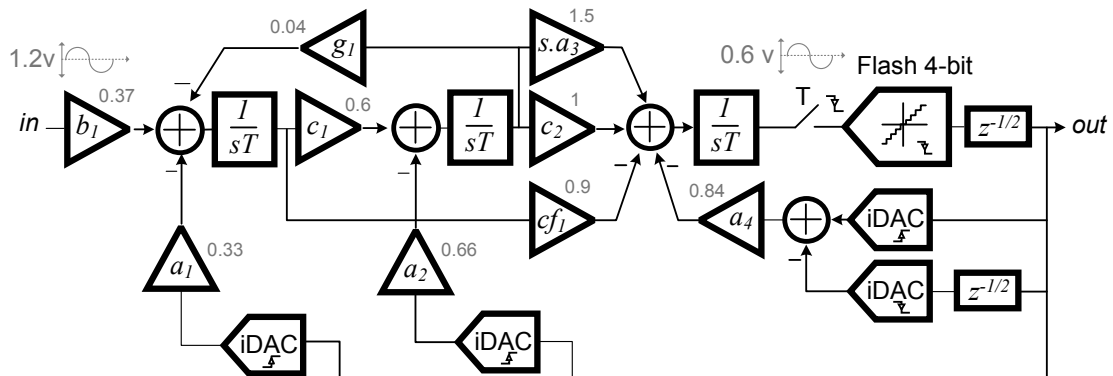
Figure 6.1: Structure of the implemented dual-feedback CT $\Delta\Sigma$ modulator.
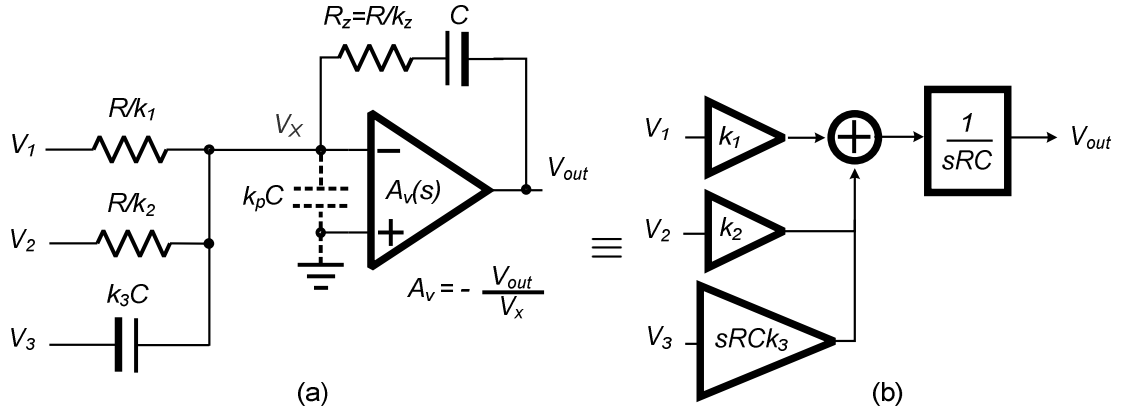
Figure 6.2: (a) Active-RC integrator with capacitive gain input, and (b) its block diagram representation

The following sections will present and overview of the system and circuit level design as well as the test and measurement results.

6.1 Modeling Active-RC Integrator with Capacitive Input

In this work, active-RC integrators have been used to take advantage of their high linearity. Eliminating the analog summer requires the last integrator to operate as a summer for the path created by coefficient sa_3 in Figure 6.1. This is achieved using a capacitor to couple between the second and third integrator in addition to a resistor to implement the path corresponding to c_2 coefficient. Thus, the general structure of the integrators implemented in this design will be similar to Figure 6.2(a). The gain-bandwidth product (GBW) of the amplifiers, used to realize the three integrators, affects the modulator dynamics and also its STF and NTF. Low-voltage amplifier design in advanced CMOS technologies often rely on multi-stage topologies [72] to achieve sufficient DC gain. Obviously such amplifiers cannot be accurately described using a single-pole model [22] as explained in the behavioral model of Chapter-3. Moreover in

wideband CT-ΔΣ modulators using higher orders NTFs and low OSR, the parasitic effects such as amplifiers stray input capacitance may not be negligible. An accurate integrator model is essential to studying the impact of the amplifier's finite speed on the modulator performance. The basic integrator model of Chapter-3 needs enhancement to account for the capacitive input paths and associated feedback factor reduction.

The building block built around an amplifier in a CT-ΔΣ modulator may receive multiple signals through different components. The general structure of such a signal processing block with two resistive and one capacitive input is shown in Figure 6.2(a). Assuming an ideal amplifier, the output of this block would be

$$Vout = \frac{k_1}{sRC}V_1 + \frac{k_2}{sRC}V_2 + k_3V_3 \tag{6.1}$$

The above ideal equation corresponds to the model in Figure 6.2(b). In practice, the amplifier exhibits a frequency-dependent gain of $A_v(s)$ which represents voltage gain from the inverting input V_x to the output V_{out}. In the circuit of Figure 6.2(a) the transfer function of the i-th input can be expressed as

$$TF_i = -\frac{Z_f}{Z_i} \cdot \frac{\beta(s) \cdot A_v(s)}{1 + \beta(s) \cdot A_v(s)} \tag{6.2}$$

where Z_i is the impedance of the *i-th* input and Z_f is the feedback impedance. For a resistive input with gain k_i the impedance ratio becomes

$$\frac{Z_f}{Z_i} = \frac{k_i(sRC/k_z + 1)}{sRC} = \frac{k_i}{s}(\frac{s}{k_z} + 1) \tag{6.3}$$

where k_i and k_z are the scaling factors of the *i-th* input resistor and the feedback resistor respectively. Also we have assumed a normalized sampling period of *RC=T=1/Fs=1* to

make the integrator model independent of the sampling frequency. The feedback factor $\beta(s)$ in the circuit of Figure 6.2(a) is

$$\beta(s) = \frac{s}{s^2 \dfrac{k_p}{k_z} + s\left[1 + k_p + \sum_j k_j + \sum_i \dfrac{k_i}{k_z}\right] + \sum_i k_i} \tag{6.4}$$

The above equation takes into account the effect of the amplifier's input parasitic capacitance and also the feedback resistor R_z through parameters k_p and k_z respectively. Substituting (6.2) and (6.3) in (6.1) leads to an expression for the output voltage as

$$Vout(s) = \left[\left(\frac{s}{k_z} + 1\right)\sum_i \frac{k_i V_i}{s} + \sum_j k_j V_j\right]\frac{\beta(s)A_v(s)}{1 + \beta(s)A_v(s)} \tag{6.5}$$

The scaling factors k_i and k_j correspond, respectively, to the resistive and capacitive inputs. The amplifier gain $A_v(s)$ can be expressed in terms of its DC gain, normalized poles, zeros and gain-bandwidth product (ω_u) as

$$A_v(s) = \frac{\displaystyle\prod_{j=1}^{m}(s/z_j + 1)}{(s/\omega_u + 1/A_0) \cdot \displaystyle\prod_{i=2}^{n}(s/p_i + 1)} \tag{6.6}$$

Note that $\omega_u = A_0 p_1$ can in general be different from the amplifier unity gain-bandwidth. Also the gain expression in (6.6) needs to include the loading effect of the feedback network.

A block diagram representation of equation (6.5) is depicted in Figure 6.3(a). The feedback-factor $\beta(s)$ is placed in both feedforward and feedback paths to isolate the virtual ground node V_x. This makes it possible to accurately model the input-stage nonlinearity of the amplifier using a non-linear element, as illustrated in Figure 6.3(b).
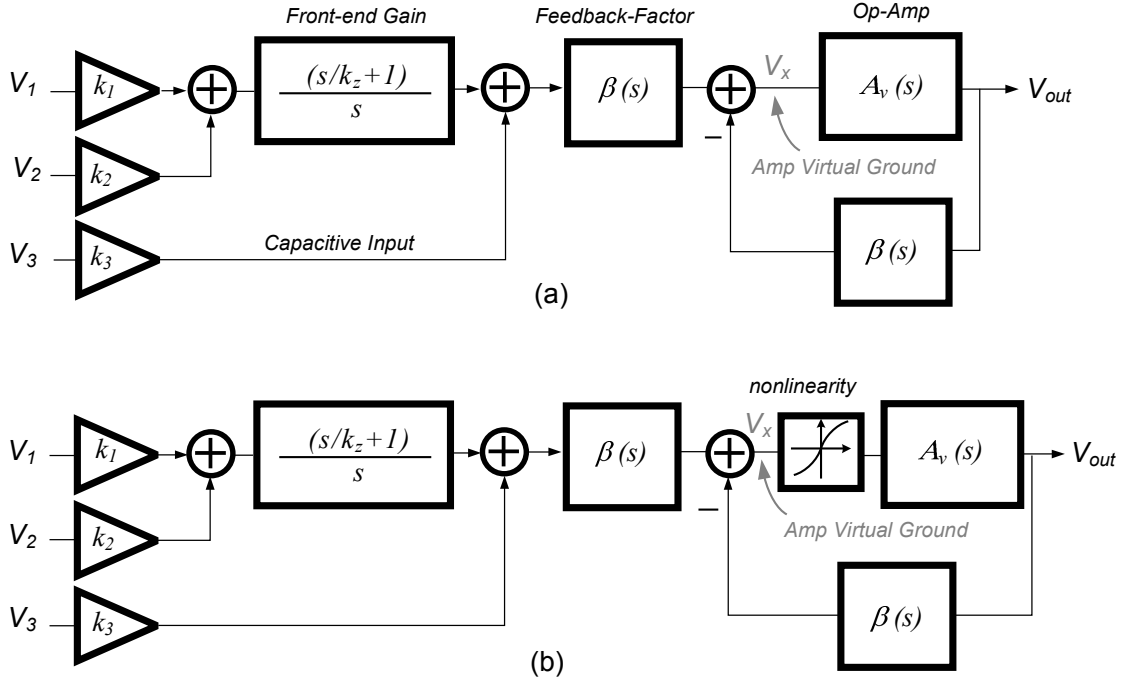
Figure 6.3: (a) Multi-input active-RC integrator model (b) including input stage nonlinearity.

6.1.1 Finite Amplifier GBW Effect on Modulator Performance

In this work, we have used the two-stage amplifier topology shown in Figure 6.4. The amplifier employs Miller compensation through a current-mode feedback path. The open loop voltage gain of the amplifier includes a low-frequency dominant pole, a pair of non-dominant complex poles, a left-half-plane zero near the complex poles and a third pole at much higher frequencies than the unity gain which can be ignored. The transfer function of the amplifier in terms of transconductance $g_{m1,2,3}$, output resistance $R_{1,2}$ and parasitic, load and compensation capacitors of respectively C_1, C_2 and C_{c1} is derived as

$$A_v(s) = \frac{A_0(\frac{s}{z_1} + 1)}{(\frac{s}{p_1} + 1)(\frac{s^2}{\omega_n^2} + \frac{2\zeta s}{\omega_n} + 1)} \tag{6.7}$$

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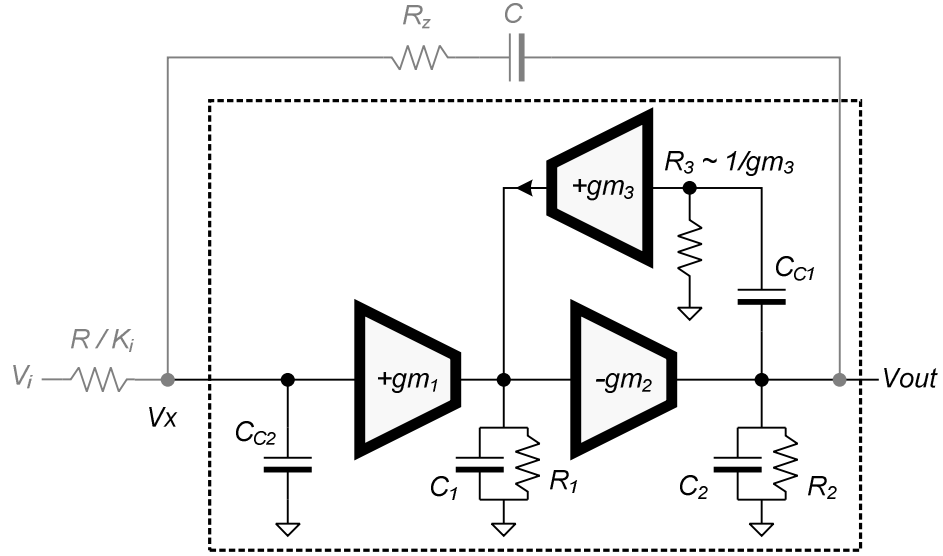
Figure 6.4: Structure of the two-stage opamp used in active-RC integrators.

where the DC voltage gain A_0, zero and poles are related to the amplifier parameters as

$$A_0 = g_{m1}g_{m2}R_1R_2$$
$$p_1 = A_0^{-1}(g_{m1}/C_{c1})$$
$$z_1 = g_{m3}/C_{c1} \tag{6.8}$$
$$\omega_n = \sqrt{(g_{m2}/C_2)(g_{m3}/C_1)}$$
$$\zeta = (z_1/2)(1 + C_{c1}/C_2)\omega_n^{-1}$$

In an active-RC integrator the integration capacitor must be included as part of the load capacitor C_2. Also capacitor C_{c2} is added to the amplifier inputs to gain further control over the closed-loop stability. The approximate closed loop GBW of this amplifier when used in an integrator application similar to Figure 6.2(a) is

$$\omega_{u-cl} \approx \frac{g_{m1}}{C_{c1}} \frac{C}{C_{c2}+C} \tag{6.9}$$

In the above equation C is the integration capacitor, g_{m1} is the transconductance of the input stage, and C_{c1} and C_{c2} are the compensation capacitors.

In the following simulations the DC gain of the amplifier is assumed to be 60 dB and the modulator sampling frequency is 160 MHz. All integrators use $k_p=0.1$ and $k_z=5$. To investigate the effect of each amplifier on the modulator performance, the closed-loop GBW of each integrator is swept between $F_s/4$ to $2F_s$ while the GBW of all other integrators is kept constant at $2F_s$. For each point, the CT loop filter $LF(s)$ has been discretized to compute the NTF. The simulation results are plotted in Figure 6.5 for all three amplifiers. Note that the NTF is shown in the anti-aliasing region of the STF, i.e. in the vicinity of F_s, for better visualization. According to the z-plane maps shown in Figure 6.5(a), the dual-feedback modulator is stable across the entire GBW sweep range of the 1st amplifier. Figure 6.5(b) indicates that both STF and NTF exhibit more variation due to the second integrator's GBW. Figure 6.5(c) reveals that the modulator stability is more sensitive to the GBW of the third integrator. However once stability has been achieved, the NTF and STF show only slight variation due to the speed of the 3rd amplifier.

The series resistor R_z is traditionally used to eliminate the right-half-plane zero resulting from signal feed-through by the integration capacitor. From frequency compensation theory it is well known that a right-half-plane zero causes phase lag which for a CT-$\Delta\Sigma$ loop translates into excess loop delay. In the dual-feedback modulator, the resistor R_z of the 2nd integrator is found to have a significant effect on stability and anti-aliasing. The simulation results when the parameter k_z $(\propto 1/R_z)$ of the second integrator is swept between 2 and 8 are shown in Figure 6.6. All other integrators are assumed to use $k_z=5$. Finite amplifier GBW of 0.5, 1.0 and 1.5 are chosen for the 1st, 2nd and 3rd integrators, respectively. Anti aliasing improves by as
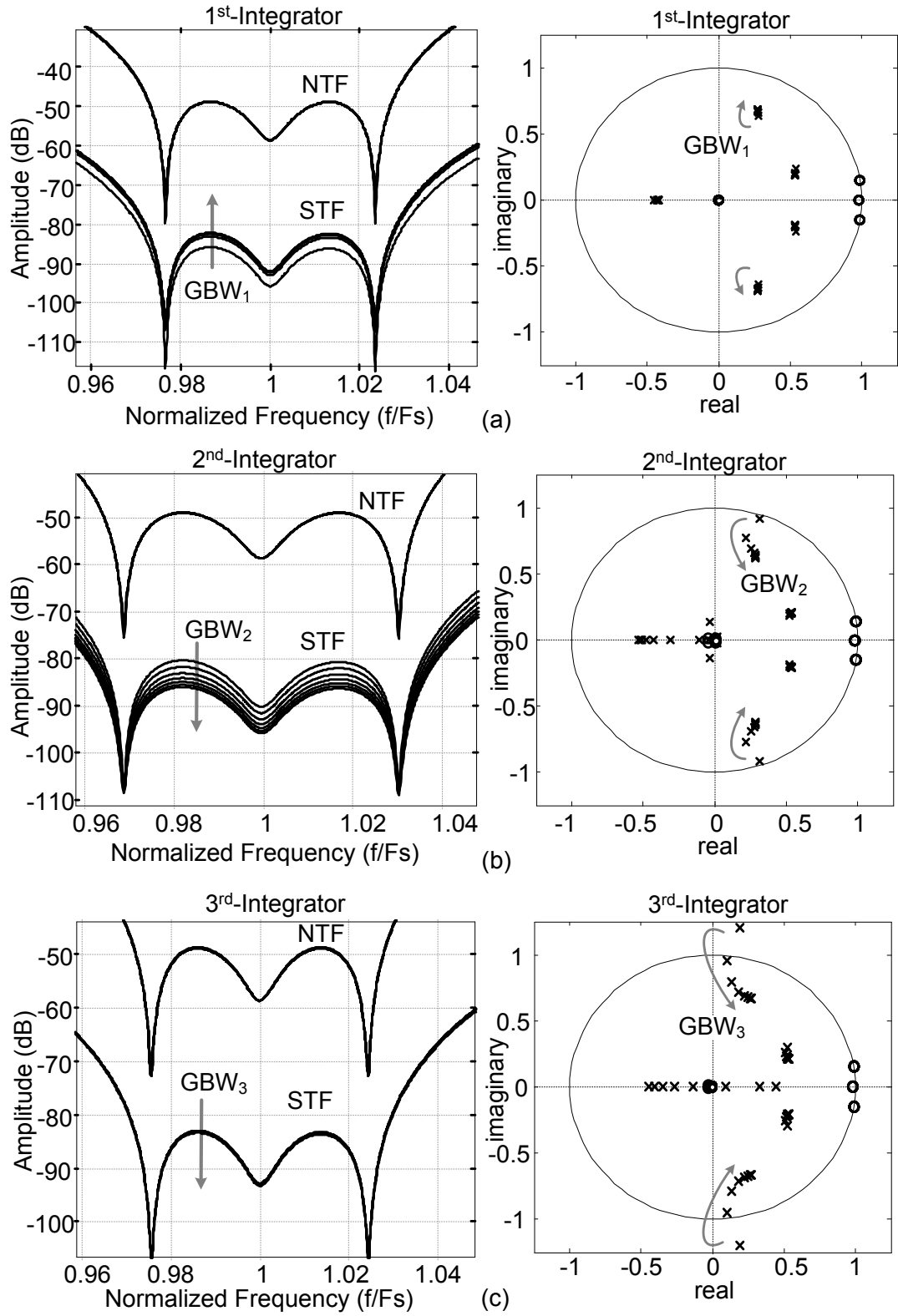
Figure 6.5: Effect of amplifier GBW on stability, NTF and STF; results shown for (a) first integrator, (b) second integrator, and (c) third integrator.
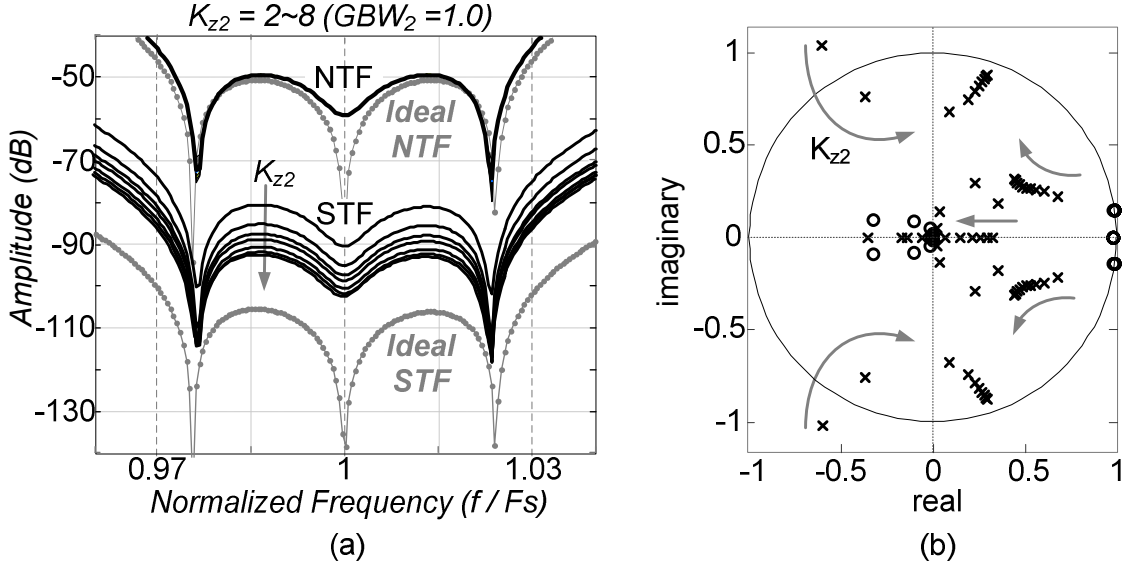
Figure 6.6: (a) STF and NTF response to *kz2* variation, (b) Pole/Zero map.

much as 14 dB as k_z increases from 2 to 8. The minimum k_z required for stability is *3* as shown in the Pole/Zero maps of Figure 6.6(b). The suitable k_z is between 4 to 5. Any further increase of k_z (smaller R_z's) degrades the performance by resulting in high-Q poles and reduced maximum stable input range. This behavior is analogous to the effect of the nulling resistor in a miller-compensated amplifier [73]. In our simulations, $k_z = 5$ was identified as a suitable value for all integrators (i.e. $R_z=R/5$).

6.1.2 RC Time Constant Variation

The effect of time-constant variation on the third-order dual-feedback modulator was analyzed using the proposed integrator model and the set of GBW and k_z parameter values obtained in the previous subsection. Figure 6.7 shows the magnitude of the largest pole of the modulator along with the estimated change in SQNR as a function of *RC* variation. The noise shaping shows 2.5 dB improvement when *RC* is reduced by
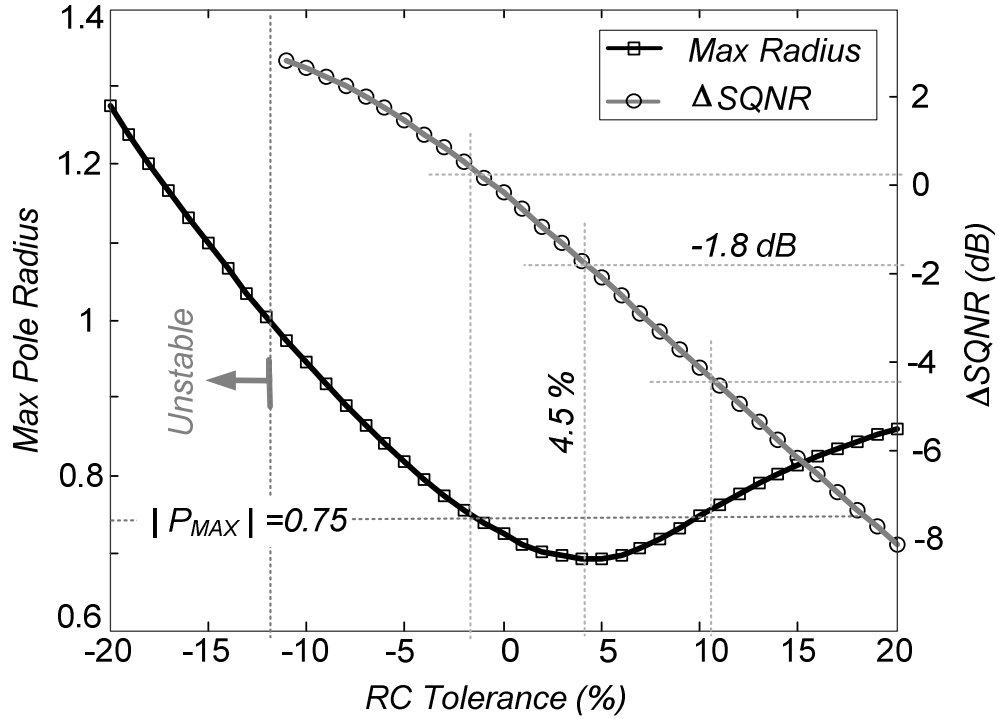
Figure 6.7: Maximum pole radius and SNR variation versus RC tolerance.

11% . Further reduction of *RC*, however, pushes the NTF poles outside of the unit circle and causes instability. Also the high-Q poles that are close to the unit circle cause NTF peaking at frequencies around $F_s/2$ and hence degrade STF filtering according to (5.5). A maximum radius of 0.75 will ensure minimal peaking and improved stability. This condition is met when *RC* variations are kept within -2% to 11%. In order to evenly spread variations across the range, all coefficients have been increased by the median of this range or 4.5 %. This results in better stability and less STF peaking at the expense of 1.8 dB reduction in SQNR. After coefficient re-adjustment, the maximum and minimum SQNR becomes, respectively, 87.7 dB and 83.3 dB across the range. These SQNR numbers were obtained from transient simulations that also accounted for limited integrator swings. The *RC* tuning needs to maintain the RC variation within +/- 6.5%. This can easily be implemented by a 4-bit trimmed integration capacitor.
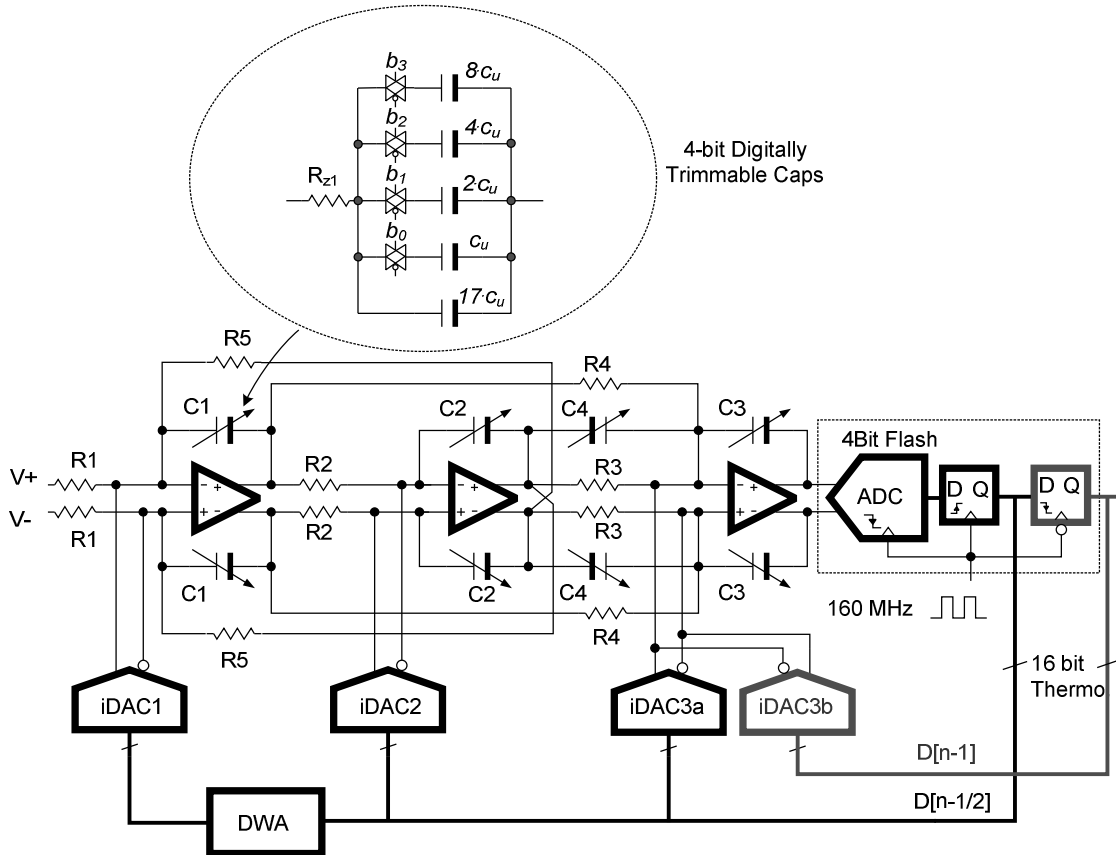
Figure 6.8: Active-RC implementation of the dual-feedback modulator.

6.2 Circuit Design

Figure 6.8 shows the circuit-level implementation of the dual-feedback modulator shown in Figure 6.1. Integrators are of active-RC type owing to their better linearity and higher signal swing. They also provide virtual ground nodes to properly sink the output signal of the current-mode DACs. All loop-filter capacitors are implemented using a bank of 16unit metal-insulator-metal (MIM) capacitors and are programmable by a 4-bit externally-applied code. The feedforward path designated by sa_3 in Figure 6.1 has been implemented using the capacitor ratio C_4/C_3. Also using the
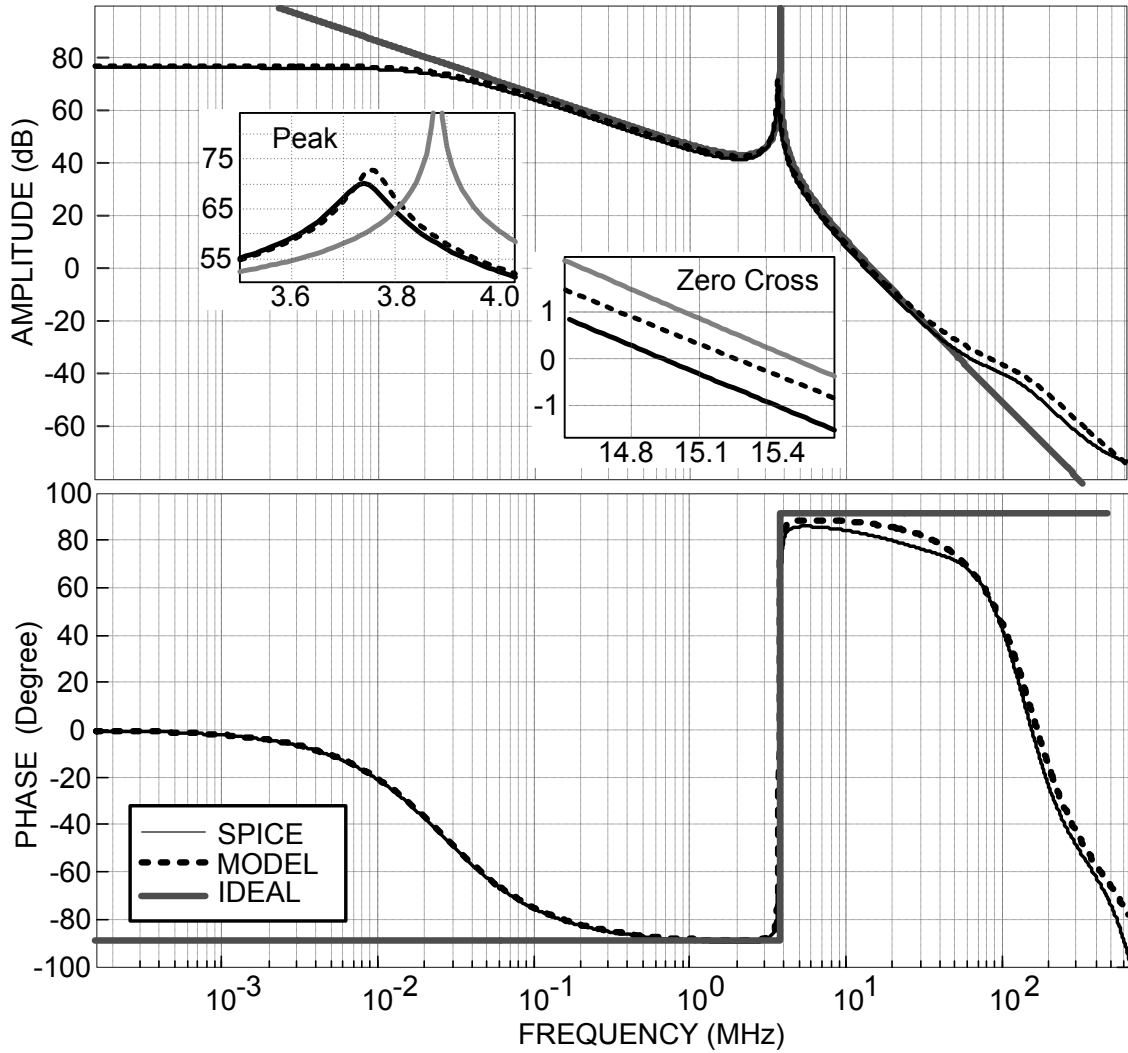
Figure 6.9: Bode Plot of the modulator filter, Spectre versus MATLAB model.

integrator model explained in the previous section, amplifier GBW of $F_s/2$, F_s and 1.5 F_s were selected for the 1st, 2nd and 3rd integrators, respectively, where F_s is the 160 MHz sampling frequency.

The magnitude response of the modulator filter is shown in Figure 6.9 and compares the transistor-level Spectre simulation with MATLAB results obtained using the proposed integrator model. The ideal response is also shown for reference. The

model predicts the peak and unity gain frequencies respectively with +0.2% and +%1.5 accuracy. The model predicts the phase response with a good accuracy as well. Clearly the peaking frequency, which corresponds to the zeros of the NTF, is moved from its ideal location due to finite amplifier GBW. However, because of sufficient margin on SQNR compared to the target dynamic range (DR), no coefficient readjustment was deemed necessary to re-center the NTF notch.

The quantizer is a 4-bit flash type and includes a half-period delay. Delay compensation is performed with DT differentiation method as explained by equation (5.28) with parameter $\tau = T/2$. Both DAC_1 and DAC_2 use NRZ pulsing because of its lower sensitivity to clock jitter. Data-Weighted-Averaging (DWA) [13] is applied only to DAC_1 for dynamic element matching while the mismatch effect of DAC_2 is noise shaped by the first integrator. Component mismatch in the DACs of the delay compensation loop has negligible effect on the modulator performance.

The 0.13 um CMOS process used for circuit design and implementation offers two threshold voltage options: nominal-VT with 500 mV and 550mV for NMOS and PMOS, respectively, and low-VT with 140mV and 160mV for N and P type devices. In the following sections we will present further details about the analog building blocks.

6.2. 1 Amplifier

The amplifiers are designed based on noise and signal swing requirements. Figure 6.10 shows the integrator output swings versus the frequency of the input signal. The results are obtained using behavioral transient simulations with a fixed input amplitude of -1 dBFS and sweeping the frequency from DC to F_s=160 MHz.
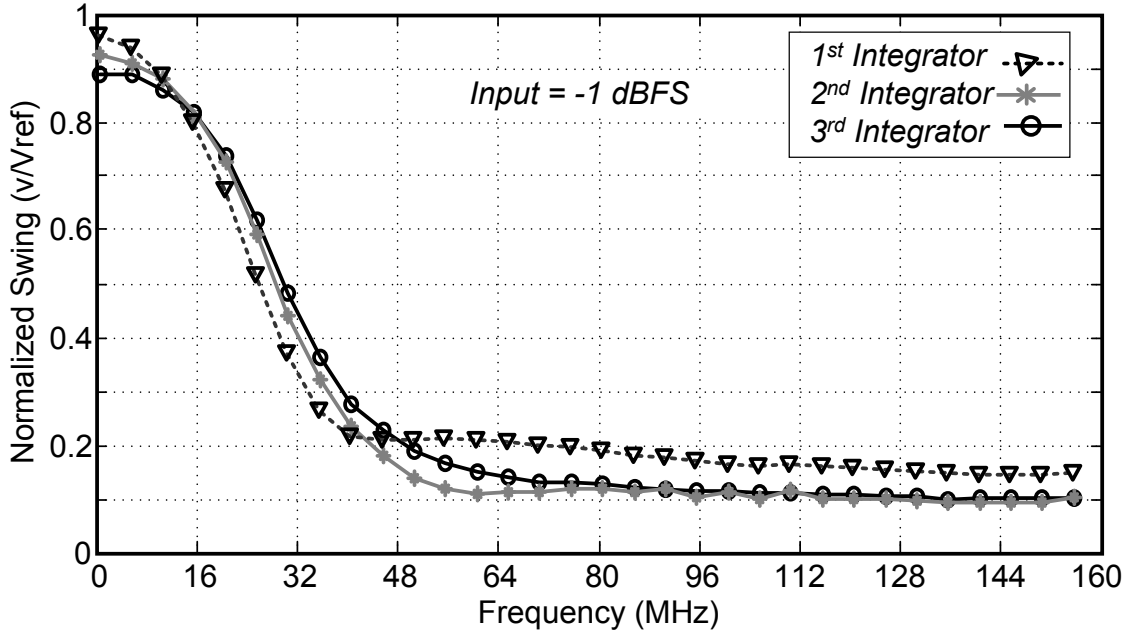
Figure 6.10: Integrator output swings versus frequency for -1 dBFS input level.

The modulator coefficients define the output swing of all integrators which are all near the full-scale for a low-frequency input signal. The low-pass profile of the output swing proves useful in preventing THD degradation by integrator clipping in the presence of a strong interferer. The amplifier schematic is depicted in Figure 6.11. The two-stage amplifier uses cascoded transistors in the first stage to achieve high DC gain. The second stage is optimized for large voltage swings in order to maximize the full-scale range of the $\Delta\Sigma$-modulator, and subsequently reduce the power consumption. The gain provided by the 2nd stage ensures a low signal swing at the output of the 1st stage, which is crucial for proper operation of the cascoded transistors. The V_{dsat} used for the devices is around 100mV which add up to 600 mV in the stack that includes the degeneration resistors. The remaining headroom to 1.2V supply provides design margin and accommodates a small swing on the output of the 1st stage. The gm_1 of the first
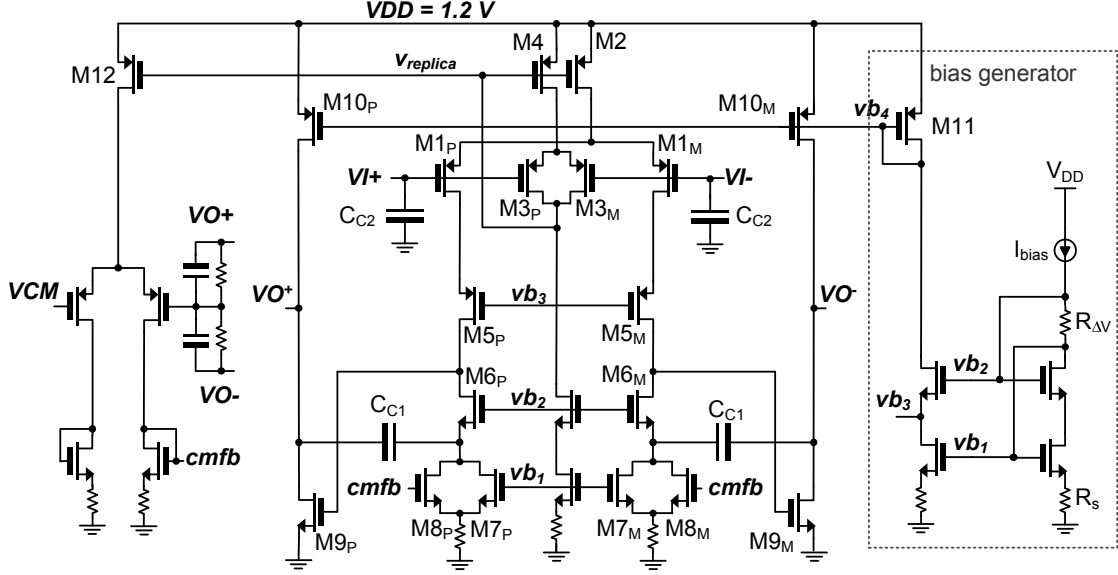
Figure 6.11: Schematic of the differential two-stage amplifier.

stage of the opamp was set by thermal noise requirements while its bias current was determined to meet a target THD of -80 dB [51]. The input referred total noise of the amplifier is derived as

$$\tilde{V}_{ni-amp}^{2} = 8KT\frac{\eta_{th}}{3g_{m1}}f_{B} + \frac{K_{fN}\eta_{f}}{C_{ox}^{2}W_{1}L_{1}}\ln(\frac{f_{B}}{f_{min}}) \tag{6.10}$$

In the above equation f_B is the signal bandwidth, f_{min} is the lower bound on the flicker noise bandwidth, K_f is the device flicker noise coefficient, W and L are device width and length respectively, η_{th} and η_f respectively are excess noise factors of thermal and flicker noise related to the opamp device parameters as

$$\begin{cases} \eta_{th} = 2\left(1 + \frac{(g_{m7} + g_{m8})}{g_{m1}} \cdot \frac{1 + (3/2)(g_{m7} + g_{m8})R_s}{[1 + (g_{m7} + g_{m8})R_s]^2}\right) \\ \eta_{f} = 2\left(1 + \frac{K_{fN}}{K_{fP}} \cdot \frac{L_1}{L_7} \cdot \frac{W_1}{W_7 + W_8} \cdot \frac{(g_{m7} + g_{m8})^2}{g_{m1}^{2}[1 + (g_{m7} + g_{m8})R_s]^2}\right) \end{cases} \tag{6.11}$$

The factor of 2 in (6.11) accounts for the fully-differential nature of the amplifier. Also both equations simply show that increasing the source degeneration resistance will

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decrease the total noise. However an upper bound for R_s exists based on the headroom limitations set by M6 , M7,8 and M9 devices.

Due to the large voltage gain of the first stage, the noise contribution of the second stage becomes negligible and has been ignored in (6.11). Using the definition $g_m = 2I_D / \Delta V$ and taking the note of equal currents flowing through R_s resistor and NMOS/PMOS, load / input devices, equation (6.11) can be re-written based on the device gate overdrive voltage $\Delta V = (V_{GS} - V_T)$ and the degeneration resistor $I.R$ drop (ΔV_s) relative values as

$$\begin{cases} \eta_{th} = 2\left(1 + \dfrac{(\Delta V_1 / \Delta V_7)[1 + 3(\Delta V_s / \Delta V_7)]}{[1 + 2(\Delta V_s / \Delta V_7)]^2}\right) \\ \eta_f = 2\left(1 + \dfrac{K_{fN}}{K_{fP}} \cdot \dfrac{L_1}{L_7} \cdot \dfrac{W_1}{W_7 + W_8} \cdot \dfrac{(\Delta V_1 / \Delta V_7)^2}{[1 + 2(\Delta V_s / \Delta V_7)]^2}\right) \end{cases} \tag{6.12}$$

The designed amplifier has $(\Delta V_s / \Delta V_1) = (\Delta V_s / \Delta V_7) = 2$ and uses larger channel lengths for M7 and M8 NMOS load devices, so that the total flicker noise is dominated by the input differential pair.

Due to limited headroom, a single current source (M2) is used for biasing the input pair. The tail current through M2 is kept relatively constant by adaptively biasing its gate using M3$_P$, M3$_M$ and M4 replica devices. Frequency compensation using current feedback through the NMOS cascode devices (M6) allows us to circumvent the right-half-plane zero problem [74]. The integrator's closed-loop response is further adjusted by capacitors C$_{C2}$ connected to the amplifier inputs. These capacitors also reduce the glitch energy and the switching noise of the current-mode DACs which particularly become highly signal-dependent when DWA is active.
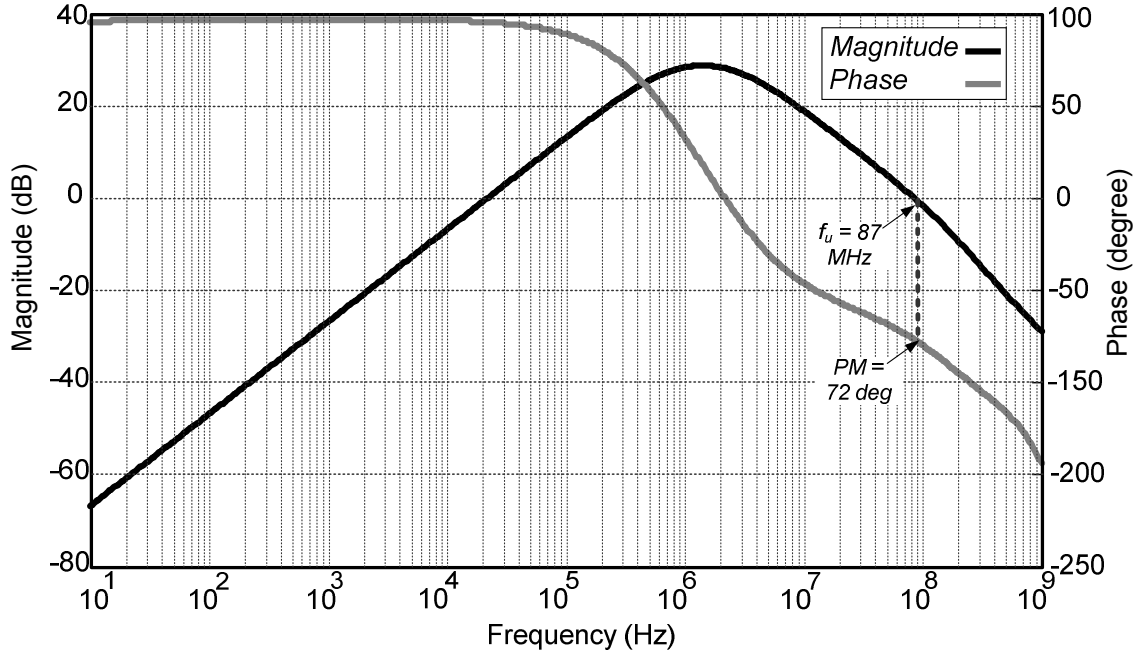
Figure 6.12: Bode Plot of the first Integrator loop.

The integrator noise and power requirement set the value of the input transconductor g_{m1}. Knowing the required closed-loop bandwidth from the integrator modeling section, the values of C_{C1} and C_{C2} capacitors are picked for adequate phase and gain margin. The C_{C1} capacitor is minimized as much as possible to allow for increasing the size of C_{C2} without sacrificing the GBW. This practice guarantees maximum attenuation of the glitches produced by current-mode DAC during switching transitions. For maximum robustness the minimum C_{C1} is determined through AC simulations such that the phase margin of the integrator loop does not go below 70 degrees. The bode plot of the first-integrator loop using the two-stage amplifier is shown in Figure 6.12. The 70 dB low-frequency attenuation of the integrator loop response is due to 70 dB DC gain of the amplifier. Also the unity-gain frequency is 87 MHz. Phase and gain margins are 72 degrees and 28 dB, respectively. The 2nd and 3rd
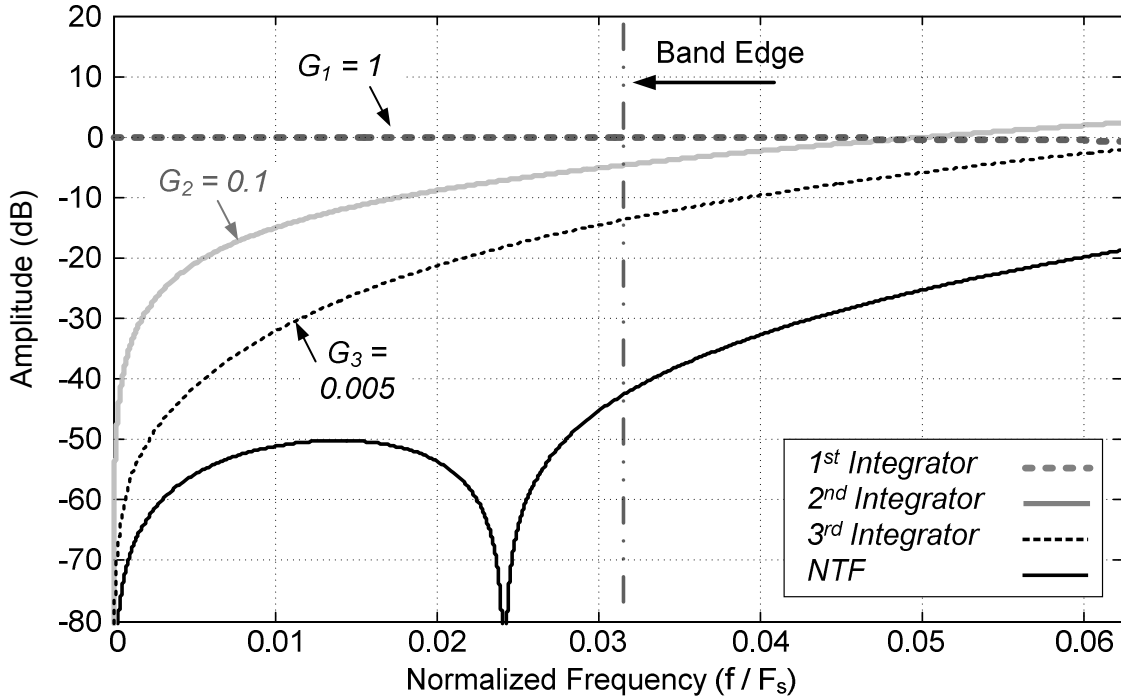
Figure 6.13: Noise transfer functions of the integrator inputs.

stage amplifiers are scaled versions of the 1st opamp by factors of 4 and 8, respectively. In the last integrator C_4 serves also as C_{C2} which eliminates the need for this capacitor in the 3rd opamp.

6.2.2 Modulator Noise Analysis and Scaling

In the designed modulator the 2nd and 3rd integrators are scaled down to reduce the total power consumption. In each integrator, increasing all resistance values by a factor k_r while decreasing all capacitors and all currents by the same factor, keeps the system dynamics unchanged. This also allows reducing the amplifier power consumption by the same factor. The scaling process exploits the noise shaping property of the internal nodes of a $\Delta\Sigma$ modulator. The closer to the quantizer, the more noise shaping occurs, as shown in the graphs of Figure 6.13. The input referred noise of

the first-integrator will see the same STF as the input signal hence, the first integrator noise is not subjected to any noise shaping. As shown in Figure 6.13 the noise transfer functions of the 2nd and 3rd integrators include a zero at DC which effectively attenuates their 1/f noise, and thereby makes the first integrator dominant in the total modulator flicker noise. This simplifies the noise analysis by only considering the thermal noise contributions of all the integrators and separately adding the flicker noise of the first stage to the total noise. The modulator input-referred thermal noise $S_{nth\text{-}in}$ can be expressed in terms of the individual integrator noise powers $S_{nth1}...S_{nth3}$ as

$$S_{nth-in} = S_{nth1}\left(1 + k_{r2}\frac{G_2}{G_1}\frac{S_{nth2}}{S_{nth1}} + k_{r3}\frac{G_3}{G_1}\frac{S_{nth3}}{S_{nth1}}\right) \tag{6.13}$$

In the above equation k_{r1} and k_{r2} respectively are the scaling factors of the 2nd and 3rd integrators. Also $G2/G1$ and $G3/G1$ are normalized noise power gains obtained from numerical integration of the noise transfer functions of Figure 6.13 which, respectively, are 0.1 and 0.005 for the 2nd and 3rd integrators.

The noise model of the first integrator is shown in Figure 6.14. The included noise sources are thermal noise of the input resistor, the resonator feedback resistor marked by g_1, the noise current of the first feedback DAC, the noise of the amplifier, and finally the noise of the nulling resistor R_{z1}. The total input-referred thermal noise of the first integrator can be derived as (see Appendix C)

$$S_{nth1} = 8KTR_1 f_B \left\{ 1 + \frac{R_1}{R_2} + \underbrace{\frac{R_{z1}}{R_1}\left(\frac{\pi^2}{3b_1^2 OSR^2}\right)}_{\text{effect of Rz}} + \right.$$

$$\left. \frac{\eta_{th}}{3g_m R_1}\left[\left(1 + \frac{R_1}{R_2}\right)^2 + \underbrace{\left(1 + \frac{2R_{z1}}{R_1 \parallel R_2}\right)\frac{\pi^2}{3b_1^2 OSR^2}}_{\text{effect of Rz}}\right] + \frac{8\hat{V}_{in}}{3\Delta V_{DAC1}}\cdot\frac{a_1}{b_1}\right\} \tag{6.14}$$

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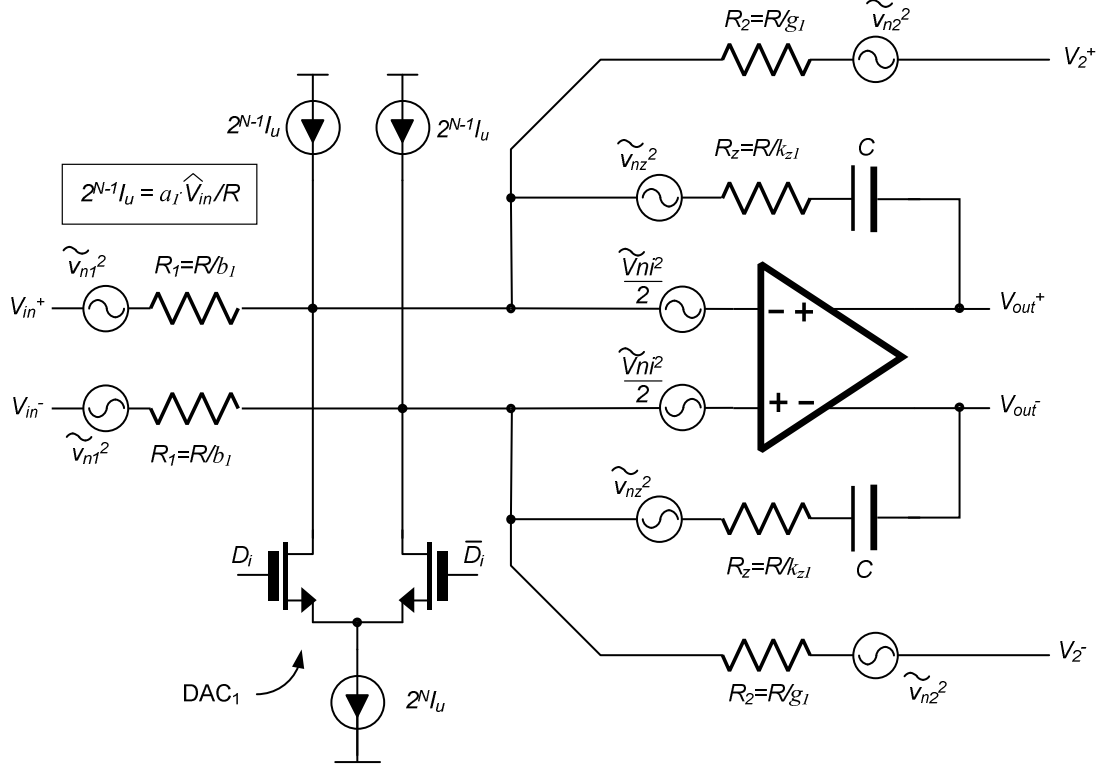
Figure 6.14: The noise model of the first integrator.

In the above equation, g_m is the input stage transconductance of the amplifier in the 1st integrator, η_{th} is the excess thermal noise factor defined in (6.12), $\hat{V}_{in}$ is the single ended peak amplitude of the input signal, ΔV_{DAC1} is the gate overdrive of the DAC current source device and f_B is the signal bandwidth. The noise contribution of R_z was found negligible due to the high impedance of the integrator feedback capacitor at baseband frequencies. Similarly, the effect of the integrator feedback impedance comprising C and R_z can be ignored in the input-referred flicker noise of the first integrator, which leads to the following equation

$$S_{nflk1} \approx \frac{K_{fN}\eta_f}{C_{ox}{}^2 W_1 L_1}\ln(\frac{f_B}{f_{\min}})(1+\frac{R_1}{R_2}) \qquad (6.15)$$

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The η_f is the excess flicker noise factor of the amplifier defined in (6.12). Also (6.14) and (6.15) can be rewritten in terms of the dimension-less coefficients of the modulator

$$S_{nth1} = 8KT\frac{R}{b_1}f_B\left[1 + \frac{g_1}{b_1} + (1+\frac{g_1}{b_1})^2\frac{b_1\eta_{th}}{3g_mR} + \frac{8\hat{V}_{in}}{3\Delta V_{DAC1}}\cdot\frac{a_1}{b_1}\right] \tag{6.16}$$

$$S_{nflk1} \approx \frac{K_{fN}\eta_f}{C_{ox}{}^2W_1L_1}\ln(\frac{f_B}{f_{\min}})(1+\frac{g_1}{b_1}) \tag{6.17}$$

In the above equations R is the reference resistance of the active-RC integrator using the definition $RC=F_s^{-1}$ where C is the reference integration capacitance. The values of the modulator coefficients b_1, g_1 and a_1 are given in Figure 6.1.

Using the noise model of the second integrator shown in Figure 6.15(a) the input-referred thermal noise of the second integrator is derived as

$$S_{nth2} = 8KT\frac{R}{c_1}f_B\left[1 + \frac{c_1\eta_{th}}{3g_mR} + \frac{8\hat{V}_{in}}{3\Delta V_{DAC2}}\cdot\frac{a_2}{c_1}\right] \tag{6.18}$$

Note that we have not included the scaling factor k_{r2} since it is already included in the total modulator noise equation in (6.13). Using the noise model of the third-integrator shown in Figure 6.15(b) we derive the following input referred thermal noise power

$$\begin{aligned}S_{nth3} = 8KT\frac{R}{c_2}f_B\Bigg\{&1 + \frac{cf_1}{c_2} + \left[(1+\frac{cf_1}{c_2})^2 + \frac{\pi^2}{3c_2{}^2OSR^2}(1+a_3)^2\right]\frac{c_2\eta_{th}}{3g_mR}\\&+ \frac{8\hat{V}_{in}}{\Delta V_{DAC3}}\cdot\frac{2a_4}{c_2}\Bigg\}\end{aligned} \tag{6.19}$$

Note that in (6.19) the amplifier noise contribution is increased due to the noise gain of the feedback network formed by C and the input capacitor a_3C. Also the delay compensation DAC$_3$ has doubled in the number of elements, since it is made of two identical DACs, 3a and 3b with their outputs shorted at the amplifier summing nodes. Hence there is a factor of 2 in front of the coefficient a_4 in (6.19).
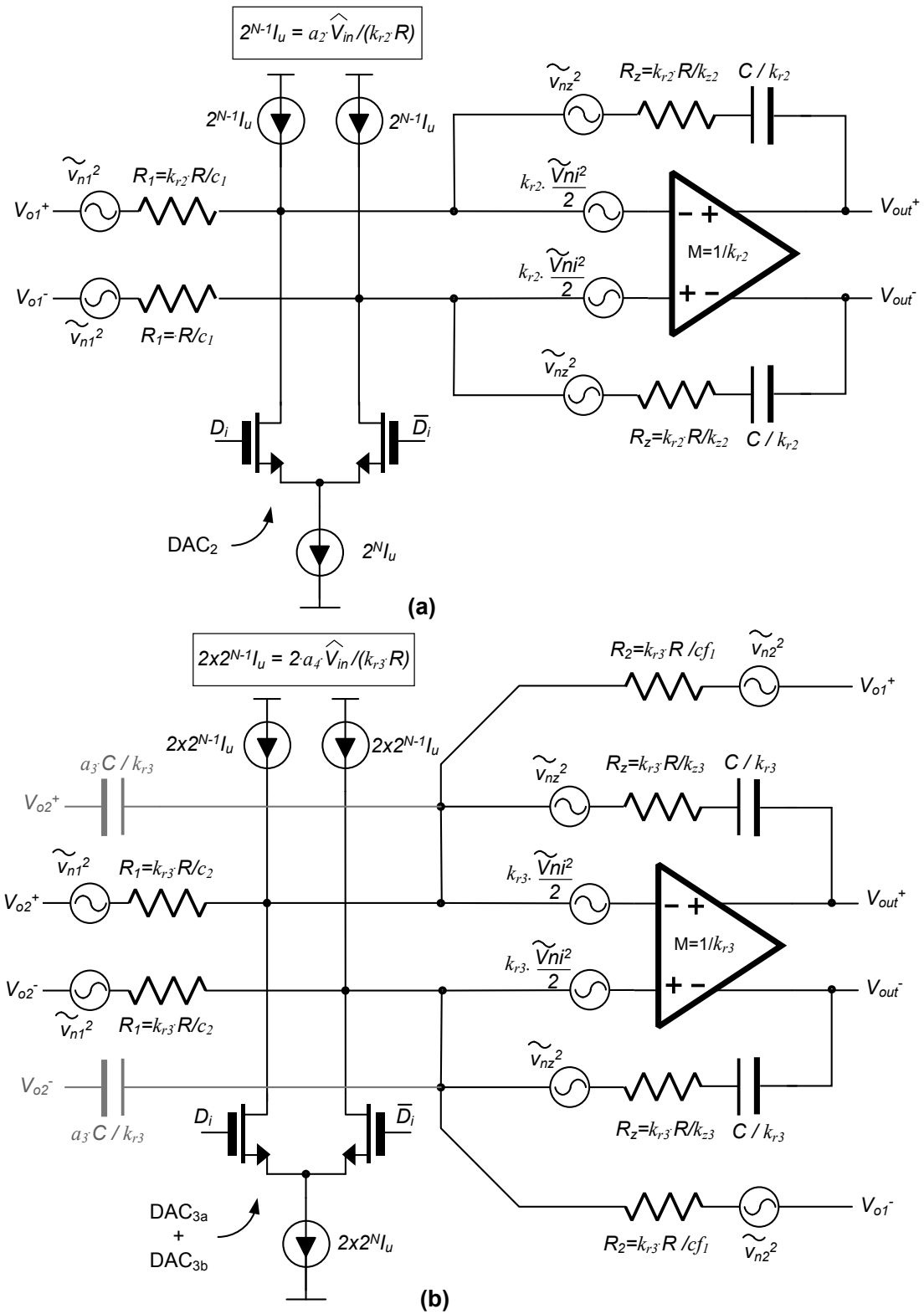
Figure 6.15: Noise models of (a) 2nd integrator and (b) third integrator.

Examining the individual integrator noise equations in (6.16), (6.18) and (6.19) reveals that, the ratio of the noise powers given in (6.17) and (6.19) to the input stage noise power given in (6.16) depends on the coefficient of the modulator, provided all DACs use the same gate overdrive voltage and all integrators use the same amplifier structure with linear scaling. Hence the total modulator input-referred noise in (6.13) can be written as a function of an unknown resistor R

$$
S_{nth-in} = KT \frac{R}{b_1} f_B \left[1 + \frac{g_1}{b_1} + (1 + \frac{g_1}{b_1})^2 \frac{b_1 \eta_{th}}{3 g_m R} + \frac{8 \hat{V}_{in}}{3 \Delta V_{DAC1}} \cdot \frac{a_1}{b_1} \right]
\\
\times \left(1 + k_{r2} \frac{G_2}{G_1} \frac{S_{nth2}}{S_{nth1}} + k_{r3} \frac{G_3}{G_1} \frac{S_{nth3}}{S_{nth1}} \right)
$$

(6.20)

It is noted that the integrator scaling increases the resistor R by k_r times and decreases the g_m of the amplifier by the same factor, hence keeping the $g_m R$ term unchanged in the denominator of noise equations in (6.16), (6.18) and (6.19). On the other hand, the dominant third-order nonlinearity of the modulator, caused by the input stage of the first integrator is given in the literature [51] for a single-stage amplifier used in a single-bit CT-$\Delta\Sigma$ modulator as

$$
HD3 = \frac{\hat{V}_{in-se}^2}{64 g_m I_D^2 R_{in}^3} (1 + \frac{R_{in}}{R_{DAC}})
$$

(6.21)

In the above equation $\hat{V}_{in-se}$ is the single-ended peak of the input. Also the term inside the parenthesis includes the ratio of the input resistor to a resistive DAC's output impedance and indicates the relative strength of the feedback to the input path in driving the amplifier inputs. Most multi-bit designs use current-mode feedback DACs in which case the ratio of the feedback to input coefficients can be used instead of resistive ratios in (6.21). Also multi-bit DACs have considerably smaller step size than

the singe-bit ones, hence a normalization coefficient $\alpha_M < 1$ is added to the equation as

$$HD3 = \frac{(\alpha_M \hat{V}_{in-se})^2}{64 g_m I_D{}^2 R_{in}{}^3} (1 + \frac{\sum k_{fbk}}{k_{in}})$$ (6.22)

In the above k_{fbk} and k_{in} respectively are coefficients of feedback and input paths attached to the summing nodes of the first amplifier. The summation is needed for cases which more than one feedback signal is injected to the first integrator. The α_M parameter is obtained from behavioral simulations by observing the maximum step size at the quantizer output and dividing it by the full scale level. In our design with 16 level (4-bits) DACs, the maximum step size was 4 LSB's, hence α_M=4/16 used in (6.22). Substituting $g_m = 2 I_D / \Delta V$, and using the integrator model in Figure 6.14 , equation (6.22) can be re-written for the designed modulator as

$$HD3 = \frac{(\alpha_M \hat{V}_{in-se})^2}{16 \Delta V_1{}^2 (g_m R)^3} [b_1{}^3 (1 + \frac{a_1 + g_1}{b_1})]$$ (6.23)

In the above equation, ΔV_1 is the gate overdrive voltage of the input transistors. Note that equation (6.23) uses $g_m R$ instead of $g_m R_{in}$ which also appears in the noise equations (6.16), (6.18) and (6.19). Hence for a known gate overdrive voltage the $g_m R$ term will be fixed and defined by the targeted HD3 according to (6.23). Also equation (6.23) assumes a single-stage amplifier (OTA). In [75] it is shown that in the case of a two-stage miller compensated amplifier the *HD3* will be less because of an increased effective g_m by a factor of $k=C/Cc$, where C and C_C are the integration and miller capacitors respectively. Based on (6.23) and the notion of effective g_m, a simulation of the power consumption can be setup by sweeping the independent variables k_{r2}, k_{r3} , and ΔV_1, to determine R and g_m values that minimize the total power consumption.
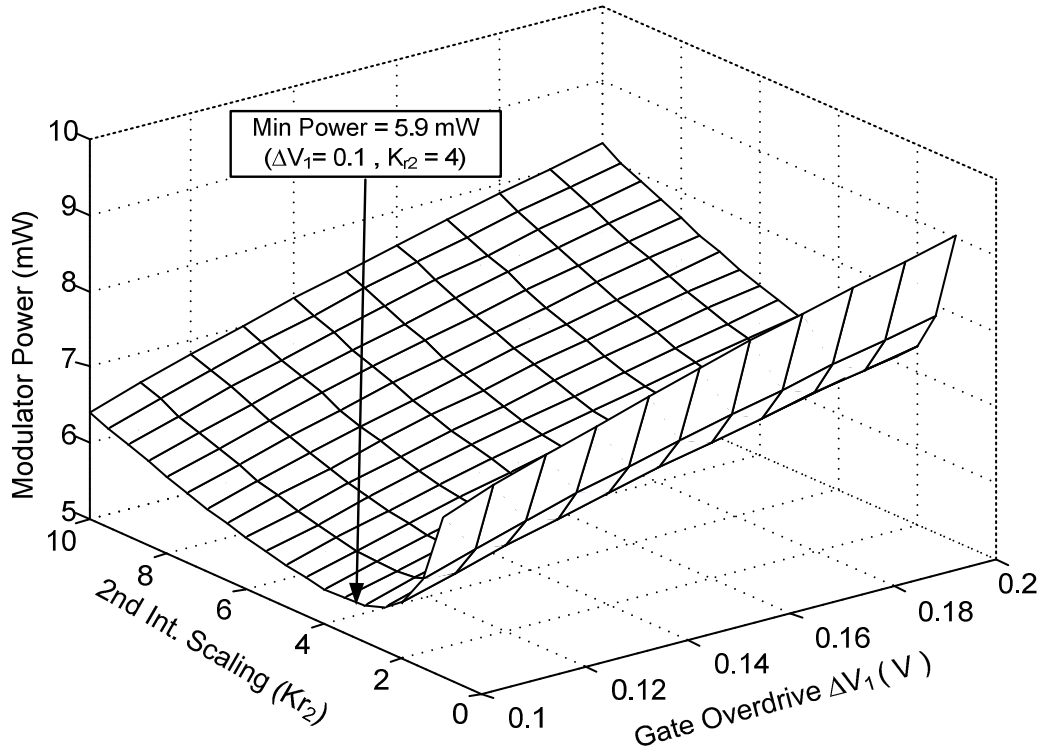
(a)
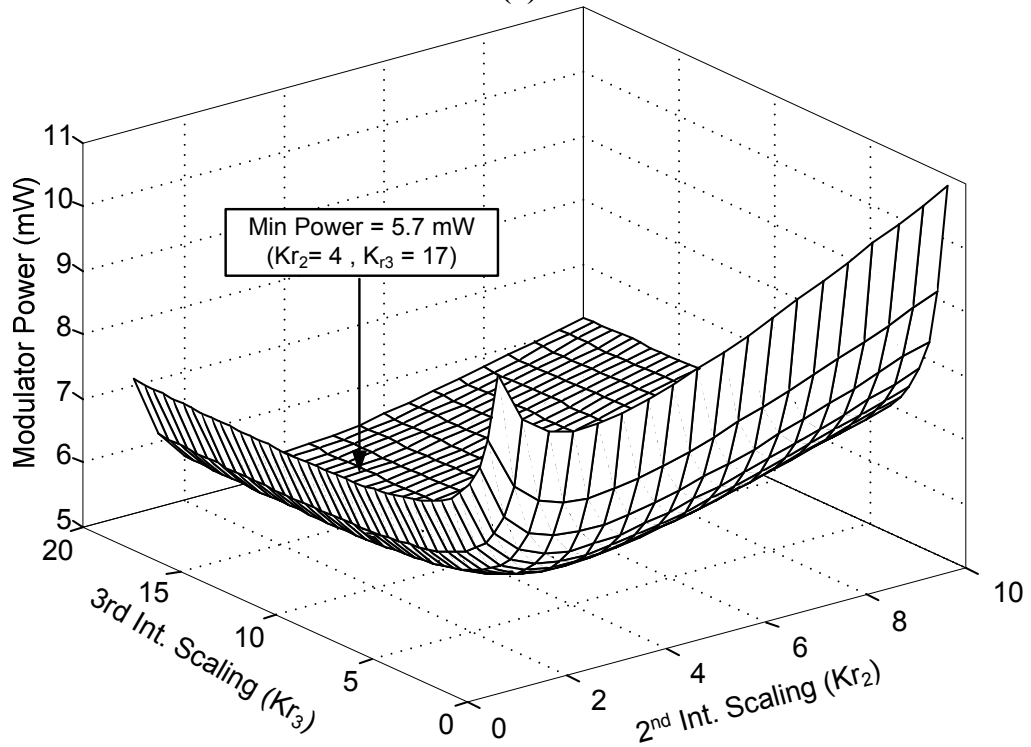
(b)

Figure 6.16: Power optimization by (a) sweeping gate overdrive and scaling factor of the 2nd integrator, (b) sweeping scaling factors of 2nd and 3rd integrators.

The 3D plots in Figure 6.16(a), and (b) show power consumption versus gate overdrive voltage and k_{r2} and k_{r3} scaling factors. The results show that the third integrator can be scaled more aggressively as its noise is shaped by modulator NTF. The optimum scaling factors are identified as 4 and 17 for the second and third integrators, respectively. Scaling by 17 is not practical due to physical design rule violations in the layout by hitting the minimum size of the capacitors. Instead a $k_{r3} = 8$ was used for the scaling of the third integrator. Power is estimated from solving equations (6.20) and (6.23) in terms of R and g_m. The bias current I_D is subsequently calculated according to $g_m = 2I_D / \Delta V$. The total quiescent current of the designed amplifier is related to the input stage transistor bias current I_D as $I_T = 10 \, I_D$. Therefore the total loop filter power consumption including all three amplifiers and DACs is estimated as:

$$P = 10V_{DD}I_D(1 + \frac{1}{k_{r2}} + \frac{1}{k_{r3}}) + \frac{2V_{DD}\hat{V}_{in-se}}{R}(a_1 + \frac{a_2}{k_{r2}} + \frac{2a_4}{k_{r3}}) \qquad (6.24)$$

The second term in (6.24) accounts for the static current of the feedback DACs. The power of the quantizer and the bias generator is not included in (6.24). This is a constant additive term which does not affect the optimal parameters obtained from the simulations shown in Figure 6.16. Also, equation (6.24) is only an estimate of the modulator power consumption, since it is relying on approximate equations such as (6.23). The transistor level parameters such as I_D, g_m and ΔV, obtained from solving (6.24) were used as a guideline in the circuit design process. The power consumption of the designed modulator closely tracked the estimated value by (6.24), although SPICE simulations showed slightly lower HD3 than the nonlinearity predicted by (6.23).
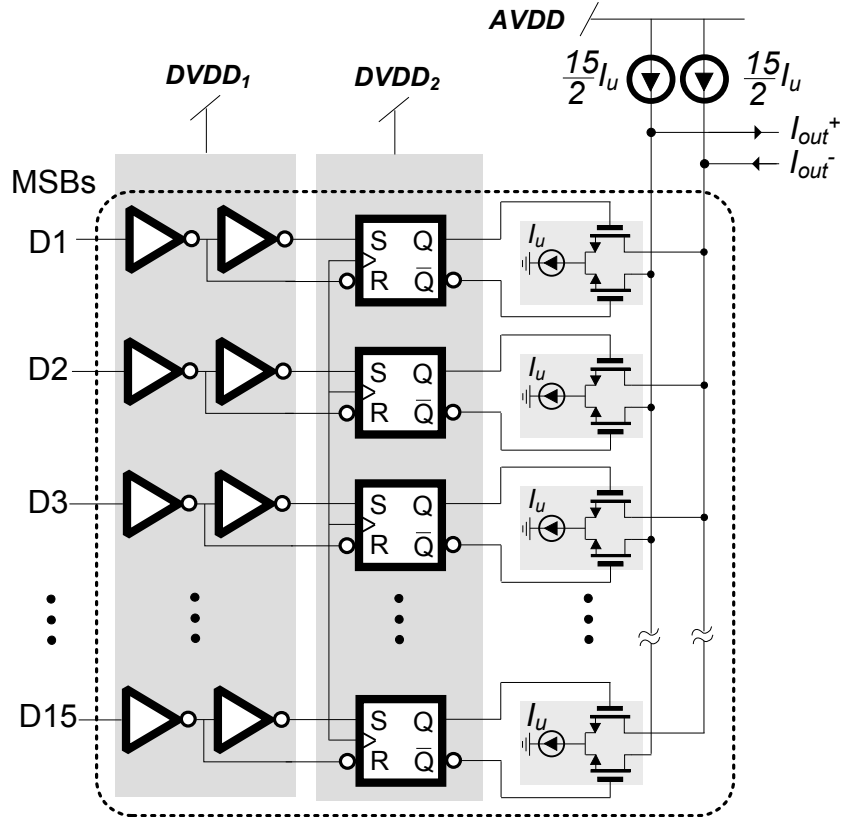
Figure 6.17: The structure of the 4-bit current mode DAC.

6.2.2 Current Mode DAC

The 4-bit current-steering DAC has the structure shown in Figure 6.17, and is composed of 15 unit current sources with differential current switches and switch drivers. The transistor-level schematic of one slice of the DAC is shown in Figure 6.18. When the data input toggles, the differential switch driver shown in Figure 6.18(a) generates overlapping pulses on the rising edge of the clock and holds the data until the next clock cycle. The current switches include dummy elements for charge injection cancellation. The schematics of the current cell and the biasing circuit are shown in Figure 6.18(b) and (c), respectively. The mismatch error of the 1st and 2nd feedback
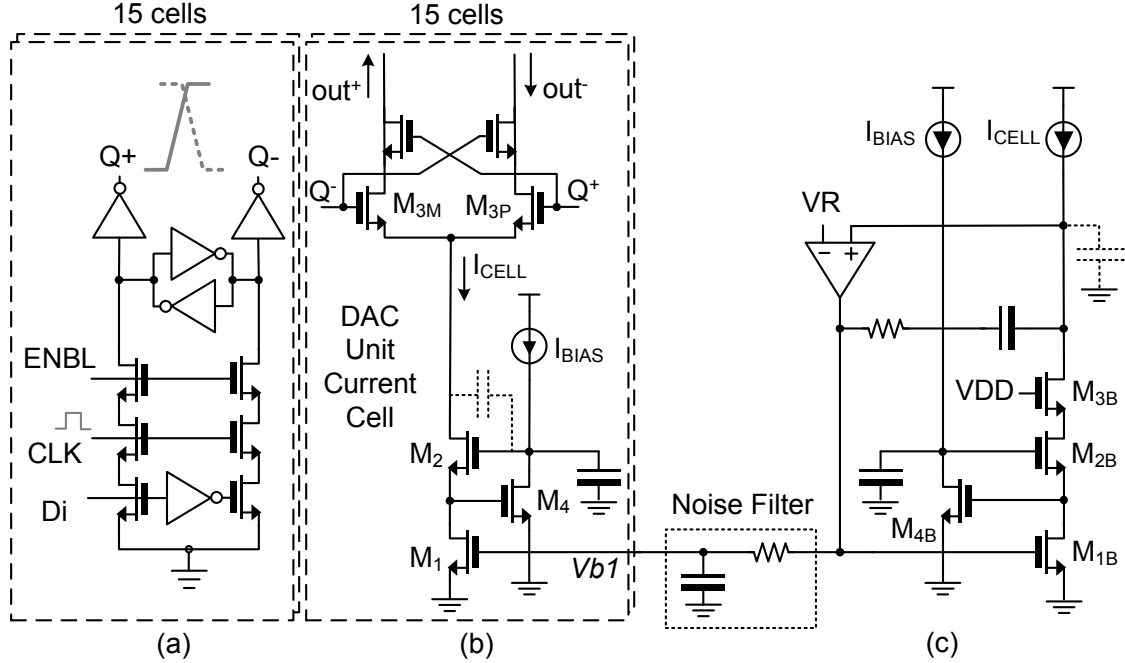
Figure 6.18: Schematic of the current-mode DAC: (a) input latch and switch driver, (b) current source and the current switch, (c) bias generator and noise-filter.

DACs is first-order noise shaped by the DWA and first integrator, respectively.

DAC behavioral simulations, as outlined in chapter 3, were employed to determine the required matching of the unit current sources. The simulation results are shown in Figure 6.19. To guarantee a minimum SNDR of 81 dB, the W and L of the NMOS current source (*M1*) were selected for 6-bit (i.e. $\sigma(\Delta I / I) = 2^{-6}$) matching according to [53]

$$\begin{cases} W^2 = \dfrac{2I}{\mu C_{ox} \sigma^2 (\Delta I / I)} \left[\dfrac{A_\beta^2}{(V_{GS} - V_T)^2} + \dfrac{4 A_{VT}^2}{(V_{GS} - V_T)^4} \right] \\ L^2 = \dfrac{\mu C_{ox}}{2I \sigma^2 (\Delta I / I)} \left[A_\beta^2 (V_{GS} - V_T)^2 + 4 A_{VT}^2 \right] \end{cases} \tag{6.25}$$

In the above equation $I = I_{DAC}/16$ is the unit element current and constants A_{VT} and A_β are transistor mismatch parameters provided by the foundry.
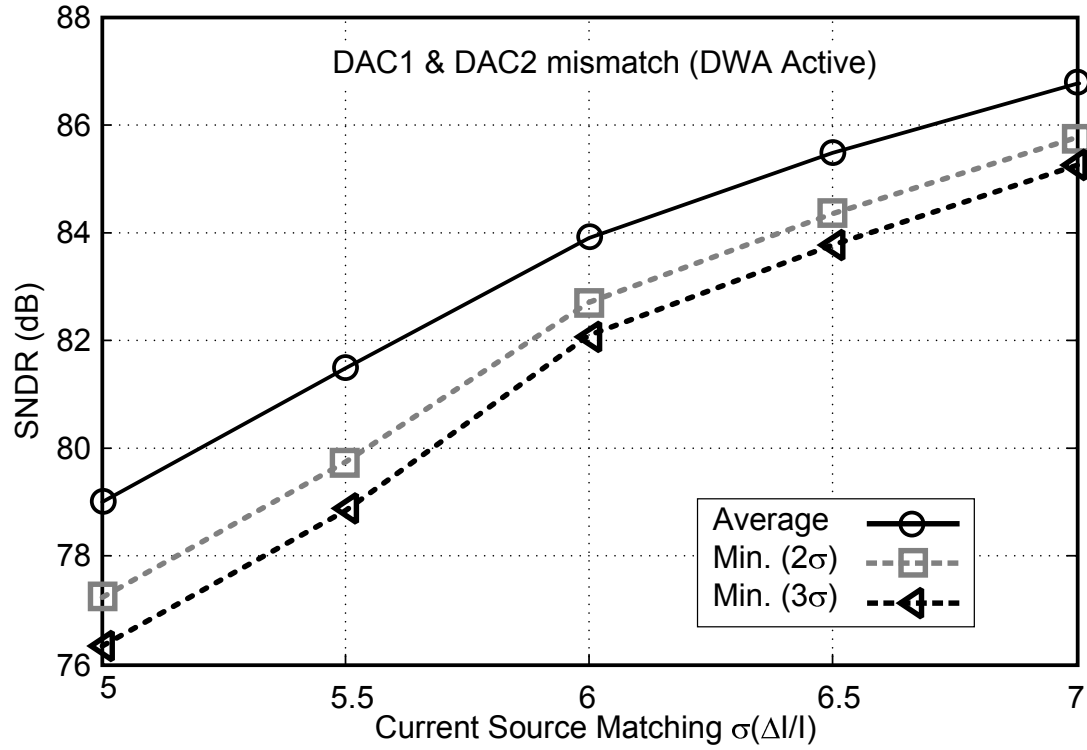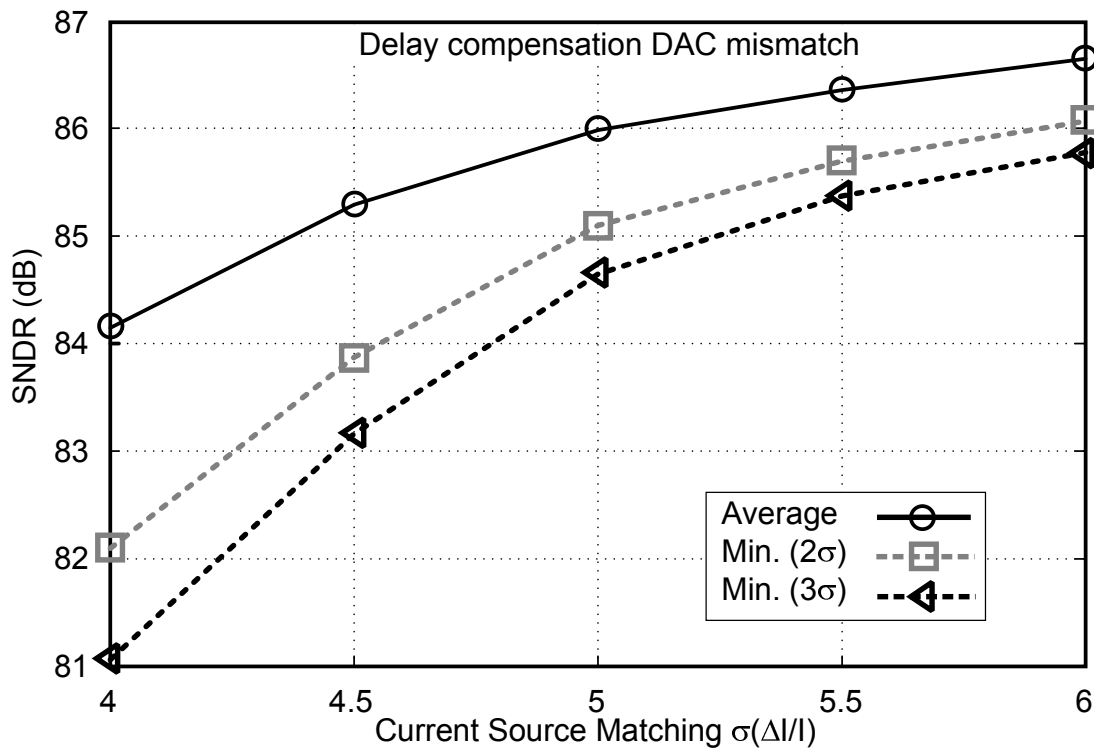
Figure 6.19: Behavioral simulation of modulator SNDR versus DAC unit element mismatch; (a) DAC_1 and DAC_2 ; (b) DAC_{3a} and DAC_{3b} .

Increasing the gate overdrive voltage ($\Delta V_{DAC} = V_{GS} - V_T$) of the current source reduces the required device area for a given matching level. This practice also results in lesser noise contribution by DAC according to (6.16). For further reduction of the output noise, a large time-constant RC-filter is placed between the bias generator and the gate of the current source. This prevents propagation of the noise of the biasing device M1B to the output. The cascode transistor M2 isolates the large capacitance of the current source device from the output node. Moreover, using regulated cascode biasing by M4 ensures a high output resistance for the unit current cells and improves the linearity.

Bypass capacitors are added to the gate of the cascode transistors to attenuate the coupled transitions through gate-drain parasitic capacitance. To increase the current copy accuracy, a low-power opamp is used in the bias generator to compensate for the voltage drop across the switch transistor (M3).
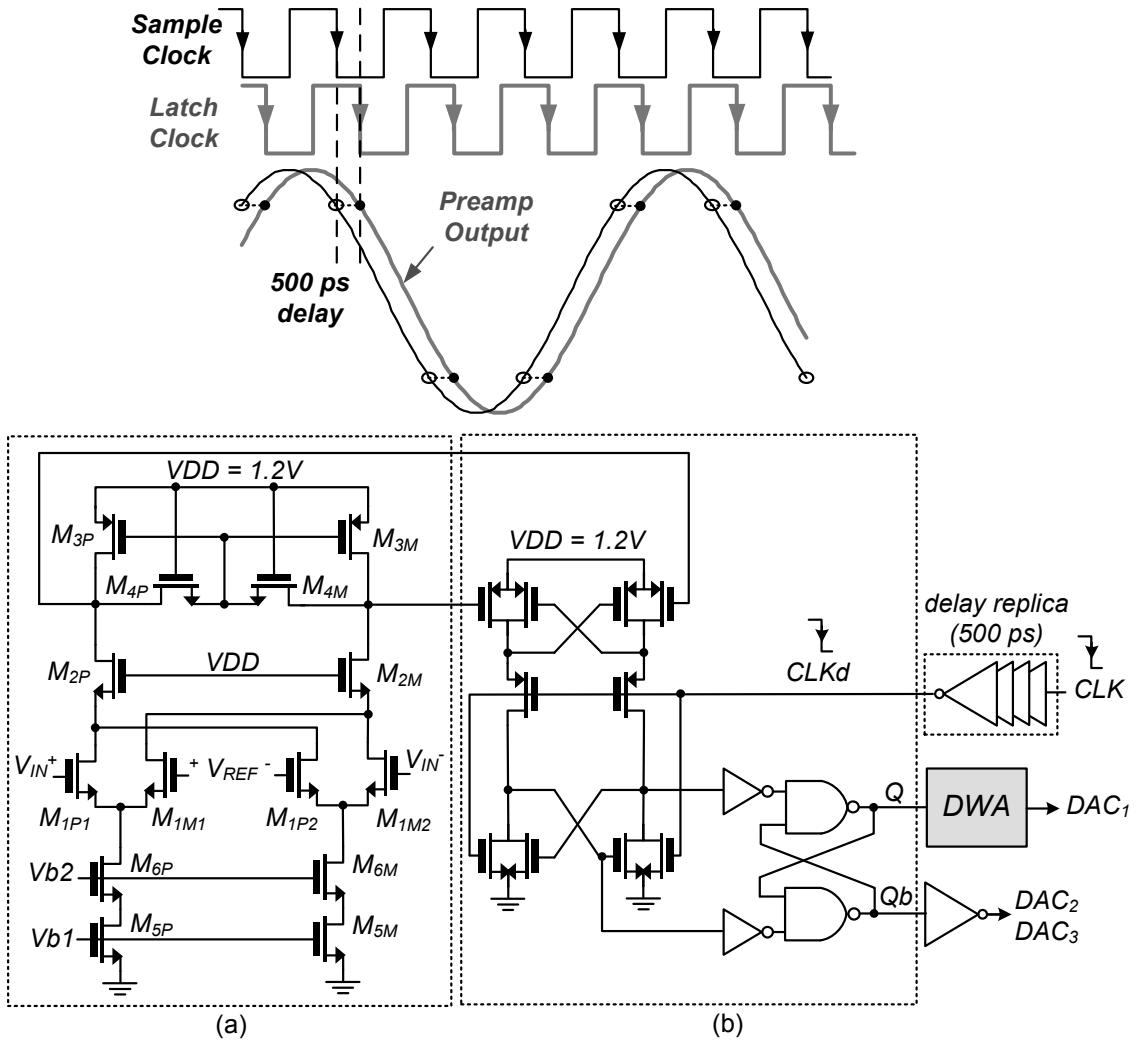
Figure 6.20: Comparator used in the Flash ADC: (a) preamplifier, (b) latch.

6.2.3 The 4-bit Flash ADC

The quantizer used in the modulator is a 4-bit Flash ADC. It consists of 15 comparators and a 16-element resistor string driven by a differential 600 mV +/- 150 mV external reference. The thermometer-coded output of the flash ADC is fed into a DWA block and then into the first-stage DAC. The second and third stage DACs are directly driven by the Flash quantizer. To correct for potential bubble errors in the Flash

ADC, the binary outputs are generated by a Wallace-Tree encoder made of 11 full-adders. The encoder is placed outside the modulator loop and is interfaced to the digital output pads. The schematics of the core building blocks of the quantizer and the thermometer-to-binary encoder are shown in Figures 6.20 and 6.21 respectively. The encoder data is reused in the DWA block for dynamic element matching of the main feedback DAC.

Each comparator consists of a pre-amplifier and a latch. The data in Figure 6.22 show the mean and standard deviation of the SNDR performance when the comparator offset standard deviation is varied from 0.1 to 1.0 LSB (LSB = 2^{-4} full-scale). A larger offset translates into lower mean and minimum (-3σ) SNDR due to an increasing in the quantizer nonlinearity. A standard deviation of a quarter-LSB for offsets ($\sigma = 2^{-6}$) will ensure around 84 dB and 81 dB average and worst-case SNDR, respectively. These values are acceptable for the targeted performance of 78 dB. Subsequently, the preamplifier devices were sized for $\sigma = 6$ mV random offset. This design target was verified by transistor-level Monte-Carlo simulations, as shown in Figure 6.23. Meeting the comparator offset requirement calls for large enough device sizes which result in large parasitic capacitance at the drain node of the input transistors. Small-size cascade transistors M2P and M2M (see Figure 6.20) isolate the pre-amp output from this parasitic capacitance and increase the bandwidth.

To avoid the issue of comparator meta-stability [31], two latches are cascaded at the output and the preamplifier gain-bandwidth product is made quite large. Long transient simulations followed by spectral analysis indicated that a 320 MHz bandwidth and a minimum DC gain of 5 for the pre-amplifier provide sufficient margin
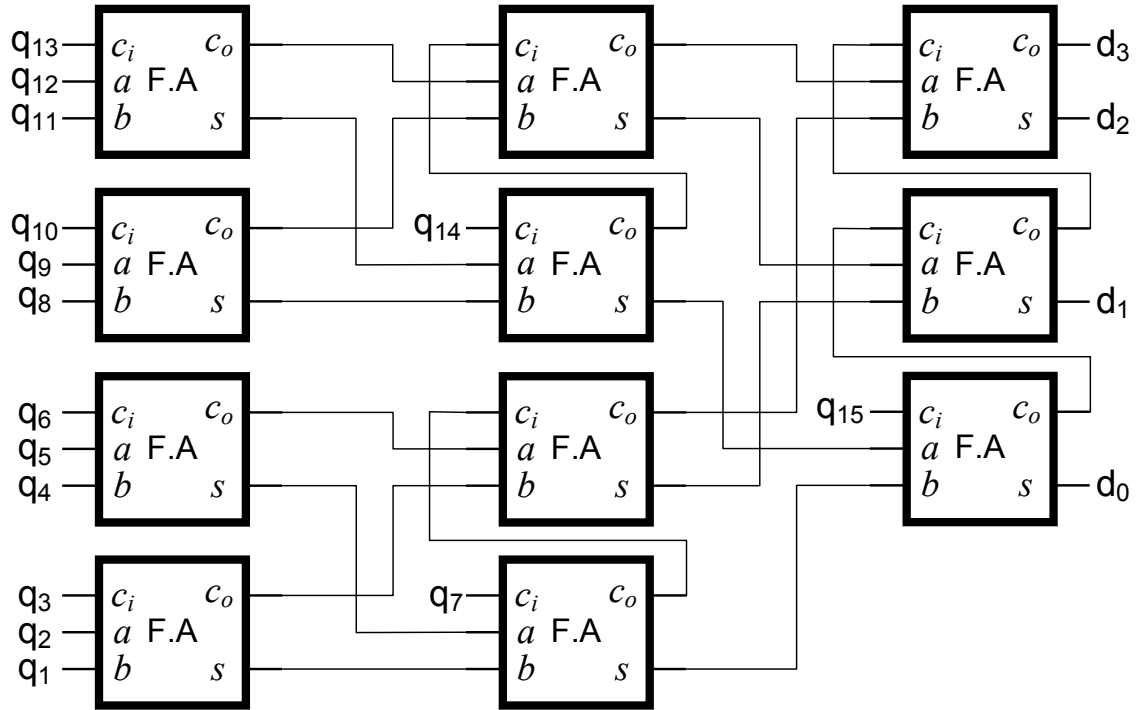
Figure 6.21: Wallace-Tree encoder used for thermometer-to-binary conversion.

for a safe operation. A comparison of the modulator output spectrum and its SNR is shown in Figure 6.24 for two different pre-amp bandwidths of 200 and 320 MHz.

Another critical issue related to the comparator design is the excess loop delay which can be caused by the finite bandwidth of the preamplifiers. This is shown conceptually in Figure 6.20 by a sinewave and its delayed version, where the latch strobe clock is delayed by the same amount to allow capturing the right sample. The relatively wide bandwidth of the pre-amplifier makes the group delay almost constant for the in-band signals. We have employed a replica pre-amp for delay generation to ensure supply, temperature and process corner tracking. A challenge associated with this technique is the increased speed requirement for the latch. Since the total delay of the comparator and DWA combination needs to be confined in half-a-sampling period,
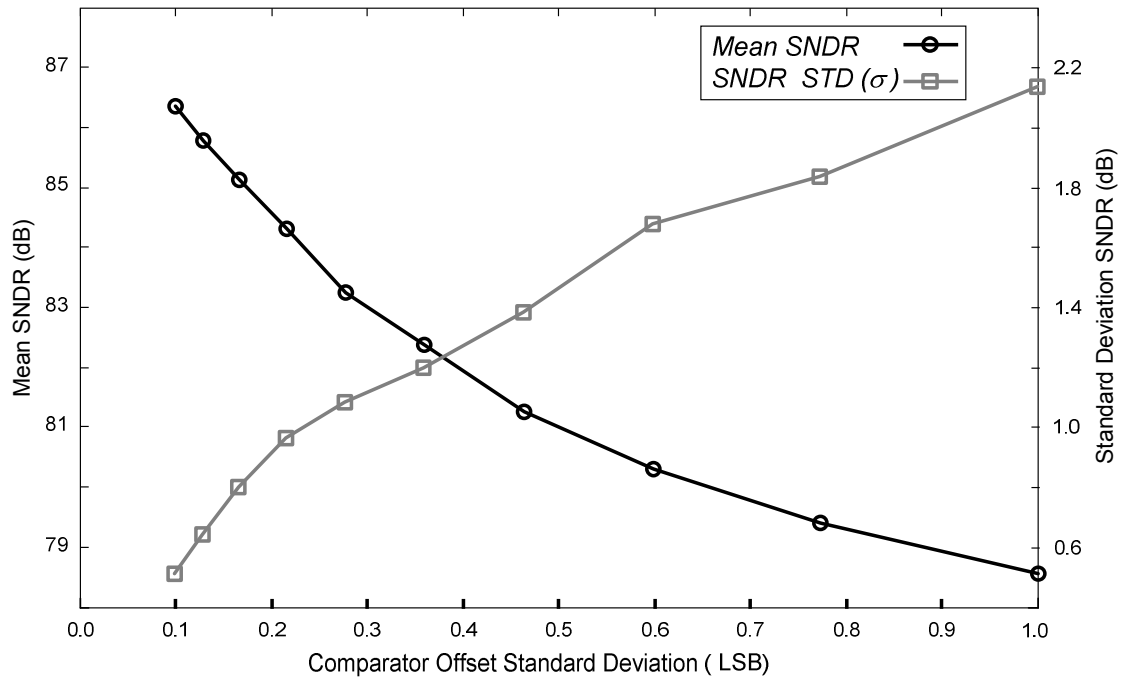
Figure 6.22: Effect of comparator offset standard deviation on modulator SNDR.
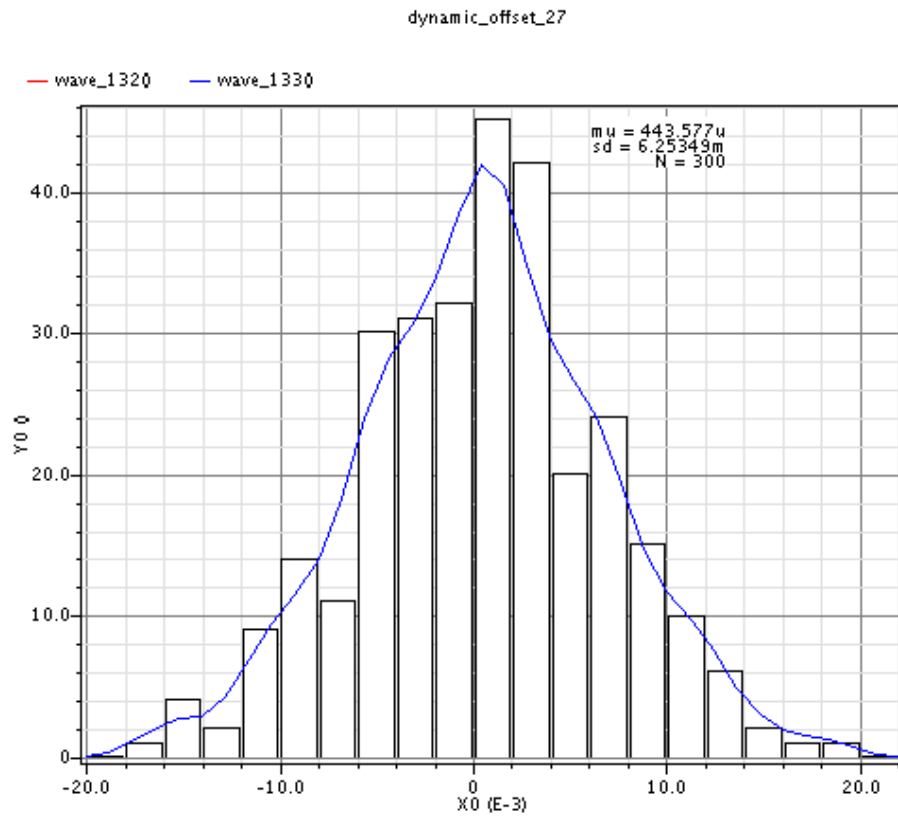
Figure 6.23: Monte-Carlo simulation of comparator input referred offset.

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delaying the strobe clock, subtracts from the response time available to the latch. In other words, the bandwidth of the pre-amp is relaxed at the expense of increasing the latch speed requirements. In the designed modulator, the delays of the comparator pre-amplifier and latch when resolving a ¼ LSB input were 500 ps and 750 ps respectively. Accordingly the latch strobe clock was delayed by 500ps to cover for the pre-amplifier delay. Also the DWA data path added another 900 ps delay, making the total latency of the feedback path 2.15 ns. This delay is sufficiently less than the required half sampling period of 3.125 ns

The total power consumption of the designed Flash ADC is 1.3 mW which is divided as 0.98 mW static and 0.32 mW dynamic power from a 1.2 V supply. In addition, a 31 uA current flows into the resistor string from a 0.3 V external reference buffer.
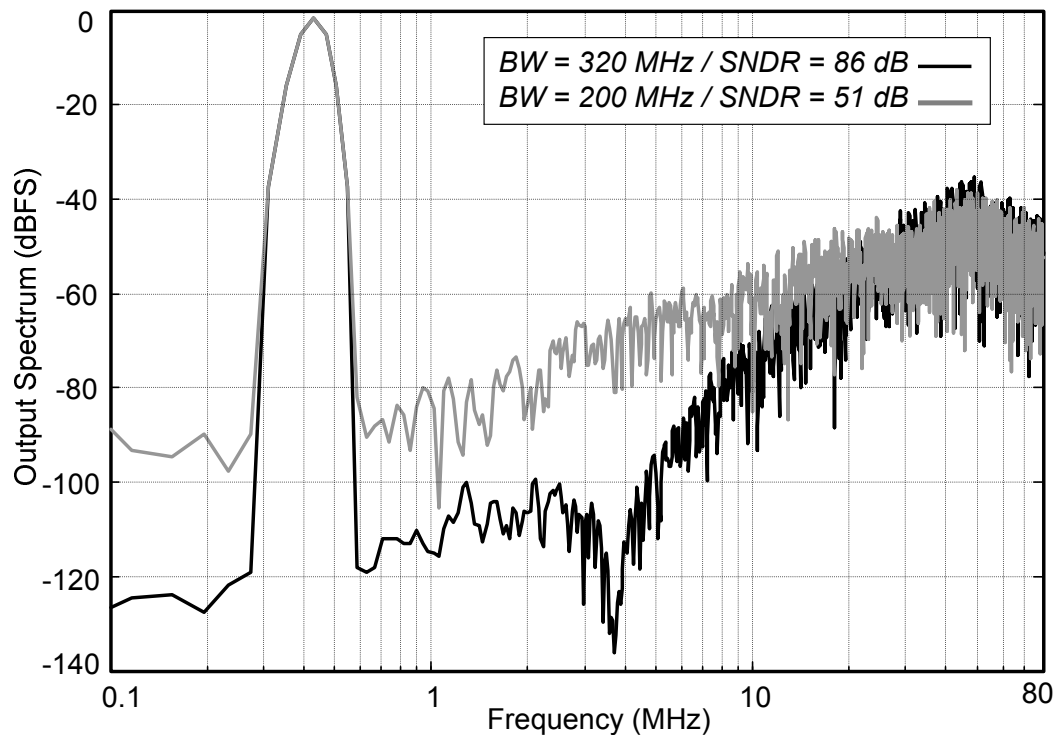
Figure 6.24: Simulated output spectrum versus preamplifier bandwidth.
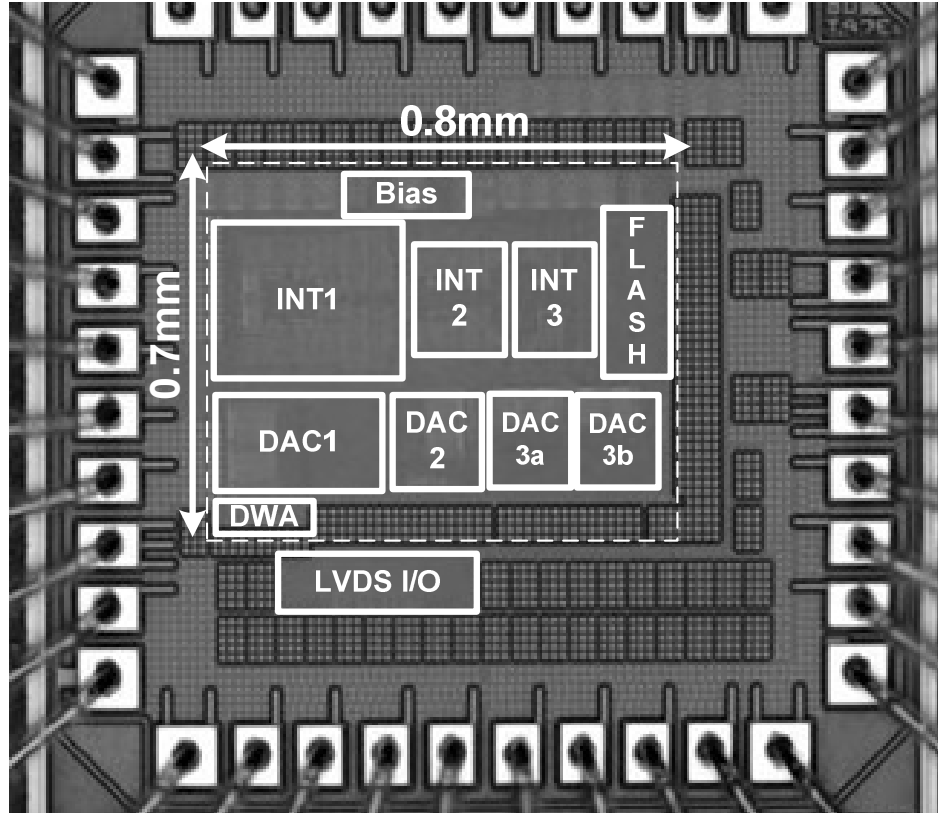
Figure 6.25: Microphotograph of the 5MHz CT-$\Delta\Sigma$ test chip.

6.3 Measurement Results

A prototype chip was fabricated in a 0.13um CMOS technology and encapsulated in a 40-pin plastic package. All the pins include ESD protection. The micro-photograph of the die is shown in Figure 6.25. The chip occupies 0.56 mm2 active area. A single 1.2 V supply is used for both analog and digital blocks. The test and measurement setup is shown in Figure 6.26. The modulator is externally clocked at 160 MHz. A 1.1 MHz sinewave was used for SNR/SNDR measurements and an additional 1.3 MHz tone was employed for two-tone measurements. Figure 6.27 shows the measured SNR / SNDR performance.
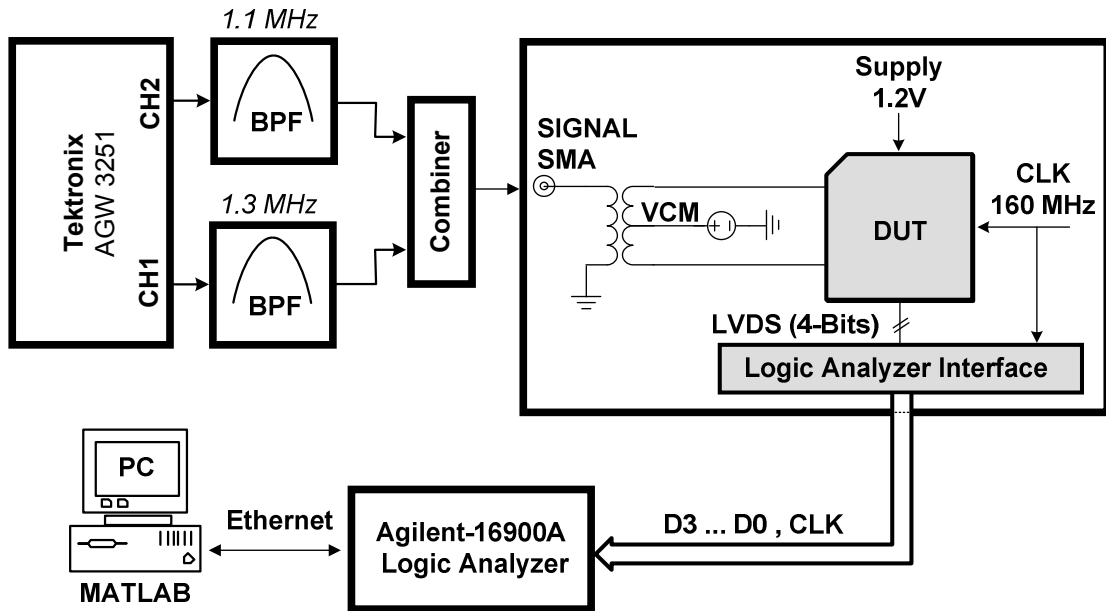
Figure 6.26: Test setup used in the measurements.
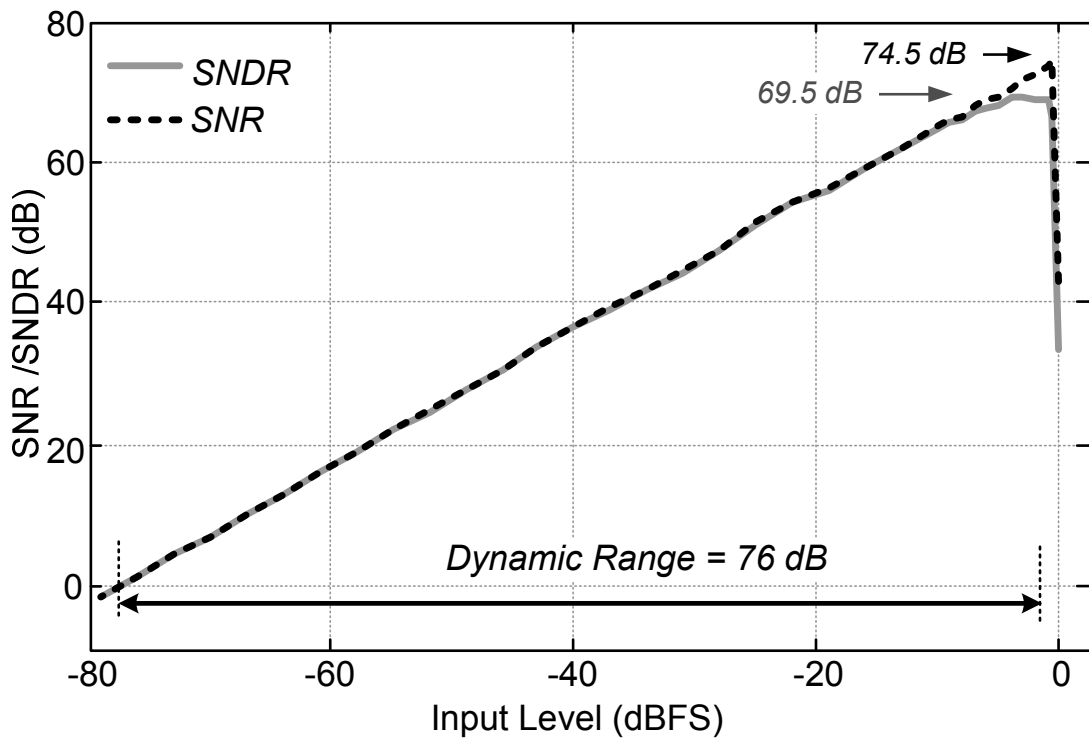
Figure 6.27: Measured SNR/SNDR performance versus input amplitude.
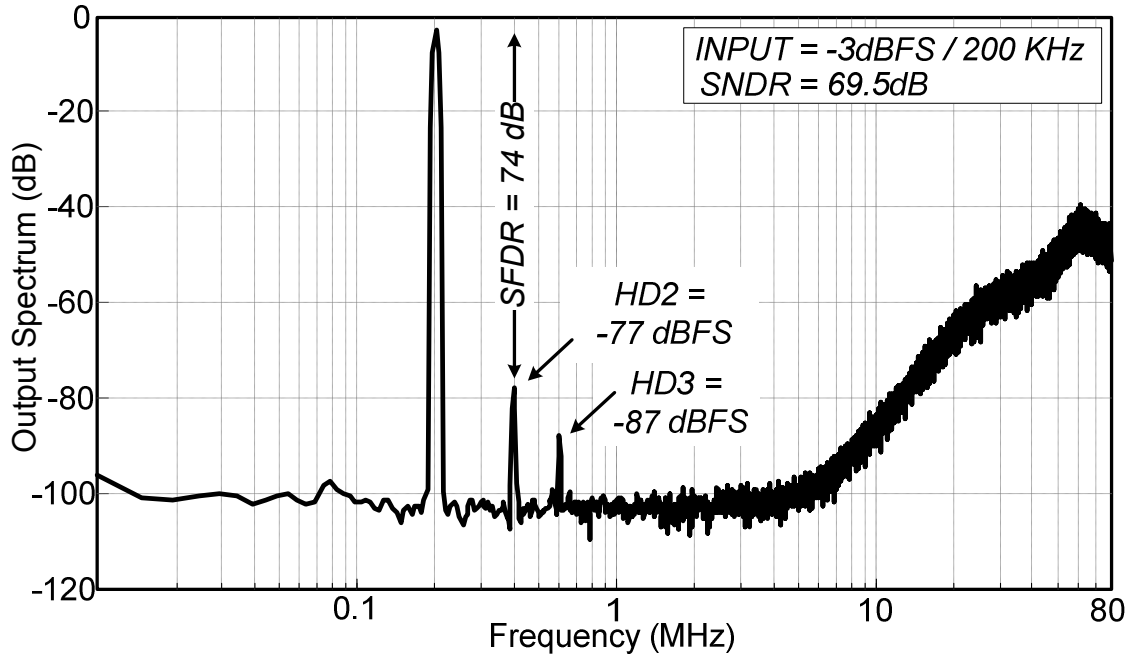
Figure 6.28: Measured output spectrum with -3dBFS tone at 200 KHz.

The modulator remains stable up to -0.5 dBFS where the SNR increases linearly by increasing the input amplitude. The modulator achieves 69.5 dB peak SNDR and 74.5 dB peak SNR for -3 dBFS and -0.5 dBFS input levels, respectively. The output spectrum for a -3dBFS input tone at 200 KHz is shown in Figure 6.28. The second-order harmonic distortion limits the SFDR of the modulator to 74 dB, while the third harmonic is at -87 dBFS for a -3 dBFS input signal. In the two-tone tests using -6 dBFS and -9 dBFS input levels, the modulator exhibits IM3 of 81 dB and 78 dB, respectively. In both cases, IM2 remains unchanged at -74 dBc as shown in Figure 6.29 plots. Both tests identify second-order harmonic distortion as the dominant source of nonlinearity. Post-fabrication study has identified the input resistor mismatch and layout asymmetry in the CMFB of the first amplifier as the root cause.
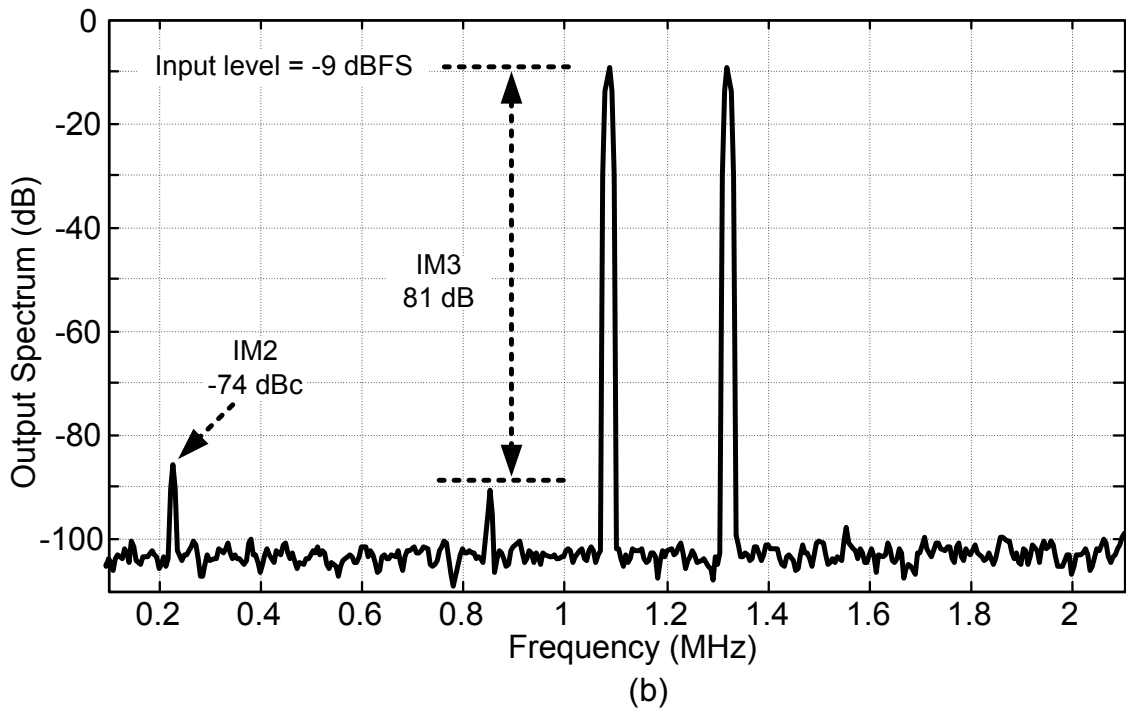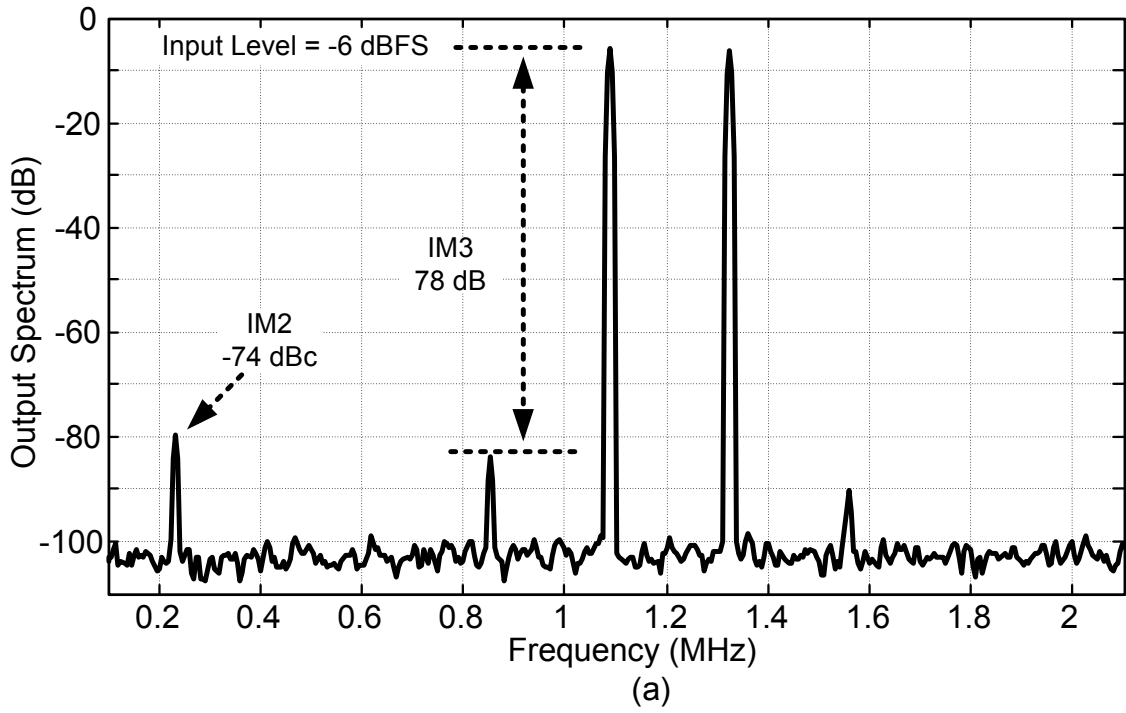
Figure 6.29: Two-tone test results with (a) -6 dBFS and (b) -9 dBFS inputs.
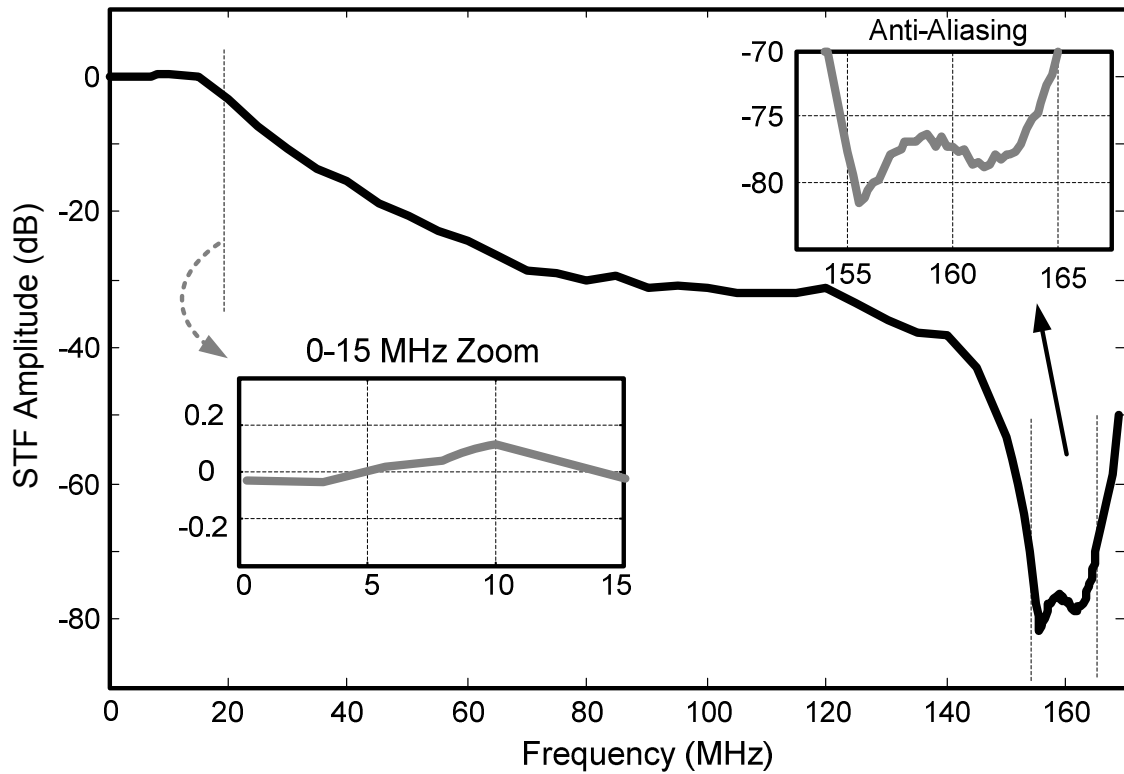
Figure 6.30: Measured output spectrum with -3dBFS tone at 200 KHz.

The modulator was designed for a target dynamic range of 76 dB while accounting for the device noise, the quantization noise, the noise and nonlinearity by DAC element mismatch, and nonlinearity caused by amplifier input stage and quantizer random offset. For a -3 dBFS input, the measured SNDR is 69.5 dB. The expected SNDR based on simulations was 70.2 dB after including measured HD2 and HD3 of, respectively, -77 and -87 dBFS. The 0.7 dB difference is attributable to unaccounted noise sources like, supply noise, unfiltered noise of the signal source, noise coupling through the test bench cables, and clock jitter. The estimated power of these extra noise sources is -81.7 dBFS.

Table 6.1: Performance Summary and Comparison

Specifications	Ref. [76]	Ref. [77]	Ref. [78]	Ref. [79]	This work
Architecture	FF-FB	FF	FF + Time Encoding	FF-FB	Dual-Feedback
Bandwidth (MHz)	20	10	20	25	5
Clock Freq. (MHz)	640	250	320	500	160
SNDR / SNR (dB)	74 / 76	65 / 68	61 / 63	63.5 / 64	69.5 / 74.5
Dynamic Range (dB)	80	71	63	70	76
Power (mW)	20	18	7	8.5	6
Anti-Aliasing (dB)	N/A	N/A	N/A	N/A	70
STF OOB Peaking	Yes	Yes	Yes	Yes	No
Process Technology	130nm	130nm	65 nm	90 nm	130 nm
Die Area (mm^2)	1.20	1.35	0.08	0.2	0.56
FOM (fJ/conversion)	122	486	170	138	246

* FOM=Power / (2$^.$ BW$^.$2^{ENOB})

The STF was characterized by sweeping the input signal frequency from 250 KHz to 155 MHz while the input level was -6 dBFS. Anti-aliasing is measured by applying a -6 dBFS sine wave at 1.1 MHz superimposed on a -6 dBFS out-of-band tone with frequency in the range of 155 to170 MHz.. The measured STF is plotted in Figure 6.36 which shows a low-pass response with maximum out-of-band peaking of 0.1 dB at 10 MHz and a minimum anti-aliasing of 70dB at 165 MHz. The measured power consumption is 6 mW from the 1.2V supply. A summary of the measured performance is provided in Table 6.1. The figure-of-merit (FOM) is 0.123 / 0.246 pJ/conversion, based on the measured DR / SNDR respectively. Table 6.1 also provides a comparison of this work with current state-of-the-art technology [77-79].

CHAPTER 7

CONCLUSION AND FUTURE WORK

This work aimed at exploring new ways of improving power efficiency and frequency response of CT $\Delta\Sigma$ modulators. The results of this research are three novel architectures that demonstrate good potential for low-power and wideband A/D conversion in wireless applications, e.g., 3G and 4G handsets.

The first architecture proposes the use of a power efficient quantizer like successive-approximation (SAR) instead of the commonly used Flash quantizer. The SAR architecture allows for increasing the quantizer resolution with smaller power and area penalty than the flash structure. The reduced out-of-band quantization noise of a higher resolution SAR enables using more aggressive noise shaping at lower over sampling ratios which is key for wideband $\Delta\Sigma$ A/D conversion.

The intrinsic latency of a SAR quantizer is a major obstacle that prevents its use in delay-sensitive CT $\Delta\Sigma$ modulator loops. In this work, the latency issue is addressed by employing a faster quantizer clock in addition to a direct feedback path to the quantizer input for full-period excess-loop-delay (ELD) compensation. The use of switched-capacitors (SC) technique allows for incorporating the delay-compensation DAC into the SAR quantizer which obviates the need for an explicit summing amplifier needed in classical ELD compensation.

A SAR quantizer with full-period conversion latency leaves no time for dynamic-element-matching (DEM), a popular means for ensuring DAC linearity. Although calibration could be an alternative in this case, we proposed the partial-data-

weighted-averaging (Partial-DWA) technique as a purely digital solution with less complexity. The Partial-DWA exploits the serial operation of a SAR to avoid the excess-loop-delay (ELD) problem while providing adequate linearity improvement.

As a proof of concept, a first-order CT-$\Delta\Sigma$ modulator with 5-bit SAR quantizer is designed and implemented in a 130 nm CMOS process which achieves 62 dB dynamic range over 1.92 MHz signal bandwidth meeting the requirements of the WCDMA standard. The prototype modulator draws 3.1 mW from a single 1.2 V supply and occupies 0.36 mm^2 of die area.

The second part of this research addresses the issue of STF out-of-and peaking. The STF peaking is troublesome in receiver design as it puts stringent requirements on the analog filters preceding the ADC. A new design methodology has been proposed to synthesize low-pass feedforward CT-$\Delta\Sigma$ modulators with peaking-free STF and without constraining the NTF. Based on the proposed method, the STF peaking of a feedforward modulator can ideally be eliminated by adding extra feed-in paths to all integrator inputs. However, this modified feedforward structure exhibits significant sensitivity such that STF peaking reappears and anti-aliasing degrades in the presence of coefficient variation due to component mismatch.

Two new architectures have been proposed which need fewer coefficients than the conventional feedforward structure and allow for implementing a low-pass STF. The first one, namely dual-feed-in topology requires only two feed-in paths for modulators of any order while using a single overall feedback. Anti-aliasing and out-of-band peaking show considerable improvement over the feedforward structure, although there remains some residual STF peaking and anti-aliasing degradation. For further

improvement the dual-feedback topology has been proposed which shows significantly better STF behavior compared to the dual-feed-in and traditional feedforward structures.

A comprehensive integrator model is proposed which allows analyzing various non-idealities encountered in real implementations such as, amplifier limited unity-gain-bandwidth (UGBW), amplifier parasitic input capacitance, series resistance in the feedback path, amplifier input-stage nonlinearity, capacitive inputs used for combining integration and addition in one stage. Based on this model the effect of amplifier UGBW and the integrator feedback resistance has been studied in a third-order dual-feedback modulator. The results show that the dual-feedback structure needs relatively small amplifier bandwidth in the first integrator for a stable and acceptable NTF and STF performance. Hence the power consumption of the dominant first-integrator can be reduced because of the reduced bandwidth requirements. The integrator model was essential to performing behavioral simulations and following out a top-down design approach in order to optimize the performance of the fabricated $\Delta\Sigma$ modulators.

For proof of concept, a third-order dual-feedback $\Delta\Sigma$ modulator was implemented in a 130 nm CMOS process. The modulator achieves 76 dB of dynamic range over 5 MHz signal bandwidth which meets the requirements of a DVB-H receiver or an LTE receiver using up to 10 MHz RF bandwidth. The modulator shows 77 dB anti-aliasing and negligible worst-case STF peaking of 0.1 dB. The measured power consumption of the modulator is 6 mW from a single 1.2 V and the die area is 0.56 mm^2.

7.1 Contributions

The contributions of this work can be summarized as follows

- Proposed a CT $\Delta\Sigma$ modulator architecture based on the power efficient SAR quantizer with built-in delay compensation, hence eliminating the explicit analog adder from the quantizer front-end and saving power and area.

- A novel 5-bit SAR A/D converter architecture with split 3bit-2bit DAC structure that reduces the total capacitance of the SAR by a factor of 4. In addition to immediate savings in chip area, the reduced input capacitance of the SAR can be leveraged to reduce the power consumption of the last integrator driving the quantizer.

- The partial-DWA technique is proposed for dynamic-element-matching in the SAR based modulator architectures. This DEM approach, despite conventional DWA, does not cause ELD problem, although at the expense of slight performance drop.

- A digital DLL based on a novel current-controlled delay element is designed to synthesize the high-speed clock of the SAR quantizer from the modulator sampling clock. This DLL uses a 6-bit current-mode DAC to control its tapped delay line and features a first-order digital low-pass filter in its control loop. The novel fully-differential delay element shows low sensitivity to supply noise, and can maintain the 50% duty cycle of its input by ensuring equal rise and fall times.

- Designed, implemented and tested a proof of concept first-order CT delta-sigma modulator based on the proposed SAR based architecture with a 1.92 MHz

bandwidth and 62 dB dynamic range and 3.1 mW power consumption for a WDCMA application.

- Proposed a methodology for synthesizing a low-pass and peaking free STF for feedforward modulators without constraining the NTF.

- Proposed the dual-feed-in modulator architecture with reduced sensitivity to coefficient mismatch. The dual-feed-in topology which needs a single feedback path is particularly suitable for multi-mode receiver applications where a reconfigurable DAC design becomes too complicated.

- Proposed the dual-feedback modulator architecture with significantly less sensitivity to coefficient mismatch. The sensitivity of a dual-feedback structure resembles that of a feedback structure with the use of only two feedback paths for any modulator order.

- Proposed a new and comprehensive integrator behavioral model which allows for modeling non-idealities such as amplifier limited UGBW and DC gain, the effect of parasitic input capacitance, the effect of switch resistance in the feedback path, and amplifier input stage nonlinearity. The model works with integrators having capacitive input paths where amplifier serves in part as an analog adder.

- Developed a methodology to determine the amplifier GBW requirements based on the use of the proposed integrator model and applied it to the third-order dual-feedback modulator. The results can be used to design stable dual-feedback CT $\Delta\Sigma$ modulators without overdesigning the amplifier bandwidth.

- Designed, implemented and tested a proof of concept third-order CT dual-feedback modulator with 5 MHz signal bandwidth and 76 dB dynamic range and 6 mW power consumption for a DVB-H receiver application.

7.2 Future Work

In this work we introduced three new CT $\Delta\Sigma$ modulator architectures and successfully implemented and tested two prototype designs. For further investigation and future work the following research topics are suggested

- Using asynchronous design for the SAR quantizer. The power efficiency of the SAR based architecture can be improved by employing an asynchronous design instead of the synchronous approach in the implemented modulator. The asynchronous design allows for running the SAR quantizer off the modulator sampling clock, hence obviating the need for a DLL in stand alone modulators. Also the combination of asynchronous operation with sub-radix-2 (non-binary) SAR algorithm can alleviate the element mismatch issue and improve the quantizer linearity.

- Using current-mode SAR architecture. Instead of using a switched capacitor SAR, a current-mode SAR can be employed and easily combined with the current-mode ELD compensation DAC, again without requiring an analog summer. This will potentially allow increasing the speed of the quantizer and achieve higher modulator bandwidths. Also it is well known that current-mode designs have better potential for low-voltage, which makes them attractive for future generations of process nodes with reduced supply voltage.

- Using background calibrated feedback DACs instead of the Partial-DWA. The use of Partial-DWA involves trading-off the ELD with required initial matching of the DAC unit elements. As a result the area of a DAC with Partial-DWA becomes larger than the one that uses full DWA, although none of the conventional DEM techniques can be used due to adding to ELD. Background calibration of the DAC elements results in smaller DAC size, without causing any delay in the modulator loop.

- Investigating the effect of amplifier UGBW in dual-feed-in modulators. The proposed integrator model provides a unique opportunity for investigating the effect of amplifier dynamics on any structure. Of particular interest would be a comparison of amplifier requirements in dual-feed-in and dual-feed-back structures.

- Design and implementation of a multi-mode modulator based on the dual-feed-in or dual-feedback architectures. Multi-mode and reconfigurable design of the CT ΔΣ modulators has become a trend recently. The dual-feed-in and dual-feed-back architectures provide a unique opportunity for these applications for two reasons. First and foremost they provide a robust low-pass STF with no out-of-band peaking which is an important and desirable feature in multi-mode applications. Secondly the modulator area will be considerably smaller since reconfigurable DACs tend to be complex and bulky.

- Using SAR or asynchronous SAR quantizer in conjunction with the dual-feedback or dual-feed-in architectures. Combining the SAR based modulator idea with robust STF dual-feed-in or dual-feedback architectures can further

improve the power efficiency of the modulators. Of particular interest would be to investigate the effect of a full-period delay of SAR quantizer on the required bandwidth by the amplifiers.

- Design of dual-feed-in or dual-feedback modulators employing background calibrated DACs. The increased DAC switching activity by employing DWA or other DEM techniques, introduces signal dependent glitches to the sensitive integrator summing nodes. Using background calibrated DACs is one way to avoid this issue which can result in improved SNDR performance.

APPENDIX A

ORDER OF THE ANTI-ALIASING FILTER

The proof of equation (2.3) is provided in this appendix. Figure A.1 shows an in-band tone, an alias tone and a low-pass anti-aliasing filter. Before filtering the input and alias amplitudes are P_{SIG} and P_{BLK} respectively. Assuming a Butterworth characteristics the magnitude response of the filter with corner frequency f_b (signal bandwidth) can be written as

$$|AA(f)|^2_{Butterworth} = \left(\frac{1}{1 + (f / f_b)^2} \right)^N \approx (f / f_b)^{-2N} \tag{A.1}$$

The dB magnitude of the filter is obtained from the above equation as

$$AA_{dB}(f) = -20N \log_{10}(f / f_b) \tag{A.2}$$

After sampling the attenuated alias tone will be folded back to the signal band, producing an spurious tone with the dB amplitude of

$$P_{spur} = P_{ALS} - 20N \log_{10}(f_{ALS} / f_b) \tag{A.3}$$
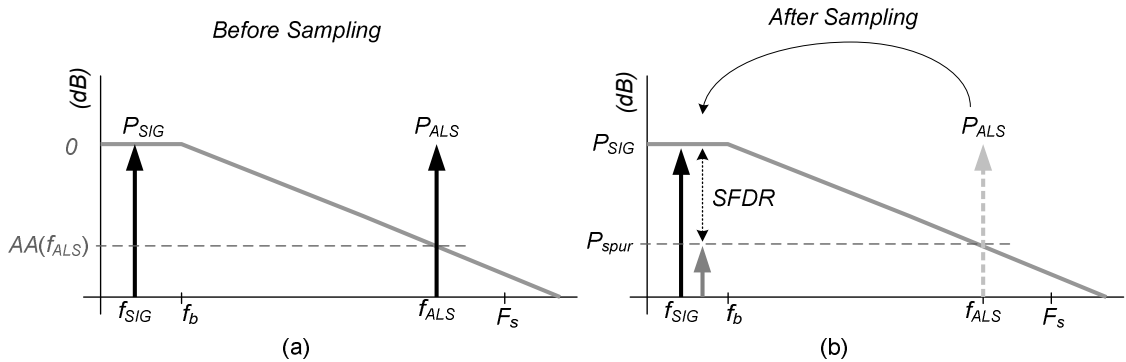
Figure A.1: Anti-aliasing filter and alias tone shown (a) before and (b) after sampling.

The minimum ant-aliasing occurs at frequency $f_{ALS} = F_s - f_b$. Therefore the worst case spurious power in dB becomes

$$P_{spur} = P_{ALS} - 20N \log_{10}(2OSR - 1) \tag{A.4}$$

Referring to Figure A.1(b) the equation of the SFDR can be written as follows

$$P_{spur} + SFDR = P_{SIG}$$
$$\Rightarrow \quad SFDR = P_{SIG} - P_{ALS} + 20N \log_{10}(2OSR - 1) \tag{A.5}$$

Using the above equation the order of the low-pass filter is estimated as

$$N_{Butterworth} = \left\lceil \frac{P_{ALS} + SFDR - P_{SIG}}{20 \log_{10}(2OSR - 1)} \right\rceil \tag{A.6}$$

In the above $\lceil x \rceil$ indicates the round up to $+\infty$ (ceil) operation. Assuming a full-scale signal with $P_{SIG} = 0$ dB, the filter order becomes

$$N_{Butterworth} = \left\lceil \frac{P_{ALS} + SFDR}{20 \ \log_{10}(2OSR - 1)} \right\rceil = \left\lceil \frac{P_{ALS} + SFDR}{6.02 \ \log_{2}(2OSR - 1)} \right\rceil \tag{A.7}$$

It is noted that the SFDR is usually required to be higher than the ADC dynamic range, so that the performance degradation due to aliasing is minimized. Therefore when assuming DR = SFDR the above equation only predicts the minimum order of the filter.

APPENDIX B

FULL-PERIOD QUANTIZER DELAY COMPENSATION

The proof of equation (4.6) is provided in this appendix. Suppose the goal is to find a transfer function $H'_d(z)$ and a scaling factor k_d such that it satisfies the following equation

$$H_d(z) = z^{-1}[k_d + H'_d(z)] \tag{B.1}$$

In the above, z^{-1} is the full period delay of the quantizer, k_d is the delay compensating direct feedback and $H_d(z)$ is the ideal DT loop transfer function which can be calculated knowing the modulator NTF. We assume that both $H_d(z)$ and $H'_d(z)$ are proper fractions (i.e. numerator order is less than denominator) and can be expressed in general form as

$$H_d(z) = \frac{\sum\limits_{i=0}^{N-1} b_i z^i}{z^N + \sum\limits_{i=0}^{N-1} a_i z^i} \tag{B.2}$$

$$H'_d(z) = \frac{\sum\limits_{i=0}^{N-1} b'_i z^i}{z^N + \sum\limits_{i=0}^{N-1} a'_i z^i} \tag{B.3}$$

In the above values of a'_i and b'_i are unknown. Plugging (B.2) and (B.3) in (B.1) yields

$$H_d(z) = \frac{\sum\limits_{i=0}^{N-1} b_i z^i}{z^N + \sum\limits_{i=0}^{N-1} a_i z^i} = z^{-1}\left(\frac{k_d z^N + \sum\limits_{i=0}^{N-1} (k_d a'_i + b'_i) z^i}{z^N + \sum\limits_{i=0}^{N-1} a'_i z^i} \right) \tag{B.4}$$

The equality in (B.4) can be re ordered as

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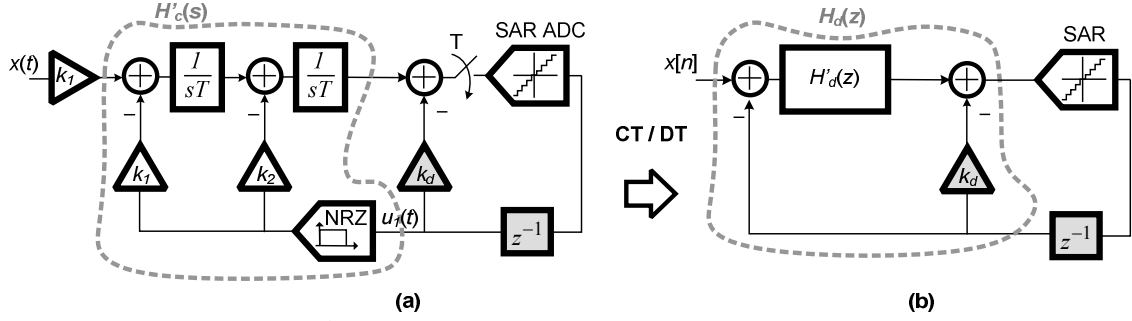
Figure B.1: (a) 2nd-order CT-ΔΣ modulator using SAR. (b) DT equivalent.

$$\frac{b_{N-1}z^{N-1} + \sum_{i=0}^{N-2} b_i z^i}{z^N + \sum_{i=0}^{N-1} a_i z^i} = \frac{k_d z^{N-1} + \sum_{i=0}^{N-2} (k_d a'_{i+1} + b'_{i+1})z^i + z^{-1}(k_d a'_0 + b'_0)}{z^N + \sum_{i=0}^{N-1} a'_i z^i} \tag{B.5}$$

To satisfy (B.5) both denominators and numerators must be equal. From the equality of denominators

$$z^N + \sum_{i=0}^{N-1} a_i z^i = z^N + \sum_{i=0}^{N-1} a'_i z^i \Rightarrow a_i = a'_i \big|_{0 \leq i \leq N-1} \tag{B.6}$$

Which means $H_d(z)$ and $H'_d(z)$ have the same poles by having the same denominators.

Also equating numerators results in

$$b_{N-1}z^{N-1} + \sum_{i=0}^{N-2} b_i z^i = k_d z^{N-1} + \sum_{i=0}^{N-2} (k_d a'_{i+1} + b'_{i+1})z^i + z^{-1}(k_d a'_0 + b'_0)$$

$$\Rightarrow \begin{cases} k_d = b_{N-1} \\ b_i = k_d a_{i+1} + b'_{i+1} & \Rightarrow b'_j = b_{j-1} - a_j b_{N-1} \quad (1 \leq j \leq N-1) \\ 0 = k_d a_0 + b'_0 & \Rightarrow b'_0 = -a_0 b_{N-1} \end{cases} \tag{B.7}$$

The above equation is the same as equation (4.6) in chapter 4. We use (B.7)

Example:

Consider the second order CT delta-sigma modulator shown in Figure B.1 with unknown coefficients k_1, k_2 and k_d. The goal is to calculated these coefficients

such that the modulator shows the classical 2nd order noise shaping of $(1 - z^{-1})^2$.

Knowing the NTF, the ideal DT loop filter is obtained as

$$H_d(z) = 1 - \frac{1}{NTF(z)} = \frac{-2z + 1}{z^2 - 2z + 1} = z^{-1}\left(k_d + H'_d(z)\right) \qquad \text{(B.8)}$$

Using (B.7) the coefficients of the delay-compensated loop filter are obtained as:

$$\begin{cases} k_d = b_1 = -2 \\ b'_1 = b_0 - a_1 b_1 = -3 \\ b'_0 = 0 - a_0 b_1 = 2 \end{cases} \Rightarrow \quad H'_d(z) = \frac{-3z + 2}{z^2 - 2z + 1} \qquad \text{(B.9)}$$

Assuming the CT prototype uses an NRZ DAC with a zero-th order hold (ZOH) transfer function and has an outer loop TF as $\left(\dfrac{k_1}{s^2} + \dfrac{k_2}{s}\right)$, the unknown coefficients

can be found by applying MATLAB's control toolbox function 'd2c' to the $H'_d(z)$ as:

$$-\left(\frac{k_1}{s^2} + \frac{k_2}{s}\right) = \text{d2c}(H'_d(z), 'zoh') = \frac{-(2.5s + 1)}{s^2} \qquad \text{(B.10)}$$

which yields $k_1 = 2.5$ and $k_2 = 1$.

$$**********************************$$

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APPENDIX C

ACTIVE-RC INTEGRATOR INPUT REFFERED NOISE

Let's consider the input referred noise of a general form integrator as shown in Figure C.1. This integrator includes a current mode DAC attached to amplifier summing node, a main resistive input path shown by R_1 and a secondary resistive input by R_2, and a nulling resistor R_z at the feedback path. Let's ignore the noise contribution of the current-mode DAC for now. The input referred noise of this integrator (without DAC) can be written as

$$\tilde{v}_{ni}{}^2 = \tilde{v}_{n1}{}^2 \left\{ 1 + \frac{1}{\tilde{v}_{n1}{}^2} \left(\tilde{v}_{n2}{}^2 \left| \frac{G_2}{G_1} \right|^2 + \tilde{v}_{n3}{}^2 \left| \frac{G_3}{G_1} \right|^2 + \tilde{v}_{n4}{}^2 \left| \frac{G_4}{G_1} \right|^2 \right) \right\} \qquad \text{(C.1)}$$

In the above G_i is the voltage gain of the *i-th* noise source to the output and the ratios of G_i to G_1 are obtained from the circuit shown in Figure C.1 as

$$\frac{G_2}{G_1} = R_1 \left(\frac{1}{R_2} \right)$$
$$\frac{G_3}{G_1} = R_1 \left(\frac{1}{R_z + 1/sC} \right) \qquad \text{(C.2)}$$
$$\frac{G_4}{G_1} = R_1 \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_z + 1/sC} \right)$$

An interesting note to take from the above equation is that the noise gain ratio is equal to the inverse of the impedance ratios for a given noise source.

Using the definitions in (C.2) the power of the input referred thermal noise can be expressed as
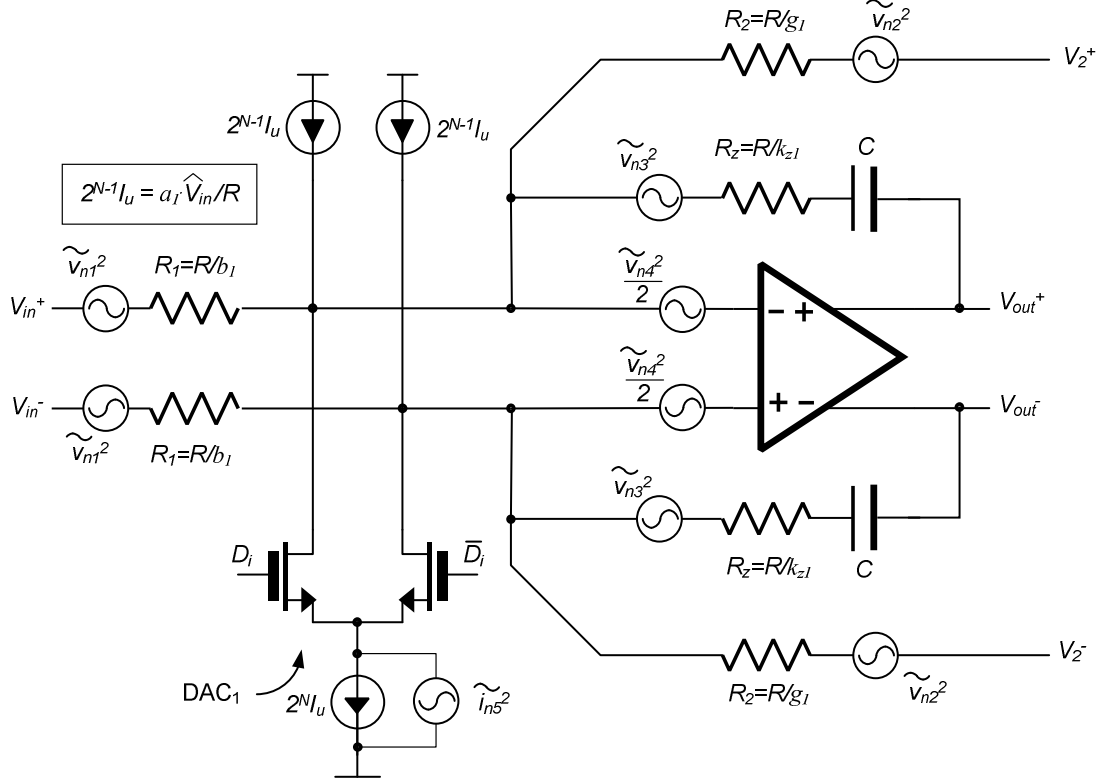
Figure C.1: The noise model of an Active-RC integrator.

$$S_{in-th} = \int_0^{f_B} \frac{\tilde{v}_{ni-th}^2}{\Delta f} df = 8KTR_1 \left\{ \underbrace{\int_0^{f_B} (1 + \frac{R_1}{R_2}) df}_{Part-A} + \underbrace{\int_0^{f_B} \frac{R_1 R_z}{|R_z + (1/j2\pi fC)|^2} df}_{Part-B} \right.$$

$$\left. + \underbrace{\int_0^{f_B} \frac{\eta_{th} R_1}{3 g_m} \cdot \left| \frac{1}{R_1 || R_2} + \frac{1}{R_z + (1/j2\pi fC)} \right|^2 df}_{Part-C} \right\} \qquad (C.3)$$

The first noise contribution (Part-A) is related to thermal noise of the input resistors R_1 and R_2 which becomes

$$S_{in-A} = 8KTR_1 \int_0^{f_B} (1 + \frac{R_1}{R_2}) df = 8KTR_1 f_B (1 + \frac{R_1}{R_2}) \qquad (C.4)$$

Also the second noise contribution (Part-B) is related to the thermal noise of the feedback resistor R_z. We use the following definitions to solve for part-B in (C.3)

$$\text{using} \begin{cases} RC = F_s^{-1} = (2f_bOSR)^{-1} \\ R = b_1R_1 \end{cases} \Rightarrow C = (2f_bR_1b_1OSR)^{-1} \qquad \text{(C.5)}$$

Therefore the input referred noise power due to R_z becomes

$$S_{in-B} = \frac{8KTR_1^2}{R_z} \int_0^{f_B} \frac{f^2}{f^2 + (b_1R_1f_bOSR/\pi R_z)^2} df \approx 8KTR_1f_B \cdot \underbrace{\left(\frac{R_z}{R_1} \cdot \frac{\pi^2}{3b_1^2OSR^2} \right)}_{\text{normalized } R_z \text{ effect}} \text{(C.6)}$$

In solving the integral in (C.6) we used the approximation $\tan^{-1}(x) \approx x - x^3/3$ for small x. Equation (C.6) indicates that the noise contribution of the feedback resistance becomes negligible at high OSRs. Nonetheless the effect of R_z needs to be carefully examined at low-OSR designs. In our design with *OSR=16, k₁=0.37, R₁=R/0.37*, and *Rz=R/5*, the normalized contribution of R_z (with respect to R_1) is 0.007 which can be easily ignored.

Part-C of equation (C.3) indicates the thermal noise contribution of the amplifier which can be simplified as

$$\begin{aligned} S_{in-C} &= 8KTR_1 \int_0^{f_B} \frac{\eta_{th}R_1}{3g_m} \cdot \left| \frac{1}{R_1 \| R_2} + \frac{1}{R_z + (1/j2\pi fC)} \right|^2 df \\ &= \frac{8KTR_1^2\eta_{th}}{3g_m(R_1 \| R_2)^2} \int_0^{f_B} \frac{[2\pi C(R_z + R_1 \| R_2)]^2 f^2 + 1}{(2\pi CR_z)^2 f^2 + 1} df \qquad \text{(C.7)} \\ &= 8KTf_B \cdot \frac{\eta_{th}}{3g_m} \left\{ (1 + \frac{R_1}{R_2})^2 + \underbrace{(1 + \frac{2R_z}{R_1 \| R_2}) \frac{\pi^2}{3OSR^2b_1^2}}_{\text{(effect of feedback } Z)} \right\} \end{aligned}$$

The above equation shows that the amplifier input referred noise depends on impedance network comprising the $R_1 \| R_2$, in parallel with the feedback impedance. Clearly the

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effect of the feedback impedance depends on OSR which can become significant at low oversampling rates. In our design with $OSR=16$, $b_1=0.37$, $R_1=R/0.37$, $R_2=R/0.04$ and $R_z=R/5$, the term including the feedback impedance effect is equal to 0.11 which can be ignored compared to R_1 and R_2 contributions. Assuming negligible contribution by feedback network, the part-C noise power is approximated as

$$S_{in-C} = 8KTR_1f_B \cdot \frac{\eta_{th}}{3R_1g_m}(1+\frac{R_1}{R_2})^2 \tag{C.8}$$

The combination of (C.5), (C.6) and (C.7) leads to the following total input referred noise power (again without accounting for DAC)

$$S_{nth1} = 8KTR_1f_B \left\{ 1 + \frac{R_1}{R_2} + \underbrace{\frac{R_{z1}}{R_1}\left(\frac{\pi^2}{3b_1^2 OSR^2}\right)}_{\text{effect of Rz}} + \right.$$
$$\left. + \frac{\eta_{th}}{3g_mR_1}\left[\left(1+\frac{R_1}{R_2}\right)^2 + \underbrace{\left(1+\frac{2R_{z1}}{R_1 \parallel R_2}\right)\frac{\pi^2}{3b_1^2 OSR^2}}_{\text{effect of Rz}} \right] \right\} \tag{C.9}$$

The noise contribution of DAC can be calculated by assuming that all noise current is integrated by the feedback capacitor. In this case the total noise current can be expressed in terms of the input resistor R_1 and single-ended peak voltage of the input as

$$\tilde{i}_{n_{DAC}}^2 = 4KTf_B\frac{2}{3}g_{m_{DAC}} \Rightarrow \tilde{v}_{n_{DAC}}^2 = 4KTf_B\frac{2}{3}g_{m_{DAC}} \cdot R_1^2 \tag{C.10}$$

The g_{mDAC} in the above is related to the single-ended full-scale DAC current which is directly proportional to the feedback coefficient a_1, the single-ended peak of the input voltage and the input resistance value R_1 and can be defined as

$$g_{m_{DAC}} = 4 \cdot (\frac{2I_{FS-se}}{\Delta V_{DAC}}) = \frac{8}{\Delta V_{DAC}} \cdot \frac{a_1\widehat{V}_{in-se}}{b_1R_1} \tag{C.11}$$

Hence equation (C.10) can be re-written as

$$\tilde{v}_{n_{DAC}}{}^2 = 8KTR_1 f_B \cdot \frac{a_1}{b_1} \cdot \left(\frac{8\widehat{V}_{in-se}}{\Delta V_{DAC}}\right) \tag{C.12}$$

It is noted that the above equation assumed a very large gain-bandwidth for the amplifier. In reality that is not the case, hence not all noise current gets integrated by the feedback capacitor. Therefore (C.12) is pessimistic and predicts the upper bond of the DAC noise. Adding (C.12) to (C.9) the total input referred noise power is obtained as

$$S_{nth1} = 8KTR_1 f_B \left\{ 1 + \frac{R_1}{R_2} + \underbrace{\frac{R_{z1}}{R_1}\left(\frac{\pi^2}{3b_1{}^2 OSR^2}\right)}_{\text{effect of Rz}} + \right.$$
$$\left. \frac{\eta_{th}}{3g_m R_1}\left[\left(1 + \frac{R_1}{R_2}\right)^2 + \underbrace{\left(1 + \frac{2R_{z1}}{R_1 \parallel R_2}\right)\frac{\pi^2}{3b_1{}^2 OSR^2}}_{\text{effect of Rz}}\right] + \frac{8\widehat{V}_{in}}{3\Delta V_{DAC}} \cdot \frac{a_1}{b_1} \right\} \tag{C.13}$$

With further simplification, assuming the contribution of Rz and the effect of feedback impedance can be ignored the input referred thermal noise power of the first integrator becomes

$$S_{nth1} = 8KTR_1 f_B \left\{ \left(1 + \frac{R_1}{R_2}\right) + \left(1 + \frac{R_1}{R_2}\right)^2 \cdot \frac{\eta_{th}}{3g_m R_1} + \frac{a_1}{b_1} \cdot \frac{8\widehat{V}_{in}}{3\Delta V_{DAC}} \right\} \tag{C.14}$$

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BIBLIOGRAPHY

[1] Y.L.Guillou, "Analyzing sigma-delta ADCs in deep-submicron CMOS technologies" RF Design, pp. 18–26, Feb. 2005.

[2] J. de la Rosa, "Sigma-Delta modulators: tutorial overview, design guide, and state-of-the-art survey," , *IEEE Trans. Circuits Syst. I, Regular Papers.*, vol. 58, no. 1, pp. 1 -21, Jan. 2011.

[3] S. Chen, R. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp.2669–2680, Dec. 2006.

[4] A. Abidi, "Direct-Conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1399–1410, Dec. 1999.

[5] M. W. Hauser, "Principles of Oversampling A/D Conversion," Journal Audio Engineering Society, Vol. 39, No. 1/2, January/February 1991, pp. 3-26.

[6] M. W. Hauser, and R. W. Brodersen, " Monolitic decimation filtering for custom delta-sigma A/D converters," *in Proc. 1988 IEEE Int. Conf. on Acoustics, Speech and Signal Processing* , Apr. 1988, pp. 2005-2008.

[7] A. B. Sripad and D. L. Snyder, " A necessary and sufficient condition for quantization errors to be uniform and white," *IEEE Trans. Acoustics, Speech and Signal Processing*, vol. 25, pp. 442-448, Oct. 1977.

[8] R. Schreier, and G. C. Temes*, Understanding Delta-Sigma Data Converters*. New York: IEEE Press, 2005.

[9] S. H. Ardalan and J. J. Paulos, " An analysis of nonlinear behavior in delta-sigma modulators," *IEEE Trans. Circuits Syst.*, vol. 34, pp. 593-603, Jun. 1987.

[10] G. D. Altinok, M. Al-Janabi and I. Kale, " A Describing Function based method for predicting the stability of higher-order high-pass $\Sigma-\Delta$ modulators," *in Proc. 2010 Conf. on Ph.D. Research in Microelectronics and Electronics* (*PRIME 2010*), pp. 1-4, July. 2010.

[11] K. Falakshahi, C. K. Yang, B. A. Wooley, " A 14-bit, 10-Msamples/s D/A converter using multibit $\Sigma\Delta$ modulation," IEEE J. Solid State Circuits, vol. 34, pp. 607-615, May 1999.

[12] B. H. Leung and S. Sutarja, " Multibit sigma-delta A/D converter incorporating a novel class of dynamic element matching techniques," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 39, no.1, pp. 35-51, Jan. 1992.

[13] R. Baird and T. Fiez, "Linearity enhancement of multibit $\Delta\Sigma$ A/D and D/A converters using data weighted averaging," *IEEE Trans. Circuits Syst. II,* vol. 42, pp.753-762, Dec. 1995.

[14] R. vanVeldhoven, "A triple-mode continuous-time $\Sigma\Delta$ modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2069-2076,Dec. 2003.

[15] Y. Matsuya et al., "A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping," *IEEE J. Solid-State Circuits*, vol. 22, pp. 921-929, Dec. 1987.

[16] L. Breems, R. Rutten, and G. Wetzker, "A cascaded continuous-time $\Sigma\Delta$ modulator with 67-dB dynamic range in 10-MHz bandwidth," IEEE J. Solid-State Circuits, vol. 39, pp. 2152-2160, Dec. 2004.

[17] O. Shoaei, "Continuous-time delta-sigma A/D converters for high speed applications.," Ph.D. dissertation, Carleton Univ., Ottawa, ON, Canada, 1995.

[18] M. Ortmanns, F. Gerfers and Y. Manoli,"A continuous-time $\Sigma\Delta$ modulator with reduced sensitivity to clock jitter through SCR feedback," *IEEE Trans. on Circuits ans systems-I: Regular Papers*, vol. 52, no. 5, pp. 875-884 , May 2005.

[19] E. L. Jury, Theory and Application of the Z-transform method. Huntington, NY: Robert Krieger Publishing Co., 1964.

[20] J. Cherry and W. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II,* vol. 46, no. 4, pp. 376-389, Apr. 1999.

[21] S. Pavan, "Excess loop delay compensation in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, pp. 1119-1123, Nov. 2008.

[22] M. Ortmanns, F. Gerfers and Y. Manoli, Compensation of finite gainbandwidth induced errors in continuous-time sigma-delta modulators, *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 6, pp. 1088-1099, June 2004.

[23] Frank Goodenough, "Analog technology of all varieties dominate ISSCC" *Electronic Design*, vol.44, no. 4, pp. 96-111, Feb. 1996.

[24] B. Murmann, "A/D converter trends: Power dissipation, scaling and digitally asssisted architectures," *in Proc. 2008 IEEE Custom Integrated Circuits Conf. (CICC) 2008*, pp. 105-112.

[25] Robert H. Walden, "Analog-to-digital converter survey and analysis," *IEEE Journal on Selected Areas in Communication*, vol. 17, no. 4, pp. 539-550, Apr. 1999.

[26] *Using SIMULINK Version 5.* : Mathworks Inc., 2002, Mathworks.

[27] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 315-325, Mar. 1999.

[28] *MATLAB Statistics Toolbox Version 3.* : Mathworks Inc. , 2001, Mathworks.

[29] L. R. Carley, R. Schreier, and G. Temes, "Delta-sigma ADCs with multibit internal converters," in *Delta-Sigma Data Converters:Theory, Design and Simulation*, S. R. Norsworthy, R. Schreier, and G.C. Temes, Eds. New York: IEEE Press, 1997, ch. 8.

[30] O. Oliaei, H. Aboushady, " Jitter effects in continuous-time Sigma-Delta modulators with delayed return-to-zero feedback," in *IEEE International Conference on Electronics, Circuits and Systems* (*ICECS-1998*), pp. 351-354, Sep. 1998.

[31] J. Cherry and W. Snelgrove, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," *IEEE Trans. Circuits Systems II, Analog Digit. Signal Process.*, vol. 46, pp. 661-676, Jun. 1999.

[32] L. Risbo, "$\Sigma\Delta$ Modulators - Stability and Design Optimization," PhD dissertation, Technical University of Denmark, 1994.

[33] K. Reddy and S. Pavan, "Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter," *IEEE Trans. Circuits Syst.I, Reg. Papers*, vol. 54, pp. 2184-2194, Oct. 2007.

[34] R. Tortosa, J. M. de la Rosa, A. Rodriguez-Vazquez and F. V. Fernandez, "Analysis of clock jitter error in multibit continuous-time $\Sigma\Delta$ modulators with NRZ feedback waveform" in *Proc. Int. Symp. Circuits and Systems* (*ISCAS-2005*), May 2005, pp.3103-3106.

[35] O. Oliaei, "Sigma-Delta modulator with spectrally shaped feedback," *IEEE Trans. Circuits Syst. II* : *Analog and digital Signal Processing ,* vol. 50, no. 9, pp. 518-530, Sep. 2003.

[36] B. M. Putter, "$\Sigma\Delta$ ADC with finite impulse response feedback DAC," in *IEEE ISSCC Dig. Tech. Papers*, February 2004, pp. 76-77.

[37] F. Colodro and A. Torralba, "New continuous-time multibit sigma-delta modulators with low sensitivity to clock jitter," *IEEE Trans. on Circuits and Systems, TCAS-I: Regular Papers*, vol.56, no. 1, pp. 74-83, Jan. 2009.

[38] M. Z. Straayer, and M. H. Perrrott, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time DS ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.

[39] V. Dhanasekaran et al.,"A 20 MHz BW 68 dB DR CT-ΔΣ ADC based on a multi-bit time-domain quantizer and feedback element," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 174–175.

[40] S. Paton, A. Di Giandomenico, L. Hernandez, A. Wiesbauer, P. Potscher, and M. Clara, "A 70-mW 300-MHz CMOS continuous-time ΣΔ ADC with 15-MHz bandwidth and 11 bits of resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1062, Jul. 2004.

[41] S. Yan, and E. Sanchez-Sinencio, "A continuous-time ΔΣ modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no.1, pp. 75–86, Jan. 2004.

[42] N. Yaghini, D. Johns, "A 43mW CT Complex ΔΣ ADC with 23MHz of Signal Bandwidth and 68.8dB SNDR," *ISSCC Dig. Tech. Papers*, pp. 502-504, Feb., 2005.

[43] Z. Li and T. Fiez, "A 14 bit continuous-time delta-sigma A/D modulator with 2.5 MHz signal bandwidth," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1873–1883, Sep. 2007.

[44] Y. S. Shu, B. S. Song, and K. Bacrania, "A 65 nm CMOS CT ΔΣ modulator with 81 dB DR and 8 MHz BW auto-tuned by pulse injection," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp. 500-501.

[45] K. Matsukawa, Y. Mitani, M. Takayam, K. Obata, S. Dosho, and A. Matsuzawa, "A Fifth-Order Continuous-Time Delta-Sigma Modulator With Single-Opamp Resonator," *IEEE J. Solid-State Circuits*, vol.45, no. 4, pp. 697-706, Apr. 2010.

[46] M. Kappes, "A 2.2-mW CMOS bandpass continuous-time multibit ΣΔ ADC with 68 dB of dynamic range and 1-MHz bandwidth for wireless applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp.1098–1104, Jul. 2003.

[47] P.Dorrer, F.Kuttner, P.Greco, P.Torta, and T.Hartig, "A 3-mW 74-dB SNR 2-MHz Continuous-Time Delta-Sigma ADC With a Tracking ADC Quantizer in 0.13-um CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no.12, pp. 2416–2427, Dec. 2005.

[48] Y. Cheng, C. Petrie, B. Nordick, D. Comer, and D. Comer, "Multibit Delta-Sigma Modulator with Two-Step Quantization and Segmented DAC, " *IEEE Trans. Circuits Syst. II*, vol. 53, no. 9, pp. 848-852, Sep. 2006.

[49] S. Chen, R. Brodersen, "A 6-bit 600-MS/s 5.3-mW Asynchronous ADC in 0.13-um CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp.2669–2680, Dec. 2006.

[50] O.Oliaei, "Design of Continuous-Time Sigma-Delta Modulators With Arbitrary Feedback Waveform," *IEEE Trans. Circuits Syst. II,* vol. 50, no. 8, pp. 437-444, Dec 2003.

[51] L. J. Breems, E. J. van der Zwan, and J. H. Huijsing, "Design for Optimum Performance-to-Power Ratio of a Continuous-time ΣΔ Modulator," in *Proc. 25ᵗʰ Eur. Solid-State Circuits Conf.* (*ESSCIRC*) *1999*, pp.318-321.

[52] B. Fotouhi, D.A. Hodges, "High-resolution A/D conversion in MOS/LSI," *IEEE J. Solid-State Circuits*, vol. 14, no.6, pp. 920–926, Dec. 1979

[53] A. Van den Bosch, M. Steyaert, and W. Sansen, "An accurate statistical yield model for CMOS current-steering D/A converters," in *Proc. IEEE ISCAS*, 2000, pp. 105-108.

[54] M.Boussaa, Y.Audet, "A 1.6 GHz Digital DLL for Optical Clock Distribution," in *Proc. IEEE NEWCAS Conf. 2005*, pp.131-134.

[55] S. Ouzounov, R. van Veldhoven, C. Bastiaansen, K. Vongehr, R. van Wegberg, G. Geelen, L. Breems, and A. van Roermund, "A 1.2 V 121-mode CT delta-sigma modulator for wireless receivers in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, February 2007, pp. 242-243.

[56] Yi Ke, P. Gao, J. Craninckx, G. Van der Plas, and G. Gielen "A 2.8-to-8.5mW GSM/Bluetooth/UMTS/DVB-H/WLAN Fully Reconfigurable CT ΔΣ with 200kHz to 20 MHz BW for 4G radios in 90nm Digital CMOS," *IEEE Symp. VLSI Circuits* (*VLSIC*) *2010*, pp.153-154, June 2010.

[57] P. Crombez, G. Van der Plas, M.S.J. Steyaert, and J. Craninckx, "A Single-Bit 500 kHz-10 MHz Multimode Power-Performance Scalable 83-to-67 dB DR CT DS for SDR in 90 nm Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no.6, pp.1159-1171, June 2010.

[58] K. Philips, P. A. C. M. Nuijten, R. L. J. Roovers, A. H. M. van Roermund, F. Muñoz Chavero, M. T. Pallarés, and A. Torralba , "A continuous-time Σ−Δ ADC with increased immunity to interferers," *IEEE J. Solid-State Circuits*, vol.39, pp. 2170-2178, Dec. 2004.

[59] L. Breems and J. Huijsing, , *Continuous-Time Sigma Delta Modulation for A/D Conversion in Radio Receivers*. Dordrecht, The Netherlands: Kluwer Academic Publishers, 2001.

[60] J.Silva, U.Moon, J.Steensgaard, and G.Temes, "Wideband low-distortion delta-sigma ADC topology', *Electronic Letters*, 2001, vol.37, pp. 737-738.

[61] E.Munoz, K.Philips, A. Torralba, "A 4.7mW 89.5dB DR CT complex sigma delta ADC with built-in LPF," *ISSCC Dig. Of Technical Papers* , pp. 500-501, Feb. 2005.

[62] M. Keller, M. Buhmann, F. Gerfers, M. Ortmanns, and Y. Manoli, "On the Implicit Anti-Aliasing Feature of Continuous-Time Cascaded Sigma-Delta Modulators", *IEEE Trans. Circuits Syst. I, Regular Papers.*, vol. 54, p.2639 , 2007.

[63] B. Benabes, M. Keramat and R. Kielbasa, "A methodology for designing continuous-time sigma-delta modulators," in *Proc. 1997 Europ. Design Test Conf.*, vol. 1, pp. 46-50

[64] S. Loeda, H. M. Reekie and B. Mulgrew, On the design of highperformance wideband continuous-time sigma-delta converters using numerical optimization, *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol.53, no. 4, pp. 802-810, April 2006.

[65] J.Maeyer, J.Raman, P.Rombouts, and L.Weyten" Controlled behavior of STF in CT $\Sigma-\Delta$ modulators", *Electronics Letters*, vol.41, Aug. 2005.

[66] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Trans. Circuits Syst. II,* vol. 40, no. 8, pp.461-466, Aug 1993.

[67] *MATLAB Control Toolbox Version 3.* : Mathworks Inc. , 2001, Mathworks.

[68] K. Ogata, *Discrete-Time Control Systems*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1997.

[69] M. Ranjbar, A. Mehrabi and O.Oliaei, "Continuous-time feed-forward $\Sigma\Delta$ modulators with robust signal transfer function," *in Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)* 2008, pp. 1878-1881.

[70] B.Xia, S.Yan, E.Sanchez "An RC time-constant auto-tuning structure for high-linearity continuous-time $\Sigma-\Delta$ modulators and active filters" *IEEE Trans. Cicuits Syst. II*, vol.51, pp. 2179-2188 Nov. 2004.

[71] M. Keller, A. Buhmann, J. Sauerbrey, M. Ortmanns, and Y. Manoli, "A comparative study on excess loop delay compensation techniques for continuous-time sigma-delta modulators," *IEEE Trans. Circuits Syst. I, Regular Papers.*, vol. 55, no. 11, pp. 3480-3487 , Nov. 2008.

[72] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 48, no. 9, pp. 1041–1056, Sep. 2001.

[73] P. Allen, D. Holberg, *CMOS Analog Circuit Design*, New York, USA : Oxford University Press, 2002.

[74] W. Sansen, *Analog Design Essentials*. Dordrecht, The Netherlands: Springer, 2006

[75] P. Sankar and S. Pavan, "Analysis of integrator nonlinearity in a class of continuous-time Delta-Sigma modulators," *IEEE Trans. Circuits Syst.II, Exp. Briefs*, vol. 54, pp. 1125-1129, Dec. 2007.

[76] G. Mitteregger, C. Ebner, S. Meching, T. Blon, C. Holuigue, and E. Romani , "A 20 mW 640-MHz CMOS continuous-time ΣΔ ADC with 20 MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB*," IEEE J. Solid-State Circuits,* vol. 41, no. 12, pp. 2641–2649,Dec. 2006.

[77] H. Kim, J. Lee, T. Kopani, S. Bazarjani, S. Kiaei, and B. Bakkaloglu, "Adaptive Blocker Rejection Continuous-Time ΣΔ ADC for Mobile WiMAX Applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2766–2779, Oct. 2009.

[78] E. Prefasi, S. Paton and L. Hernandez, "A 7 mW 20 MHz BW time-encoding oversampling converter implemented in a 0.08 mm 65 nm CMOS circuit," *IEEE J. of Solid-State Cicuits*, vol. 46, no. 7, pp. 1562-1574, July 2011.

[79] J. G. Kauffman,P. Witte, J. Becker, and M. Ortmanns, " An 8.5 mW continuous-time ΣΔ modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR," *IEEE J. of Solid-State Circuits*, vol. 46, no. 12, pp. 2869-2881, Dec. 2011.