微处理器体系结构级测试程序自动生成技术

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Abstract

In this paper, a novel specification driven and constraints solving based method to automatically generate test programs from simple to complex ones for advanced microprocessors is presented, and its prototype sytem——MA2TG (microprocessor architectural automatic test program generator) is introduced. It can generate not only random test programs but also a sequence of instructions target to specific constraints. The proposed methodology makes three important contributions. First, it simplifies the microprocessor architecture modeling and eases adoption of architecture modification via Architecture Description Language (ADL) specification. Second, it generates test programs for specific constraints utilizing the power of state-of-art constraints solving techniques. Finally, the size of the test program for microprocessor verification and the verification time are dramatically reduced. MA2TG has been applied on DLX processor and the embedded microprocessor EStar to illustrate the usefulness of the approach.

摘要

提出了一种由体系结构描述驱动的基于约束求解的微处理器体系结构级测试程序自动生成的新方法,并基于此开发了原型系统——MA2TG (microprocessor architectural automatic test program generator).该系统不仅可以随机生成测试程序,最主要的是可以产生针对特定要求的测试程序.其优点在于:首先,通过体系结构语言描述简化了体系结构建模,方便了对目标处理器体系结构的探索;第二,利用比较成熟的约束求解技术来生成满足需求的测试程序;第三,极大地缩减了测试程序的大小以及微处理器的验证时间.MA2TG已应用于DLX处理器和自主开发的EStar嵌入式微处理器的验证.实验结果表明了此方法的有效性.

References:

[1] Bergeron J. Writing Testbenches: Functional Verification of HDL Models. Boston: Kluwer Academic Publishers, 2000.

[2] Dill DL. What's between simulation and formal verification? In: Proc. of the 35th Design Automation Conf. San Francisco: ACM Press, 1999. 328-329.

[3] O'Krafka B, Mandyam S, Kreulen J, Raghavan R, Saha A, Malik N. MPTG: A portable test generator for cache-coherent multiprocessors.

In: Meitz RO. Proc. of the 14th Annual Int'l Phoenix Conf. on Computers and Communications. Scottsdale: IEEE Service Center, 1995. 38-44.

[4] Aharon A, Goodman D, Levinger M, Lichtenstein Y, Malka Y, Metzger C, Molcho M, Shurek G. Test program generation for functional verification of powerPC processors in IBM. In: Proc. of the 32nd Design Automation Conf. San Francisco: ACM Press, 1995. 279-285.

[5] Chandra A, Iyengar V, Jameson D, Jawalekar R, Nair I, Rosen B, Mullen M, Yoon J, Armoni R, Geist D, Wolfsthal Y. AVPGEN-A test generator for architecture verification. IEEE Trans. on Very Large Scale Integration (VLSI) Systems, 1995, 3(2):188-200.

[6] Rubin S, Levinger M, Pratt RR, Moore WP. Fast construction of test-program generators for digital signal processors. In: Proc. of the IEEE Int'l Conf. on Acoustics, Speech, and Signal Processing, Vol 4, Phoenix: Omni Press, 1999. 1989-1992.

[7] Malik N, Roberts S, Pita A, Dobson R. Automaton: An autonomous coverage-based multiprocessor system verification environment. In: Proc. of the 8th IEEE Int'l Workshop on Rapid System Prototyping. IEEE Computer Society, 1997. 168-172.

[8] Aharon A, Bar-David A, Dorfman B, Gofman E, Leibowitz M, Schwartzburd V. Veryfication of the IBM RISC System/6000 by a dynamic biased pseudo-random test program generator. IBM Systems Journal, 1991,30(4):527-538.

[9] Wu LM, Wang KC, Chiu CY. A BNF-Based automatic test program generator for compatible microprocessor VADL. ACM Trans. on Design Automation of Electronic Systems, 2004,9(1):105-132.

[10] Mishra P, Dutt N. Graph-Based functional test program generation for pipelined processors. In: Proc. of the 2004 Design Automation and Test in Europe Conf. and Exposition (DATE 2004). Paris: IEEE Computer Society, 2004. 182-187.

[11] Kumar V. Algorithms for constraint-satisfaction problems: A survey. AI Magazine, 1992,13(1):32-44.

[12] Halambi A, et al. 2004. http://www.cs.toronto.edu/~gkatsi/efc/README

[13] Grun P, Halambi A, Khare A, Ganesh V, Dutt N, Nicolau A. Expression: An ADL for system level design exploration. Technical Report, 98-29. Irvine: University of California, 1998.

[14] Bashford S, Bieker U, Harking B, Leupers R, Marwedel P, Neumann A, Voggenauer D. The MIMOLA Language Version 4.1. University of Dortmund, 1994.

[15] Freericks M. The nML Machine description formalism. Technical Report, Technische Universitat Berlin, Fachbereich Informatik, 1991.

[16] Pees S, Hoffmann A, Zivojnovic V, Meyr H. LISA: Machine description language for cycle-accurate models of programmable DSP architecture. In: Proc. of the 36th ACM/IEEE Conf. on Design Automation. New York: ACM Press, 1999. 933-938.