

论文

基于FPGA的CCSDS图像数据压缩系统的设计

陈哲<sup>1</sup>, 涂国防<sup>1</sup>, 张灿<sup>1,2</sup>, 陈德元<sup>1</sup>

- 1. 中国科学院研究生院信息科学与工程学院, 北京 100049;
- 2. 中国科学院研究生院信息安全国家重点实验室, 北京 100049

摘要:

针对CCSDS图像数据压缩(IDC)标准,提出了一种基于FPGA的CCSDS IDC并行实现方案.该方案包括离散小波变换(DWT)、直流系数量化编码、位平面编码(BPE)、码字拼接等4个模块.位平面编码模块采用了并行扫描、并行编码的快速算法,以提高编码速度.仿真结果表明了本方案的可行性和有效性,处理时间比现有的CCSDS IDC串行编码改进方法减少了13.6%,适用于空间通信的图像数据压缩编码.

关键词: CCSDS 图像压缩编码 并行编码 FPGA

Design of CCSDS image compression system based on FPGA

CHEN Zhe<sup>1</sup>, TU Guo-Fang<sup>1</sup>, ZHANG Can<sup>1,2</sup>, CHEN De-Yuan<sup>1</sup>

- 1. School of Information Science and Engineering, Graduate University, Chinese Academy of Sciences, Beijing 100049, China;
- 2. State Key Laboratory of Information Security, Graduate University, Chinese Academy of Sciences, Beijing 100049, China

Abstract:

We report the design and implementation of CCSDS image data compression (IDC) parallel scheme based on FPGA. This scheme includes four modules: discrete wavelet transform(DWT), direct coefficient quantified encoding, bit plane encoding(BPE),and code processing. In order to put on speed, we use the parallel scanning and parallel encoding in the BPE module. The experimental results show the feasibility and efficiency of this scheme, and compared to the modified method of CCSDS IDC serial encoding, the processing time has reduced by 13.6%. Our scheme is fit for image data compression in the space communication.

Keywords: CCSDS image compression bit plane encoding FPGA

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通讯作者:

作者简介:

作者Email: chenzhe07@mails.gucas.ac.cn

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