电子与信息学报
JOURNAL OF ELECTRONICS & INFORMATION TECHNOLOGY

电子与信息学报 » 2011, Vol. 33 » Issue (10) :2536-2540 DOI: 10.3724/SP.J.1146.2011.00363

基于FPGA的稀疏网络关键节点计算的硬件加速方法研究

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Node Importance Analysis in Complex Networks Based on Hardware Computing

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摘要 随着互联网、生物医学及社交网络等复杂网络研究的深入，如何寻找其等效图中关键节点越来越重要。中介中心度作为衡量图中节点重要性的主要指标，其单点的计算复杂度高达$O(N^3)$，因而成为关键节点计算问题的难点。该文在对传统的中介中心度快速算法进行分析之后，提出了一种适用于硬件设计的改进算法。同时，基于算法中各点独立、以及相邻计算间无数据依赖的特点，该文利用改进算法实现了一个流水线结构的8计算单元并行计算系统，并在FPGA上完成了硬件系统的设计和验证。通过对比8核CPU软件系统的计算时间，该文的硬件计算系统实现了4.31倍的加速比。

关键词： FPGA 中介中心度 硬件计算 复杂网络 图

Abstract： Betweenness centrality is a widely used indicator to measure the node importance in complex network s, but it is computationally-expensive to calculate betweenness centrality. In this paper, analysis on the traditional betweenness centrality algorithms is completed and a novel algorithm is proposed to meet the hardware design features. Based on this algorithm, parallel computing system is implemented on FPGA with task level coarse grained parallelism and pipeline based fine grained parallelism. The experimental results show that the FPGA based implementation achieves up to 4.31 times speedup compared with an 8-core CPU implementation.

Keywords： FPGA Betweenness centrality Hardware computing Complex networks Graphs

Received 2011-04-14;

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引用本文:

史圣卿, 陈凯, 汪玉, 罗嵘.基于FPGA的稀疏网络关键节点计算的硬件加速方法研究[J] 电子与信息学报, 2011,V33(10): 2536-2540

Shi Sheng-Qing, Chen Kai, Wang Yu, Luo Rong.Node Importance Analysis in Complex Networks Based on Hardware Computing[J] , 2011,V33(10): 2536-2540

链接本文:

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