电子与信息学报
JOURNAL OF ELECTRONICS & INFORMATION TECHNOLOGY

电子与信息学报 » 2010, Vol. 32 » Issue (6) :1395-1400 DOI: 10.3724/SP.J.1146.2008.01689

可编程逻辑阵列分段递进优化布局算法研究

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A Research on Subsection Progressive Optimization Placement Algorithm of FPGA

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摘要 为了提高FPGA(Field Programmable Gate Array)的布通率并优化电路的连线长度，在模拟退火算法的基础上，该文提出一种新的FPGA布局算法。该算法在不同的温度区间采用不同的评价函数，高温阶段采用半周长法进行快速优化布局，低温阶段在评价函数中加入变量因子并进行适度的回火处理，以此来优化布局。实验表明，该算法提高了布通率，优化了连线长度，与最具代表性的VPR(Versatile Place and Route)布局算法相比布线通道宽度提高了近6%，电路总的连线长度降低了4~23%。

关键词： FPGA 布局 评价函数 布通率 模拟退火 VPR (Versatile Place and Route)

Abstract： A novel FPGA simulated annealing placement algorithm is proposed to improve the routability and optimize the length of wires. Different cost functions are applied to different temperature range. In high temperature stage, the half perimeter method is utilized to fast optimize the placement; while in low temperature stage, a variable factor is added into the cost function and the reasonable temper process is also used to improve the quality of placement. Experiment results demonstrate that, compared with the VPR, the proposed method requires 6% fewer routing tracks and the length of wire is 4~23% shorter.

Keywords： FPGA Pacement Cost function Routability Simulated annealing VPR (Versatile Place and Route)

Received 2008-12-12;

通讯作者: 杨海钢

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引用本文:
崔秀海; 杨海钢; 龚 萧; 黄 娟; 谭宜涛.可编程逻辑阵列分段递进优化布局算法研究[J] 电子与信息学报, 2010,V32(6): 1395-1400

Cui Xiu-hai[①]; Yang Hai-gang[①]; Gong Xiao[①②]; Huang Juan[①②]; Tan Yi-tao[①②].A Research on Subsection Progressive Optimization Placement Algorithm of FPGA [J] , 2010,V32(6): 1395-1400

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