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ADSL中宽带ΣΔ调制器的系统设计

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摘要：

非对称数字用户环路（ADSL）是一种宽带接入网技术,对其调制解调器电路中模数转换器的带宽和精度要求较高。ΣΔ调制器具有高精度和低功耗的优点，但是由于采用过采样技术，其带宽较小。为了增加带宽适合宽带应用，本文采用基于块数字滤波器的调制器结构设计了应用于ADSL 的两通道二阶宽带ΣΔ调制器系统。该ΣΔ调制器在不提高系统时钟频率的条件下，可使系统的有效采样频率增为原来的两倍，从而使得其带宽增加1倍。采用带通噪声传递函数降低了由于通道系数失配而折叠到信号带宽内的噪声，提高了调制器的信号噪声失真比。利用SIMULINK软件工具对电路非理想特性进行了建模和仿真，仿真结果表明在系统时钟频率为71.4MHz，系数失配为0.5%的条件下，调制器的带宽为1.1MHz，噪声失真比为83.9dB，满足ADSL的应用要求，并且该调制器能够有效地抑制闲杂音,不需要采用随机扰动信号来抑制调制器的闲杂音,简化了后续的电路设计。

关键词： 块数字滤波器；ΣΔ调制器；折叠噪声

System Design of Broadband ΣΔ Modulator for ADSL Applications

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Abstract:

Asymmetric digital subscriber line (ADSL) is a broadband access network technology and needs broadband and high precision analog to digital convertors. ΣΔ modulator has the advantages of high resolution and low power, but its bandwidth is low because of adopting the oversampling technology. In order to increase the bandwidth for broadband applications, the system design of a broadband two-channel second-order ΣΔ modulator for ADSL applications is presented, which is based on the digital block filer theory. The effective sampling frequency of the modulator can be doubled with keeping the system clock frequency unchanging, which makes the bandwidth of the modulator double. To reduce the folded noise caused by mismatch between two channels, a band-pass filter is adopted. The system model with mismatch between two channels is built and simulated by SIMULINK. Simulation results show that the modulator achieves a signal to noise and distortion ratio of 83.9dB and a bandwidth of 1.1MHz with the system clock frequency of 71.4 MHz and mismatch of 0.5% between two channels. Furthermore, the modulator has the ability of idle tones suppression and does not need the dither signal generated by extra circuit to suppress the idle tones, reducing the complexity of the circuit.

Keywords: folded noise

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