

短文与研究通讯

低电压下CMOS数字电路概率模型研究

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摘要:

为解决数字电路低功耗问题, 电路工作电压被不断降低, 导致电路逻辑器件呈现概率特性。本文提出了低电压下CMOS数字电路的错误概率模型, 并完成硬件电路测试验证。本文首先详述了深亚微米(DSM)量级的门电路及模块在低电压供电条件下导致器件出错的因素, 结合概率器件结构模型推导基本逻辑门概率模型, 并提出了状态转移法用于完成由门级到模块级的概率分析模型; 我们搭建硬件平台对CMOS逻辑芯片进行了低供电压测试, 通过分析理论推导结果与实测结果, 验证并完善了分析模型。实验结果表明, 由状态转移法推导的电路概率模型符合电路实际性能, 从而为构建低电压下数字电路概率模型提供了可靠分析模型。

关键词: 低电压 概率器件 概率模型 状态转移法

The probabilistic model for CMOS digital circuits in low supply voltage

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Abstract:

In order to achieve the goal of low power consumption, the operating voltage is step-down, which leads to a soft error of logic devices. The probabilistic models of soft error for CMOS digital circuits with low supply voltage are proposed in this paper, and hardware circuit verification is also performed. The factors, which cause the soft error for deep submicron(DSM) CMOS logic device with low supply voltage, are introduced, and the probabilistic models for the logic gates are deduced based on the structure of devices. A novel state-transfer method is proposed to establish the probabilistic models for the digital circuit modules. In order to verify this method, we establish the hardware platform. The test results show that the probabilistic models, which obtained by the state-transfer method, match the circuits testing. Thus, proposed model can be used in the digital circuit performance study with low supply voltage.

Keywords: low voltage probabilistic device probabilistic model state-transfer method

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