

论文

基于GPGPU和CUDA的高速AES算法的实现和优化

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摘要:

随着高性能计算需求的不断增长,人们开始将目光投向具有强大计算能力及高存储带宽的GPU设备.与擅长处理复杂性逻辑事务的CPU相比,GPGPU(general purpose graphic processing unit,通用图形处理器)更适合于大规模数据并行处理.CUDA(compute unified device architecture,统一计算架构)的出现更加速了GPGPU应用面的扩张.基于GPGPU和CUDA技术对AES算法的实现进行加速,得到整体吞吐量6~7Gbit/s的速度.如果不考虑数据加载时间,对于1MB以上的输入规模,吞吐量可以达到20Gbit/s.

关键词: 通用图像处理器 统一计算架构 AES算法 并行计算

Implementation and optimization of high speed AES algorithm based on GPGPU and CUDA

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Abstract:

Compared with the CPU which is good at handling logic complexity service, GPGPU (general purpose graphic processing unit) is suitable for large-scale parallel processing computing. The emergence of CUDA (compute unified device architecture) accelerates the expansion of application of GPGPU. We accelerate the implementation of AES algorithm based on GPGPU and CUDA and achieve a total throughput of 6~7Gbit/s. Regardless of the time of data loading and storing, a throughput of 20Gbit/s towards an input size over 1MB can be achieved.

Keywords: GPGPU(general purpose graphic processing unit) CUDA(compute unified device architecture) AES algorithm parallel computing

收稿日期 2010-07-23 修回日期 2010-11-01 网络版发布日期

DOI:

基金项目:

中国科学院知识创新工程(YYYJ-1013)和国家科技支撑课题(2008BAH32B04)资助

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参考文献:

[1] Kedem G, Ishihara Y. Brute force attack on UNIX passwords with SIMD computer //Proceedings of the 8th USENIX Security Symposium.1999.

[2] Olano M, Lastra A. A shading language on graphics hardware: the PixelFlow shading system [J]. Journal of Computer Graphics,1998: 159-168.

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[3] Cook D L, Keromytis A D. Cryptographics: exploiting graphics cards for security //Advancements in Information Security Series. Springer, 2006.

[4] Cook D L, Ioannidis J, Keromytis A D, et al. CryptoGraphics: secret key cryptography using graphics cards //RSA Conference, Cryptographer's Track (CT-RSA). 2005.

[5] Cook D L, Baratto R, Keromytis A. Remotely keyed cryptographics secure remote display access using (mostly) untrusted hardware //ICICS05 Conference Proceedings. December 2005.

[6] Manavski S A. CUDA compatible GPU as an efficient hardware accelerator for AES cryptography //2007 IEEE International Conference on Signal Processing and Communications (ICSPC 2007). Dubai, United Arab Emirates, November 2007.

[7] Harrison O, Waldron J. AES encryption implementation and analysis on commodity graphics processing units //Ches 2007. LNCS,2007,4727:209-226.

[8] Fiorese C, Budak C. AES on GPU: a CUDA implementation //Proc of CHES. 2007.

[9] Yamanouchi T. GPU Gems 3 . chapter 36: AES encryption and decryption on the GPU . SEGA Corporation. http://http.developer.nvidia.com/GPUGems3/gpugems3_ch36.html.

[10] Biagio A D, Barengi A, Agosta G, et al. Design of a parallel aes for graphics hardware using the cuda framework //IEEE International Symposium on Parallel& Distributed Processing. May 2009.

[11] Joppe W Bos¹, Dag Arne Osvik, Deian Stefan. Fast implementations of AES on various platforms //EPFL IC IIF LACAL, Station 14, CH-1015 Lausanne, Switzerland Fjoppe Bos, Dept of Electrical Engineering. The Cooper Union, NY 10003, New York, USA,2009.

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1. 王润泽 王颖 杨栋毅.大规模FFT并行计算中2维SRAM的设计[J]. 中国科学院研究生院学报, 2008,25(1): 123-128