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10 Gbps LDPC编码器的FPGA设计

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FPGA-based Design of LDPC Encoder with Throughput over 10 Gbps

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摘要 该文针对准循环双对角结构的低密度奇偶校验(LDPC)码，提出了一种基于FPGA的高吞吐量编码器实现方法。提出了一种快速流水线双向递归编码算法，能显著提高编码速度；同时设计了一种行间串行列间并行的处理结构计算中间变量，在提高编码并行度的同时可有效减少存储资源的占用量；设计还针对多帧并行编码的情况优化了存储结构，有效复用了数据存储单元和RAM地址发生器，进一步提高FPGA的资源利用率。对一组码长为2304的IEEE 802.16e标准LDPC码，在Xilinx XC4VLX40芯片上，该方法可实现时钟频率200 MHz，信息吞吐量达10 Gbps以上的编码器，且占用不超过15%的芯片逻辑资源和50%左右的RAM存储资源。

关键词： 低密度奇偶校验(LDPC)码 编码器 高吞吐量

Abstract: This paper presents a high-throughput encoding method for IEEE 802.16e-like Low-Density Parity-Check (LDPC) codes. It is based on a fast double-recursion pipeline method, and can significantly improve the encoding speed. For more parallelism and less storage consumption, a partially-parallel architecture is designed. Furthermore, the storage system is optimized for parallel multi-frame coding, and the data storage unit and RAM address generator are shared for improving resource utilization. Design results are provided for an implementation on a Xilinx XC4VLX40 FPGA for codes with code length 2304 bit. It is shown that the proposed method can achieve a throughput in excess of 10 Gbps under a maximum clock frequency of 200 MHz, with the requirement of no more than 15% gate area and about 50% RAM storage.

Keywords: Low-Density Parity-Check (LDPC) code Encoder High throughput

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