



教職員工

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潘权 副教授

个人简介

潘权博士, 主要研究工作集中在高速模拟/射频集成电路设计, 主要包括: Wireline/Wireless高速通信集成电路(接收机/发射机)、Serdes/clock and data recovery (CDR) 电路、低噪声放大器/频率综合器、GaN集成电路、硅光互连研究。课题负责人不仅在国际主流会议/期刊上发表多篇高水平学术论文, 同时有超过8年丰富的国内外工作经验, 包括4年硅谷业界最前沿的工作经验。

个人主页

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招聘信息: 本课题组目前正在招聘研究助理教授、博士后、科研助理、博士生、硕士生, 同时欢迎来自国内外一流大学的访问学者和交流学生(招聘信息有效中), 有意加入者请将申请邮件以及简历发送至: panq@sustech.edu.cn。

教育经历

- 2014 香港科技大学电子及计算机工程学系, 博士学位
- 2005 中国科学技术大学电子科学与技术系, 学士学位

工作经历

2018-至今 南方科技大学, 助理教授

研究简介

- 高速光通信集成电路
- 硅光互连研究
- Serdes/CDR电路
- 模拟/射频集成电路

所获荣誉

- 2017 杰出青年作者奖, IEEE电路系统协会。
- 2014 创新奖, 第四届香港科大百万创业大赛

代表文章

1. J. Wang, Q. Pan* et al., "A Fully-Integrated 25Gb/s Low-Noise TIA+CDR Optical Receiver Designed in 40nm-CMOS," TCAS-II, DOI 10.1109/TCSII.2019.2925363, Jun. 2019.
2. Q. Pan et al., "A 42-dBΩ 25-Gb/s CMOS Transimpedance Amplifier with Multiple-Peaking Scheme for Optical Communications," IEEE Transactions on Circuits and Systems II: Express Briefs, Feb. 2019.
3. Y. Guo, and Q. Pan, "A PAM-4 80-Gb/S Variable-Gain Transimpedance Amplifier in 40-nm CMOS Technology," in IEEE International Conference on Integrated Circuits, Technologies and Applications, Nov. 2018.
4. Q. Pan, Y. Wang, Z. Hou, L. Sun, L. Wu, W. H. Ki, P. Chiang, and C. P. Yue, "A 41-mW 30-Gb/s CMOS Optical Receiver with Digitally-Tunable Cascaded Equalization," in Proc. European Solid-State Circuits Conf., Sep. 2014.
5. Q. Pan, Z. Hou, Y. Wang, Y. Lu, W. H. Ki, K. C. Wang, and C. P. Yue, "A 48-mW 18-Gb/s Fully Integrated CMOS Optical Receiver with Photodetector and Adaptive Equalizer," in Symp. VLSI Circuits Dig. Tech. Papers, pp. 116-117, Jun. 2014.
6. Q. Pan, Z. Hou, Y. Li, A. W. Poon, and C. P. Yue, "A 0.5-V P-Well/Deep N-Well photodetector in 65-nm CMOS for monolithic 850-nm optical receivers," IEEE Photonics Technology Letters (PTL), vol. 26, no. 12, pp. 1184-1187, Jun. 2014.
7. Q. Pan, T. J. Yeh, C. Jou, F. L. Hsueh, H. Luong, and C. P. Yue, "A performance study of layout and Vt options for low noise amplifier design in 65-nm CMOS," in IEEE Radio Frequency Integrated Circuits Symp., pp. 535-538, Jun. 2012.
8. G. Zhu, Q. Pan, J. Zhuang, C. Zhi, and C. P. Yue, "A Low-Power PAM4 Receiver Using 1/4-Rate Sampling Decoder with Adaptive Variable-Gain Rectification," in 2017 IEEE Asian Solid-State Circuits Conf., Nov. 2017.
9. Y. Wang, D. Luo, Q. Pan, L. Jing, Z. Li, and C. P. Yue, "A 60-GHz 4-Gb/s Fully Integrated NRZ-to-QPSK Fiber-Wireless Modulator," IEEE Transactions of Circuits and Systems-I (TCAS-I), vol. 64, issue. 3, pp. 653-663, Mar. 2017.
10. L. Sun, Q. Pan, K. C. Wang, and C. P. Yue, "A 26-28-Gb/s clock and data recovery circuit with embedded equalizer in 65-nm CMOS," IEEE Transactions of Circuits and Systems-I (TCAS-I), vol. 61, no. 7, pp. 2139-2149, Jul. 2014.

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